

INDUSTRIAL STRENGTH... Start Your Application From **YOURITECH**

Integration support

Obsolescence Management

PCAP

Embedded Systems

Human Machine Interface

Touch Solutions

Software

Production Custom designs Installation

Quality Management

Open Frame Monitors

LCD Controller

Research & Development

Firmware

EMC tests

on-site service

In-house Manufacturing

Optical Bonding

Cover glass

System solutions

OEM Solutions

Custom Display

Mechanical design



MODEL NO : ET062NH01-T

MODEL VERSION: 01

SPEC VERSION : 1.0

ISSUED DATE: 2022-11-29

☐ Preliminary Specification

☒ Final Product Specification

Customer : _____

Approved by	Notes

Youri Confirmation

Prepared by	Reviewed by	Approved by
John	Johnny	Wang

1. Introduction

1.1 Scope of application

LCD specification: Dots 360xRGBx960

As to basic specification of the driver IC, refer to the IC (ST7701SN) specification and data book.

All material & processing of the LCD module should be Lead Free.

1.2 TFT features:

Structure: TFT PANNEL+IC +FPC+BL;

ALL O'CLOCK Type LCD

360 dot-segment and 960 dot-common outputs;

16.7M Color can be selected by software;

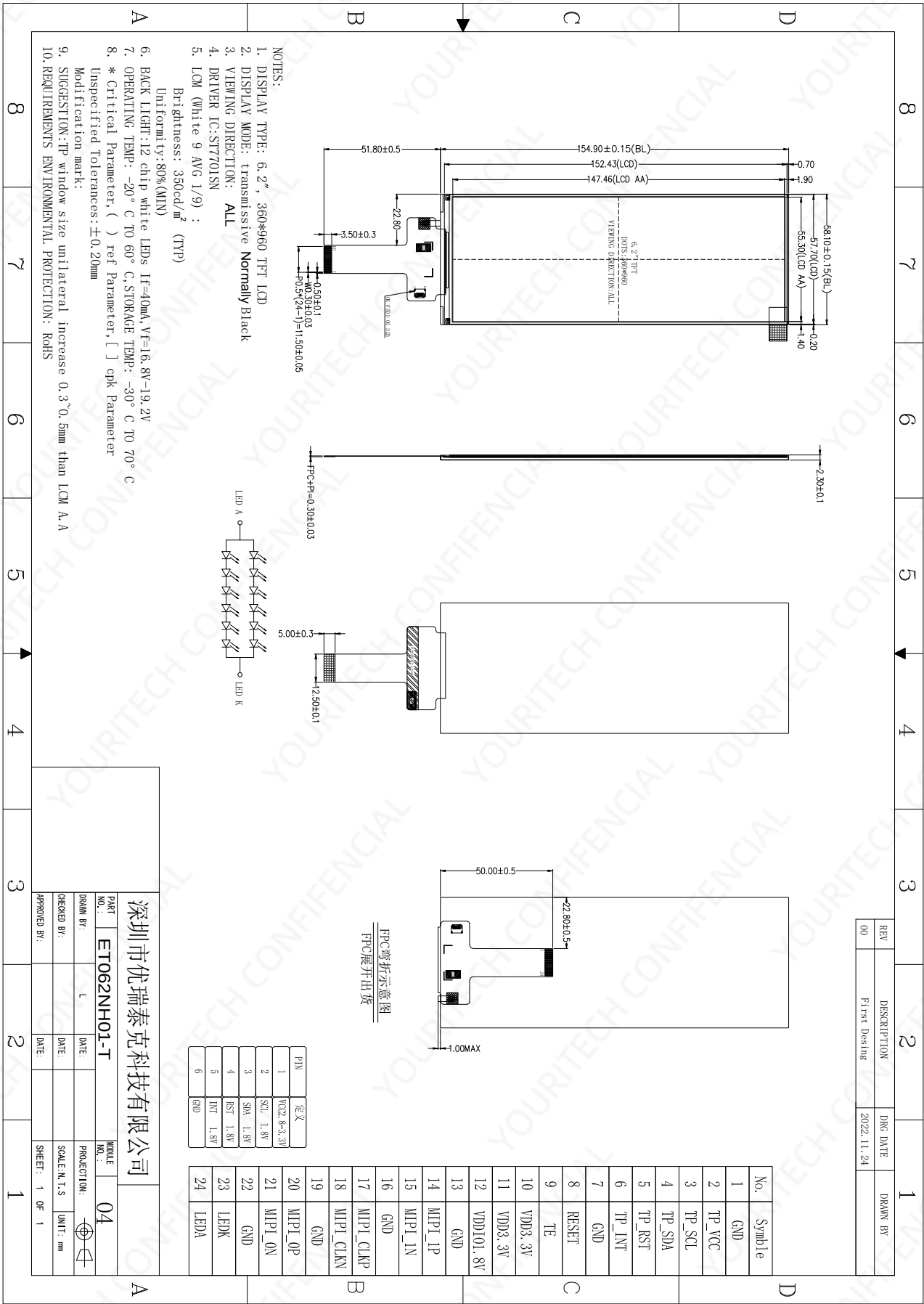
White LED back light;

2lane MIPI interface

1.3 Applications:

2. LCM General specification

ITEM	Standard value	Unit
LCD Type	Normally Black	--
Drive element	TFT active matrix	--
Number of pixels	360*3RGB(H)X960(V)	Dots
Pixel arrangement	RGB Vertical Stripe	--
Pixel Pitch (W*H)	0.1536 (H) x 0.1536 (V)	mm
Active area	55.30(H) x 147.46(V)	mm
Viewing direction	ALL O'CLOCK	-
TFT Driver IC	ST7701SN	
TFT interface	2lane MIPI Interface	-
LCM Size(W*H*T)	58.10(W) ×154.90(H) ×2.30(T)	mm
Approx. Weight	TBD	g
Touch structure		
Touch Driver IC		
Touch Interface		



3.Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
LCM Operating Temperature	T _{OPR}	-20	+60	°C
LCM Storage Temperature	T _{STG}	-30	+70	°C
Humidity	RH	-	90	%

4.Electrical Characteristics

4.1 TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage for I/O	IOVCC	1.65	1.8	3.3	V
Supply Voltage for(DC/DC)	VDD	2.5	3.3	3.3	V
Supply Voltage for(DC/DC)	AVDD				V
Supply Voltage for(DC/DC)	AVEE				V

4.2 Back-Light Unit Characeristics

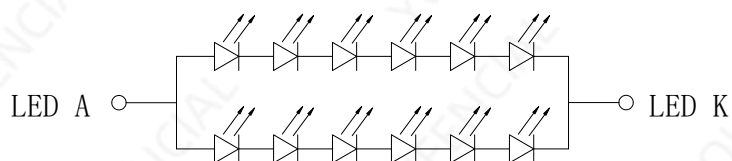
The back-light system is an edge-lighting type with 12 white LEDs. The characteristics of the back-light are shown in the following tables.

Characteristics	Symbol	Min.	Type	Max.	Unit	Notes
Forward Voltage	V _F	16.8		19.2	V	-
Forward current	I _F	--	40	-	mA	-
Luminance(With LCD)	L _v		350	--	cd/m ²	-
LED life time	N/A	----	30,000	--	Hr	Note 1

Note:

- (1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=20mA/LED. The LED life time could be decreased if operating I_L is larger than 25mA/LED.

Backlight circuit diagram shown in below:



5. Module Function Description

Pin No.	Symbol	Functional	Notes
1	GND	Power Ground	
2	CTP_VCC 2.8- 3.3V	Touch panel Power supply 2.8~3.3V	
3	CTP_SCL 1.8V	Touch panel I2C clock	
4	CTP_SDA 1.8V	Touch panel I2C data	
5	CTP_RST 1.8V	Touch panel reset	
6	CTP_INT 1.8V	Touch panel interrupt output	
7	GND	Power Ground	
8	RESET	Reset signal input terminal. Active at ‘L’ .	
9	TE	Frame head pulse for tearing effect.	
10-11	VDD 3.3V	Power Supply For LCD.	
12	IOVCC 1.8V	Power Supply For I/O.	
13	GND	Power Ground	
14	D1P	Positive polarity of low voltage differential data 1 signal	
15	D1N	Negative polarity of low voltage differential data 1 signal	
16	GND	Power Ground	
17	CLKP	Positive polarity of low voltage differential clock signal	
18	CLKN	Negative polarity of low voltage differential clock signal	
19	GND	Power Ground	
20	D0P	Positive polarity of low voltage differential data 1 signal	
21	D0N	Negative polarity of low voltage differential data 1 signal	
22	GND	Power Ground	
23	LEDK	Power supply for backlight cathode input terminal.	
24	LEDA	Power Supply For LED Backlight Anode Input.	

6. Timing Characteristics

POWER ON/OFF SEQUENCE

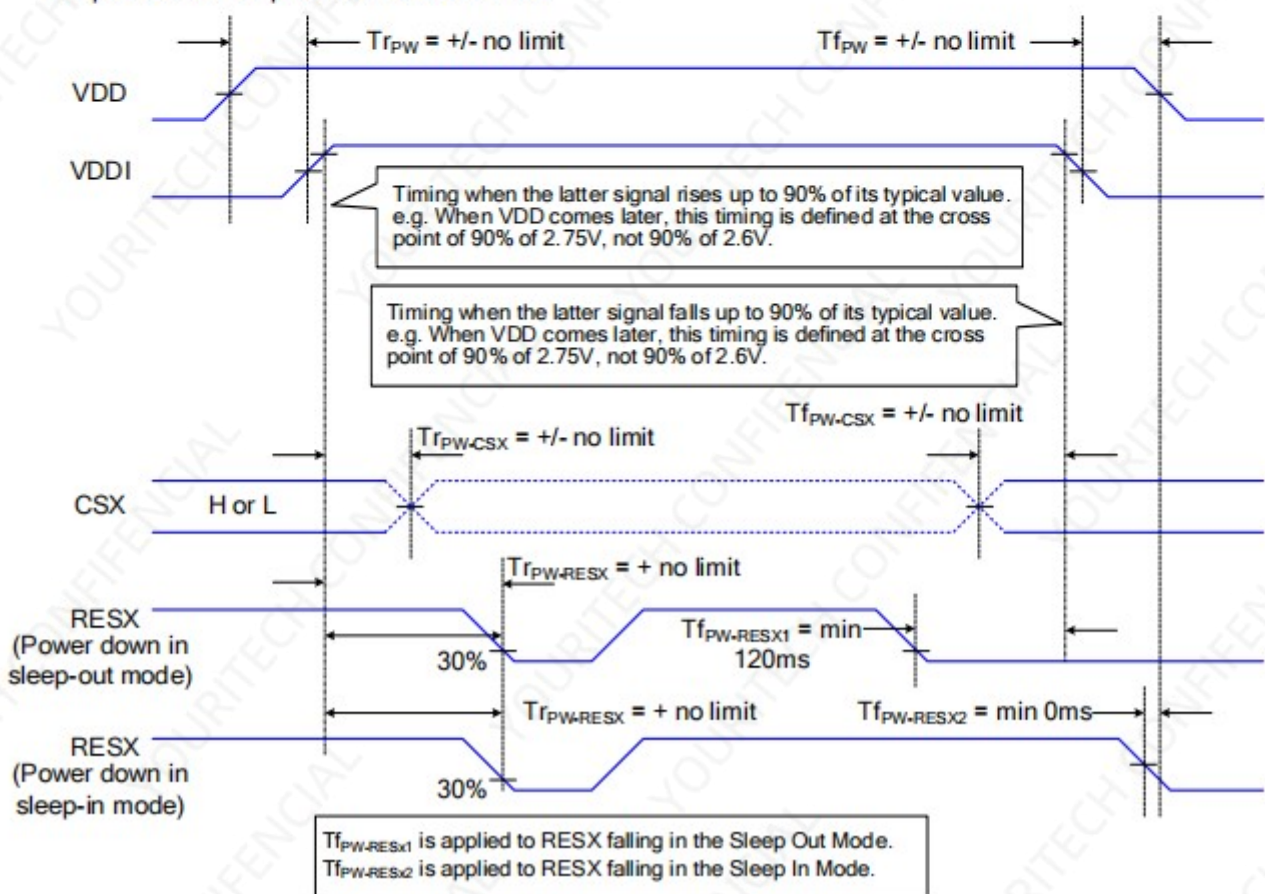
VDDI and VDDA can be applied or powered down in any order. During the Power Off sequence, if the LCD is in the Sleep Out mode, VDDA and VDDI must be powered down with minimum 120msec. If the LCD is in the Sleep In mode, VDDA and VDDI can be powered down with minimum 0msec after the RESX is released.

CSX can be applied at any timing or can be permanently grounded. RESX has high priority over CSX.

Notes:

1. There will be no damage to the ST7701SN if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
3. There will be no abnormal visible effects on the display between the end of Power On Sequence and before receiving the Sleep Out command, and also between receiving the Sleep In command and the Power Off Sequence.
4. If the RESX line is not steadily held by the host during the Power On Sequence as defined in Sections 9.1 and 9.2, then it will be necessary to apply the Hardware Reset (RESX) after the completion of the Host Power On Sequence to ensure correct operations. Otherwise, all the functions are not guaranteed.

The power on/off sequence is illustrated below



Uncontrolled Power Off

The uncontrolled power-off means a situation which removed a battery without the controlled power off sequence. It will neither damage the module or the host interface.

If uncontrolled power-off happened, the display will go blank and there will not any visible effect on the display (blank display) and remains blank until "Power On Sequence" powers it up.

MIPI Interface Characteristics:

High Speed Mode



Figure 4 DSI clock channel timing

Figure 5 Rising and falling time on clock and data channel

VDDI=1.8, VDD=2.8, AGND=DGND=0V, Ta=25 °C

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-CLK+/-	$2xU_{INSTA}$	Double UI instantaneous	2.5	25	ns	
DSI-CLK+/-	U_{INSTA} U_{INSTB}	UI instantaneous halves	1.25	12.5	ns	$UI = U_{INSTA} = U_{INSTB}$
DSI-Dn+/-	t_{DS}	Data to clock setup time	0.15	-	UI	
DSI-Dn+/-	t_{DH}	Data to clock hold time	0.15	-	UI	

Table 7 Mipi Interface- High Speed Mode Timing Characteristics

Low Power Mode

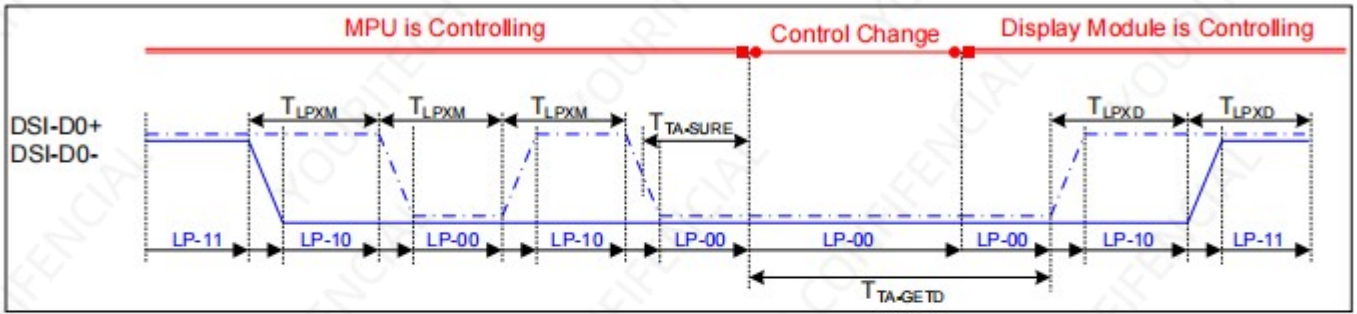


Figure 6 Bus Turnaround (BTA) from display module to MPU Timing

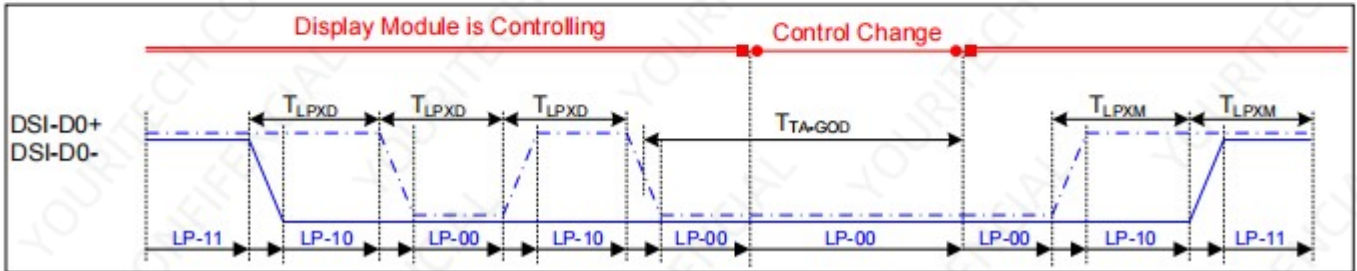


Figure 7 Bus Turnaround (BTA) from MPU to display module Timing

$VDDI=1.8, VDD=2.8, AGND=DGND=0V, T_a=25^\circ C$

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-D0+/-	TLPXM	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Input
DSI-D0+/-	TLPXD	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Output
DSI-D0+/-	TTA-SURED	Time-out before the MPU start driving	T_{LPXD}	$2 \times T_{LPXD}$	ns	Output
DSI-D0+/-	TTA-GETD	Time to drive LP-00 by display module	$5 \times T_{LPXD}$		ns	Input
DSI-D0+/-	TTA-GOD	Time to drive LP-00 after turnaround request-MPU	$4 \times T_{LPXD}$		ns	Output

Table 8 Mipi Interface Low Power Mode Timing Characteristics

DSI Bursts Mode

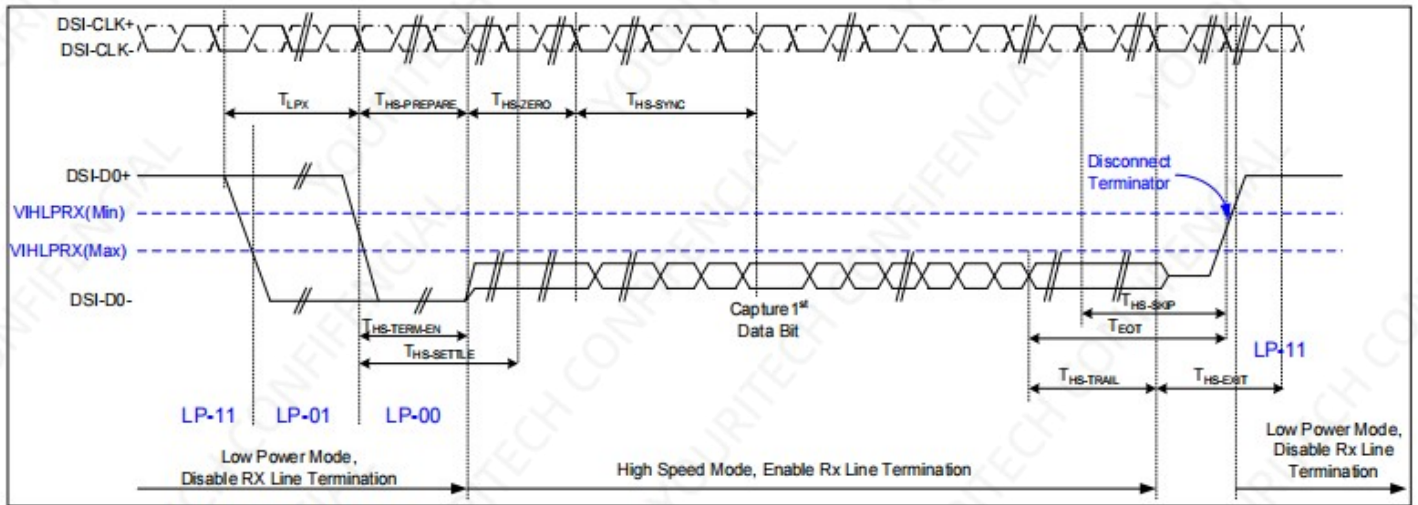


Figure 7 Data lanes-Low Power Mode to/from High Speed Mode Timing

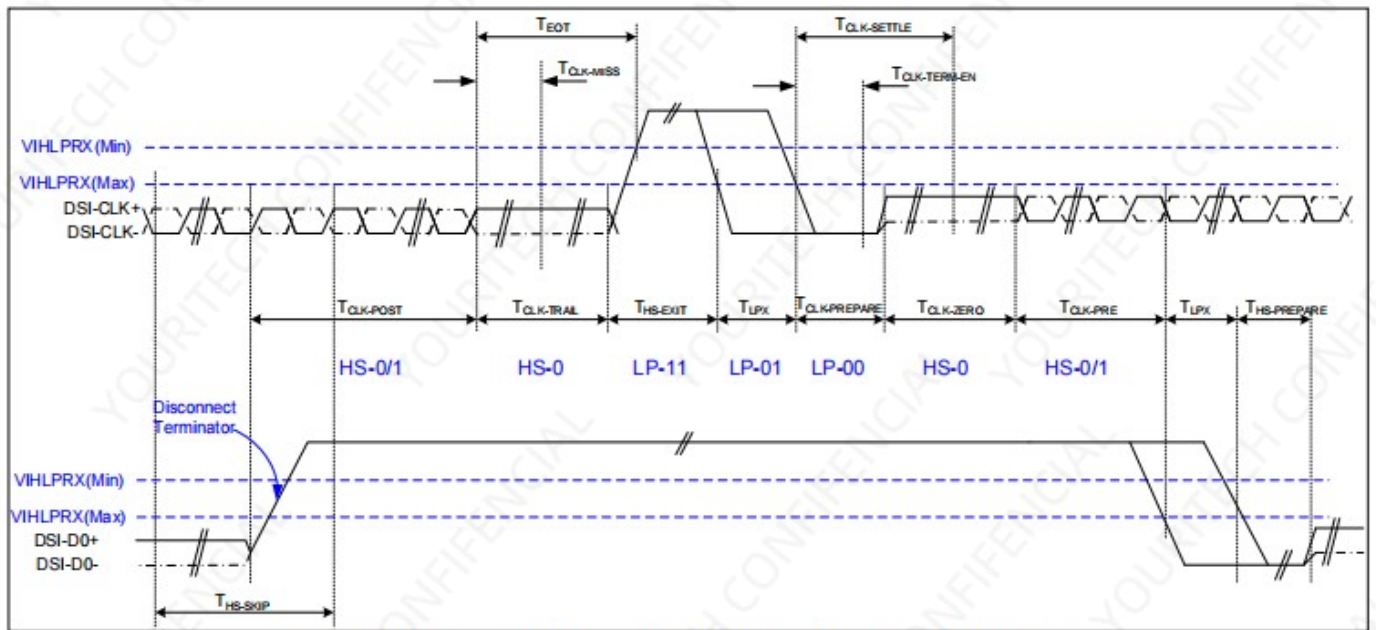


Figure 8 Clock lanes- High Speed Mode to/from Low Power Mode Timing

VDDI=1.8, VDD=2.8, AGND=DGND=0V, Ta=25 °C

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing						
DSI-Dn+/-	TLPX	Length of any low power state period	50	-	ns	Input
DSI-Dn+/-	THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40+4 UI	85+6 UI	ns	Input
DSI-Dn+/-	THS-TERM-EN	Time to enable data receiver line termination measured from when Dn crosses VILMAX	-	35+4 UI	ns	Input
DSI-Dn+/-	THS-PREPARE + THS-ZERO	THS-PREPARE + time to drive HS-0 before the sync sequence	140+ 10UI	-	ns	Input
High Speed Mode to Low Power Mode Timing						
DSI-Dn+/-	THS-SKIP	Time-out at display module to ignore transition period of EoT	40	55+4 UI	ns	Input
DSI-Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-Dn+/-	THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4 UI	-	ns	Input
High Speed Mode to/from Low Power Mode Timing						
DSI-CLK+/-	TCLK-POS	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+5 2UI	-	ns	Input
DSI-CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns	Input
DSI-CLK+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS transmission	38	95	ns	Input
DSI-CLK+/-	TCLK-TERM-EN	Time-out at clock lan display module to enable HS transmission	--	38	ns	Input
DSI-CLK+/-	TCLK-PREPARE + TCLK-ZERO	Minimum lead HS-0 drive period before starting clock	300	-	ns	Input
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8UI	-	ns	Input
DSI-CLK+/-	TEOT	Time form start of TCLK-TRAIL period to start of LP-11 state	-	105n s+12 UI	ns	Input

Reset Description:

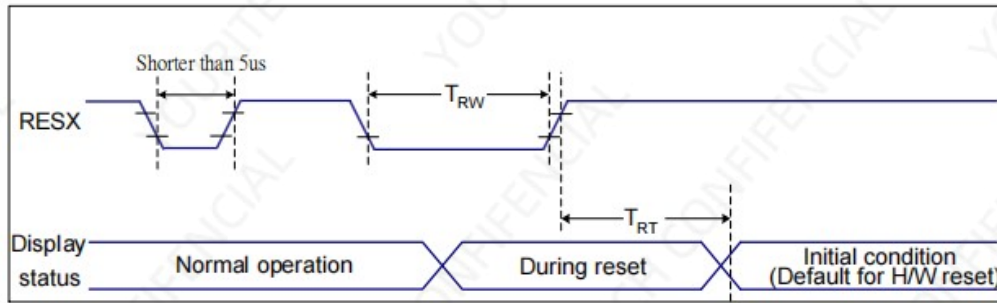


Figure 9 Reset Timing

VDDI= 1.8, VDD=2.8, AGND=DGND=0V, Ta=25 °C

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5) 120(Note 1, 6, 7)	ms

Table 9 Reset Timing

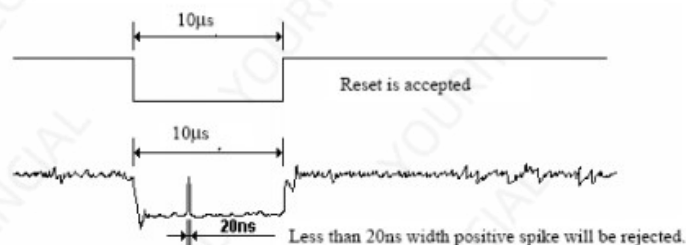
Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

7. Optical Characteristics

Optical Specification

The test of Optical specifications shall be measured in a dark room (ambient luminance $\leq 1\text{lu}$ x and temperature = $25\pm 2^\circ\text{C}$) with the equipment of Luminance meter system (Goniometer system and TOPCON BM-5) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and Φ equal to 0° . The center of the measuring spot on the Display surface shall stay fixed.

The backlight should be operating for 30 minutes prior to measurement.

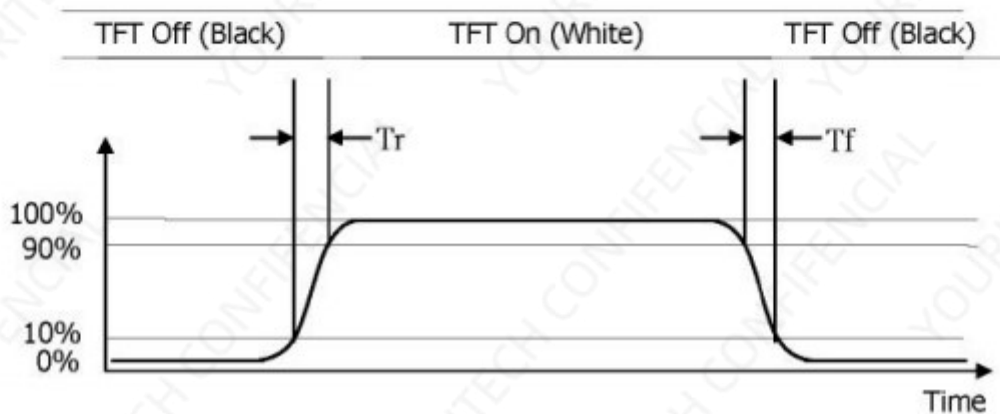
Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle range	Horizontal	Θ_3	CR > 10	80	89	-	Deg.	Note 1
		Θ_9		80	89	-	Deg.	
	Vertical	Θ_{12}		80	89	-	Deg.	
		Θ_6		80	89	-	Deg.	
Luminance Contrast ratio		CR	$\Theta = 0^\circ$	900	1200	-		Note 2
Color Gamut	NTSC	CIE1931	$\Theta = 0^\circ$	61	66	-	%	Note 5 @C Light
Reproduction of color	White	W _x	$\Theta = 0^\circ$	Typ -0.03	0.286	Typ +0.03		
		W _y			0.318			
Response Time		GTG ave	Ta= 25° C $\Theta = 0^\circ$	-	35	40	ms	Note 6
Cross Talk		CT	$\Theta = 0^\circ$	-	-	2.0	%	

Note :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface.
2. Contrast measurements shall be made at viewing angle of $\theta = 0^\circ$ and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (See FIGURE 1 shown in Appendix) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Center Luminance of white is defined as the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in FIGURE 4 for a total of the measurements per display.
4. The White luminance uniformity on LCD surface is then expressed as : $\Delta Y = \frac{\text{Minimum Luminance of 9 Points or 5 points}}{\text{Maximum Luminance of 9 Points or 5 points}}$ (See FIGURE 2).
5. The color chromaticity coordinates specified in Table 5. shall be calculated from the spectral data measured with C light. Measurements shall be made at the center of the panel.
6. The electro-optical response time measurements shall be made as FIGURE 5 shown in Appendix by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is T_d , and 90% to 10% is T_r .



8. Reliability Test Item

No.	Test Item	Test Condition	Notes
1	High Temp. Storage	+70°C / 96H	1. Functional test isOK. Missing Segment,short, unclear segment non-display,display abnormally and liquid crystal leakare un-allowed. 2. No low temperature bubbles,end seal loose andfall, frame rainbow.
2	Low Temp. Storage	-30°C / 96H	
3	High Tempe. Operating	+60°C / 96H	
4	Low Tempe. Operating	-20°C / 96H	
5	High Temperature /Humidity storage	50°C x 90%RH /96H	
6	Thermal and cold shock	Static state, -20°C (30min) ~60°C (30min) , 50 cycles	

9. Packing Method----TBD

- END -