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■ Preliminary Specifications

☐ Final Specifications

Title	6.7-inch LCM Product Specifications
Model Name	ET067FH01-R
Version	P0

Customer

Approved by Date

Notice: This Specification is subject to change without notice.

Approved By	Prepared By
Leo 2026-03-16	Aurice 2026-03-16

REVISION HISTORY

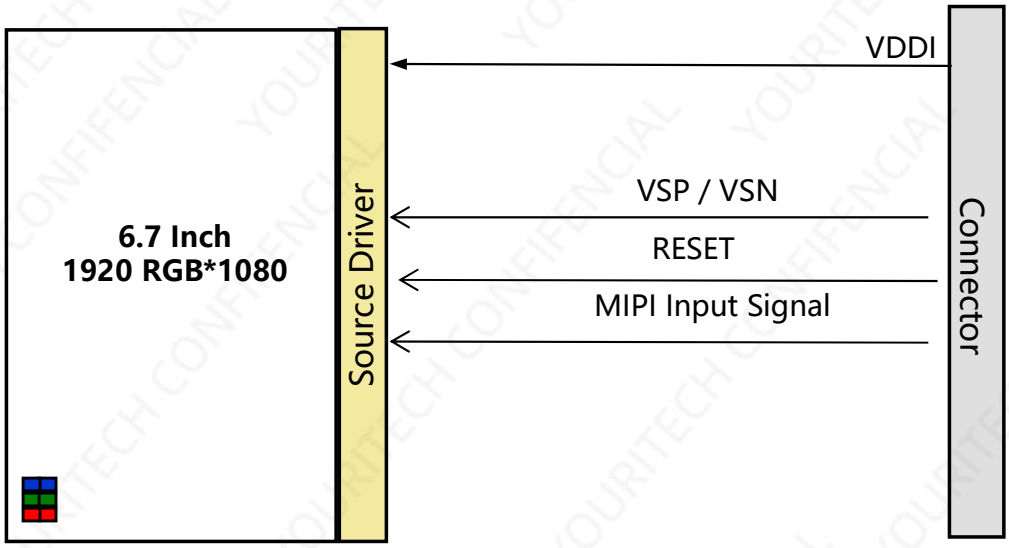
REV.	PAGE	DESCRIPTION OF CHANGES	DATE	PREPARED
P0		Initial Release	2026.03.13	Aurice

CONTENTS

1.0 GENERAL DESCRIPTION

ET067FH01-R is a color active matrix a-Si LCM, using a-Si (amorphous silicon) TFTs (Thin Film Transistors) as an active switching devices. The LCM has a **6.7 inch** diagonall y measured active area with 1920×1080resolutions (1920 horizontal by 1080 vertical pixel arra y). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this FOG can display 16.7M colors.

<Figure 1. FOG>



1.2 Features

- PPI: 328
- Color Gamut: NTSC 60%(Typ)
- MIPI Interface
- RoHS Compliant

1.3 Application

- **HMI**

1.4 General Specification

<Table 1. General Specifications> [Ta= 25±2℃]

Parameter	Specification	Unit	Remark
Dimensional Outline	156.32×99.63 ×3.0	mm	m
Active Areae	148.32(H) ×83.43 (V)	m	Note 1.1
Power consumption	6.0W(BL)(fog unknown)	W	電流:175mA /電壓 :32V
Number of Pixels	1920(H)x1080(V)	pixels	-
Pixel Pitch	25.75(H) x77.25 (V)	μm	-
Pixel Arrangement	RGB Vertical Stripe	-	-
Display Colors	16.7M	-	-
Color Gamut	60% (Typ.)		CF @C Light
Display Mode	Normally Black	-	-
Viewing Direction	85/85/85/85 (Typ.)	Deg.	CR>=10
Weight	TBD	gram	-
IC	GH8323-i1*2		Note 1.2

Note 1.1: H: horizontal length, V: vertical length.

Note 1.2: Compatible ICs for this product include GH8323-i1,Please contact IC manufacturer and vetify it when you choose any one of them.The information we suppose about IC just for reference.

2.0 ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage values are listed in Table 2. All the measurements should be operated with driver IC and FPC mounted.

<Table 2. Absolute Maximum Ratings>

Parameter	Symbol	Min.	Max.	Unit	Remarks
Supply Voltage	VDDI	-0.3	+3.6	V	Note 1&2
	VSP	-0.3	6.6	V	
	VSN	-0.3	-6.6	V	
Operating Temperature (Humidity)	T_{OP}	-30	+80	℃	
	RH	10	90	%	At 60° C
Storage Temperature (Humidity)	T_{ST}	-30	+80	℃	
	RH	10	90	%	At 60° C

Note:

1. These range above is maximum value not the actual operating temperature . Actual Operating temperature is no more than 40℃ and temperature refers to the LCM surface temperature ;

2.BOE is not responsible for product problems beyond the use conditions.

3.0 ELECTRICAL SPECIFICATIONS

3.1 Electrical Specifications

<Table 3. LCD FOG Electrical Specifications >

Parameter		Symbol	Values			Unit	Notes
			Min.	Typ.	Max.		
Power Supply Input Voltage		VDDI	2.5	-	3.6	V	Ta = 25 ℃ Note 1
		VSP	4.5	-	6.3	V	
		VSN	-4.5	-	-6.3	V	
Current Consumption	Operating	VCC=IOVCC	-	-	-	mW	-
	Sleep in	VCC=IOVCC	-	-	-	uW	

Note:

1.This is the voltage range of the IC. In this range, when the voltage is too low, the brightness of LCD may decrease

4.0 INTERFACE CONNECTION.

4.1 Electrical Interface Connection

The Interface Connector assignments are listed in Table 4

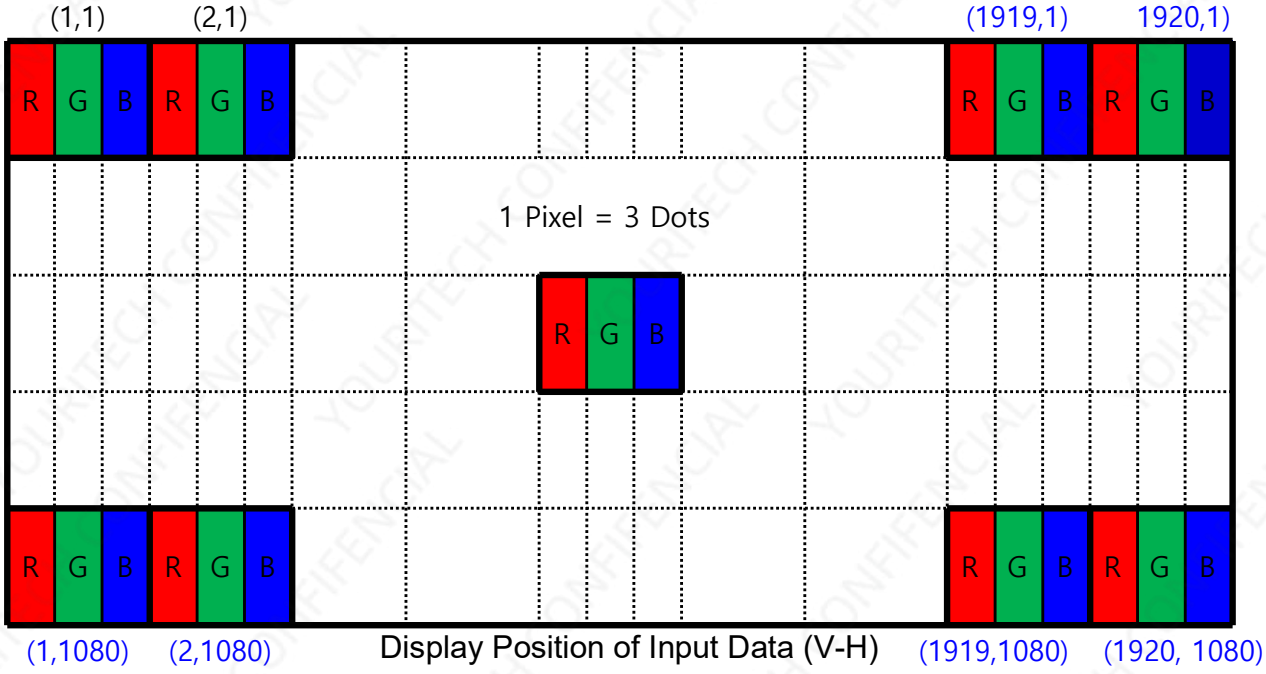
< Table 4. Pin Assignments for the Interface Connector >

No.	Symbol	No.	Symbol	No.	Symbol	No.	Symbol
1	NC	11	MIPI_1N	21	MIPI_3P	31	LED-
2	IOVCC	12	MIPI_2P	22	GND	32	LED-
3	IOVCC	13	GND	23	NC	33	NC
4	GND	14	MIPI_CKN	24	NC	34	VSN
5	RST	15	MIPI_CKP	25	GND	35	VSN
6	NC	16	GND	26	NC/TE	36	NC
7	GND	17	MIPI_2N	27	PWMO	37	VSP
8	MIPI_0N	18	MIPI_2P	28	NC/BIST	38	VSP
9	MIPI_0P	19	GND	29	NC	39	LED+
10	GND	20	MIPI_3N	30	GND	40	LED+

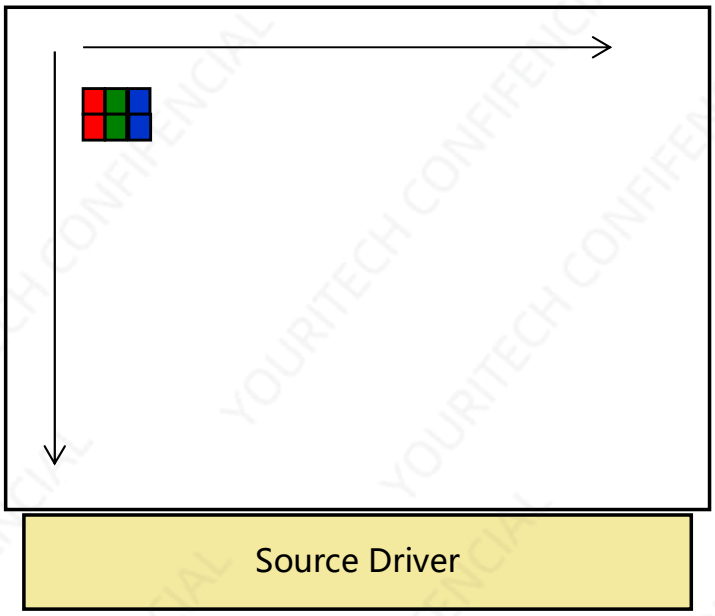
CN型号: FP0521 40PIN or EQU

4.2 Data Input Format

<Figure 2. Pixel Format>



<Figure 3. Scan direction>



4.3 MIPI Interface Timing

4.3.1 MIPI DSI Timing Characteristics

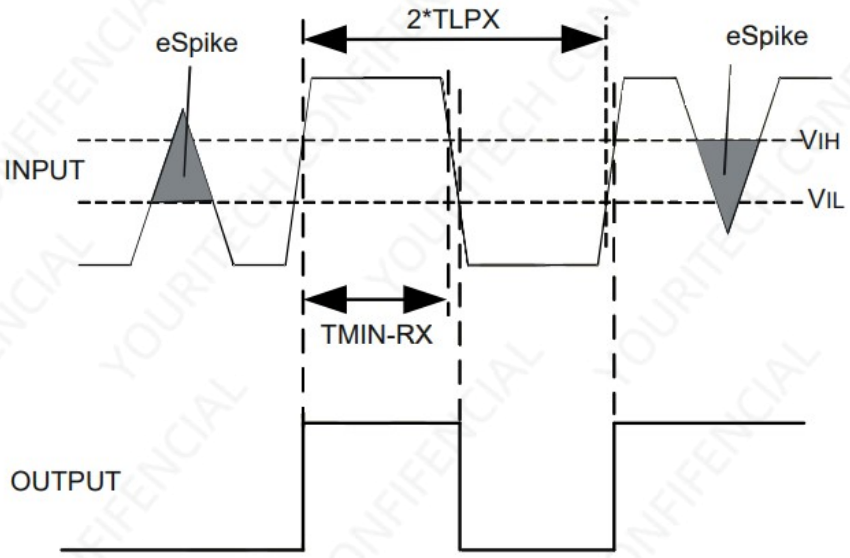
<Table 5. MIPI Interface Timing Specifications >

Item	Symbols		Min	Typ	Max	Unit	Note
DCLK	Period	tCLK	14.26	13.92	12.48	ns	
	Frequency	-	70.1	75.2	80.1	MHz	
Hsync	HSYNC period time	tHT	1945	1960	1980	tCLK	
	Horizontal Valid	tHV	1920			tCLK	
	Horizontal Blank	tHB	20	20	20	tCLK	
	Horizontal front porch	fHF	5	20	40	tCLK	
	HSYNC pulse width	fHW	2	-	10	tCLK	
Vsync	VSYNC period time	tVT	1200	1280	1350	tHP	
	Vertical Valid	tV	1080			tHP	
	Vertical Blank	tVB	88	88	88	tHP	
	VSYNC front porch	fVF	32	12	182	tHP	
	VSYNC pulse width	fVW	20	-	40	tHP	

4.3.2 MIPI Rx Interface Timing Parameter

The specification of the MIPI Rx interface timing parameter is shown in Figure 7.

< Figure 4. MIPI Rx Interface Timing >



< Table 6 Input Glitch Rejections of Low-Power Receivers>

Parameter	Description	Min.	Typ.	Max.	Unit	Note
VIH	Logic 1 input threshold	880	-	-	mV	-
VIL	Logic 0 input threshold, not in ULP state	-	-	550	mV	-

< Table 7 LP-RX DC Specifications >

Parameter	Description	Min.	Typ.	Max.	Unit	Note
eSPIKE	Input pulse rejection	-	-	300	V.ps	1, 2, 3
TMIN	Minimum pulse width response	20	-	-	ns	4
VINT	Peak-to-peak interference voltage	-	-	200	mV	-
fINT	Interference frequency	450	-	-	MHz	-

Note:
1. Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1 state
2. An impulse less than this will not change the receiver state.
3. In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.
4. An input pulse greater than this shall toggle the output.

< Table 8. High-Speed Receiver (RX) >

Parameter	Description	Min.	Typ.	Max.	Unit	Note
VCMRXDC	Common-mode voltage HS receive mode	70	-	330	mV	1,2
VIDTH	Differential input high threshold	-	-	70	mV	-
VIDTL	Differential input low threshold	-70	-	-	mV	-
VIHHS	Single-ended input high voltage	-	-	460	mV	1
VILHS	Single-ended input low voltage	-40	-	-	mV	1
ZID	Differential input impedance	80	100	125	Ω	-

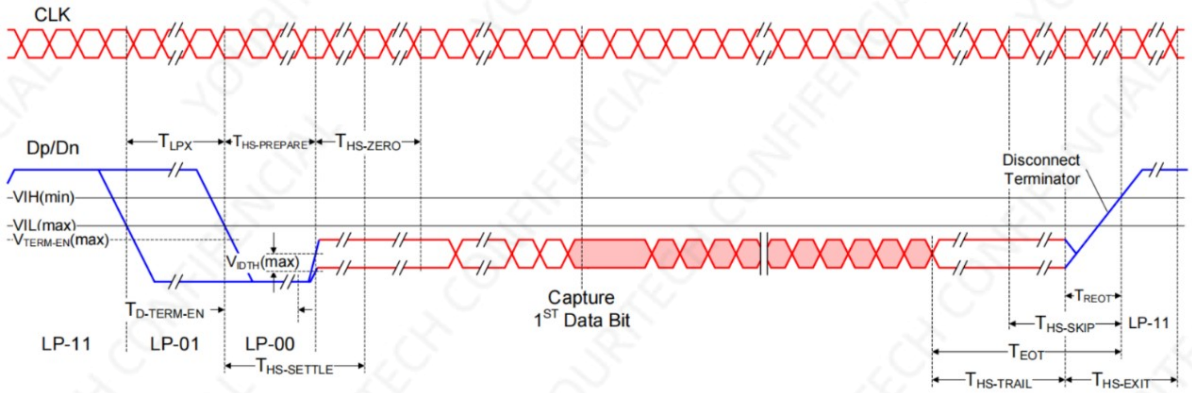
Note:
1. Excluding possible additional RF interference of 100mV peak sine wave beyond 450M Hz.
2. This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level
tolerance and variations below 450MHz

< Table 9. HS Receiver DC Specifications >

Parameter	Description	Min.	Typ.	Max.	Unit	Note
ΔVCMRX(HF)	Common mode interference beyond 450 MHz	-	-	100	mV_{pp}	1
CCM	Common mode termination	-	-	60	pF	2

Note:
1. ΔVCMRX(HF) is the peak amplitude of a sine wave superimposed on the receiver inputs.
2. For higher bit rates a 14pF capacitor will be needed to meet the common-mode return lo ss specification.

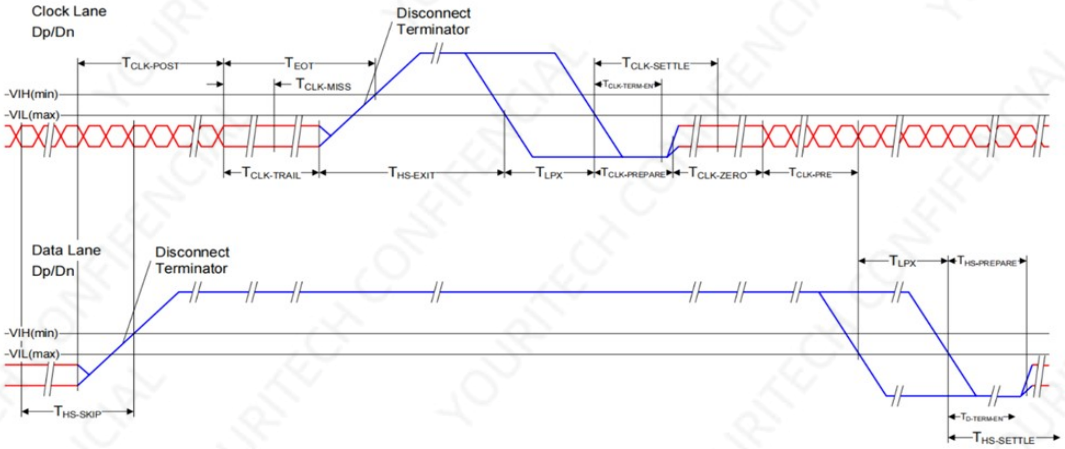
< Figure 5. Burst Mode Data Transmission >



< Table 10. Burst Mode Data Transmission Specifications >

Parameter	Description	Min	Typ	Max	UNIT
TLPX	Transmitted length of any Low-Power state period	50	-	-	ns
THS-PREPARE	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40 + 4*UI	-	85 + 6*UI	ns
THS-PREPARE + THS-ZERO	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 + 10*UI	-	-	ns
TD-TERM-EN	Time for the Data Lane receiver to enable the HS line termination.	-	-	35 + 4*UI	ns
THS-SETTLE	Time interval during which the HS receiver shall ignore any Data Lane HS transitions.	85 + 6*UI	-	145 + 10*UI	ns
THS-TRAIL	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	Max(n*8*UI, 60+n*4*UI)	-	-	ns
THS-EXIT	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

<Figure 6 Switching the Clock Lane between Clock Transmission and Low-Power Mode>

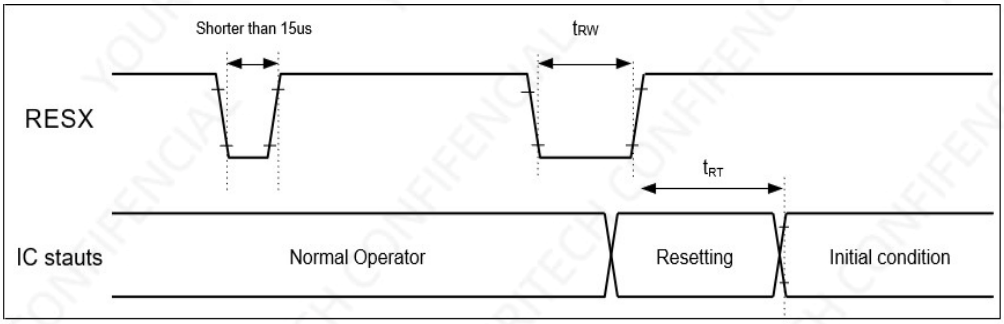


< Table 11. Switching the Clock Lane between Clock Transmission and Low-Power Specifications >

Parameter	Description	Min	Typ	Max	UNIT
TCLK-POST	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode.	60 + 52*UI	-	-	ns
TCLK-PRE	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8*UI	-	-	ns
TCLK-PREPARE	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38	-	95	ns
TCLK-PREPARE + TCLK-ZERO	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300	-	-	ns
TCLK-TERM-EN	Time for the Clock Lane receiver to enable the HS line termination.	-	-	38	ns
TCLK-TRAIL	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60	-	-	ns
THS-EXIT	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

4.4 Reset Timing:

< Figure 7 Reset input timings >



< Table 12. Reset input Specifications >

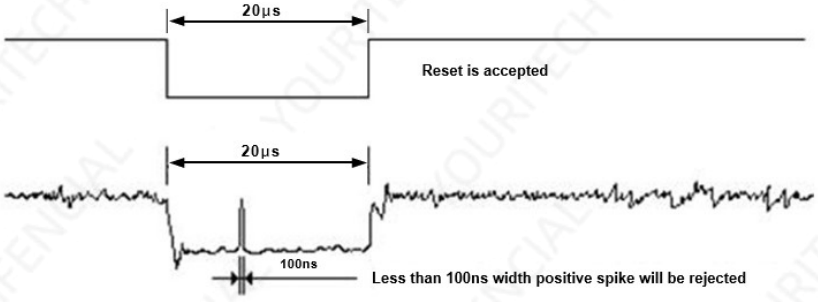
Symbol	Parameter	Related pins	Min.	Max.	Unit
tRW	Reset "L" pulse width(2)	RESX	20	-	μs
tRT	Reset complete time(3)	-	-	5(5)	ms
		-	-	120(6) (7) (8)	ms

Note:
1. The reset complete time also required time for loading ID bytes from OTP to registers. This loading is done every time when there is HW reset complete time (tRT) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 15 μs	Reset Rejected
Longer than 20 μs	Reset
Between 15 μs and 20 μs	Reset Start

3. During the resetting period, the display will be blanked (The display is entering blanking sequence, whic h maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for H/W reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:

< Figure 8 Reset timings >



1. When Reset is applied during Sleep In Mode.
2. When Reset is applied during Sleep Out Mode.
3. is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out comman d cannot be sent for 120msec.
4. After Sleep Out command, it is necessary to wait 120msec then send RESX.

5.0 POWER SEQUENCE

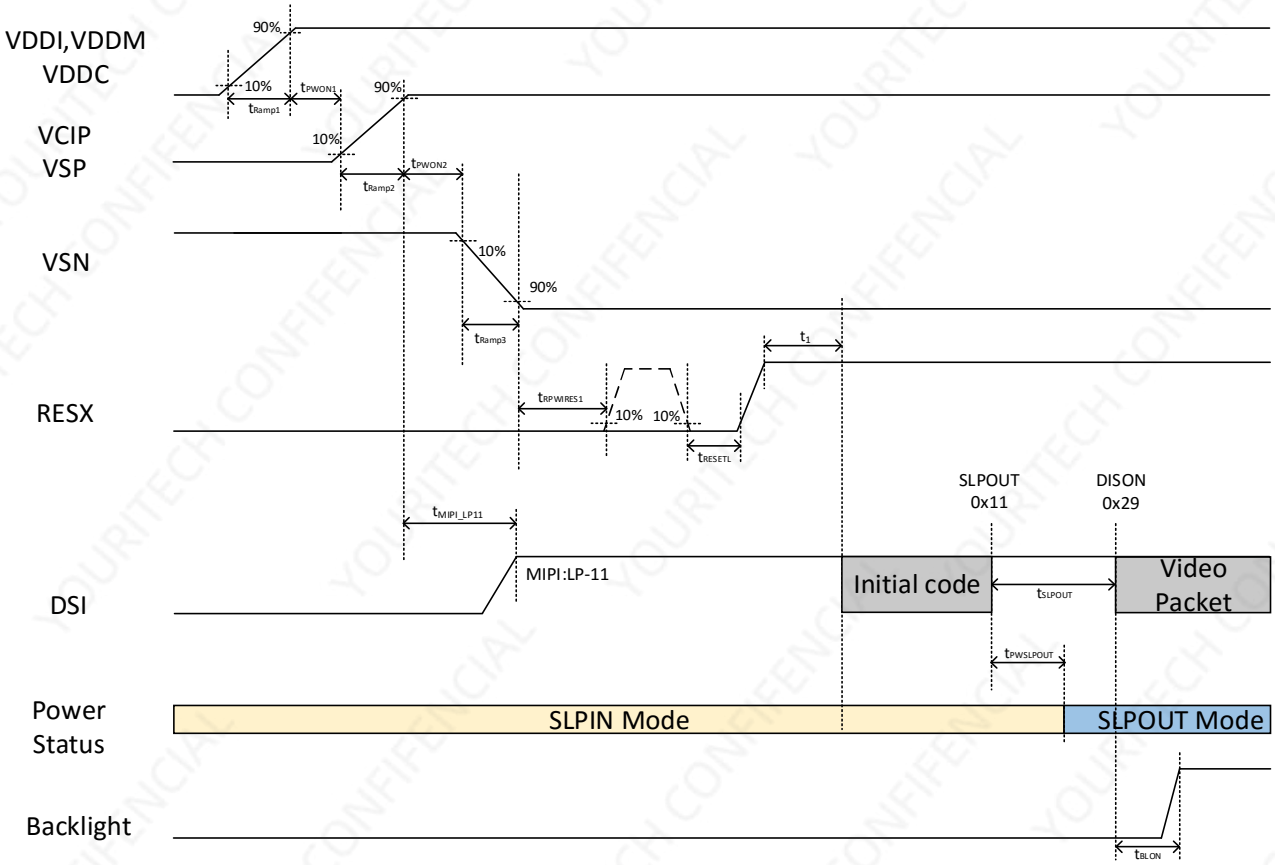
5.1 Power ON Sequence

The power on sequence timing for different power input modes and interfaces are shown as below table13

< Table 13. Power ON Sequence Specifications >

Symbol	Value			Unit	Remark
	Min	Typ	Max		
tPWON1	0	5	-	ms	
tPWON2	0	5	-	ms	
tPWON3	0	5		ms	
tPWON4	0	5		ms	
tramp1	0.2	-	20	ms	VDDI, VDDM
tramp2	0.2	-	20	ms	VCIP, VSP
tramp3	0.2	-	20	ms	VSN
tramp4	0.2	-	-	ms	VGL
tramp5	0.2	-	-	ms	VGH
tRPWIRES1	10	-	-	ms	
tRPWIRES2	1	-	-	ms	
tMIPI_LP11	-	-	tRPWIRES1	ms	
tRESETL	20	-	-	μs	
t_1	5	-	-	ms	
tSLPOUT	120	-	-	ms	
tPWSLPOUT	-	45	-	ms	
tBLON	2	-	-	VS	

< Figure 9 Power ON Sequence timings >



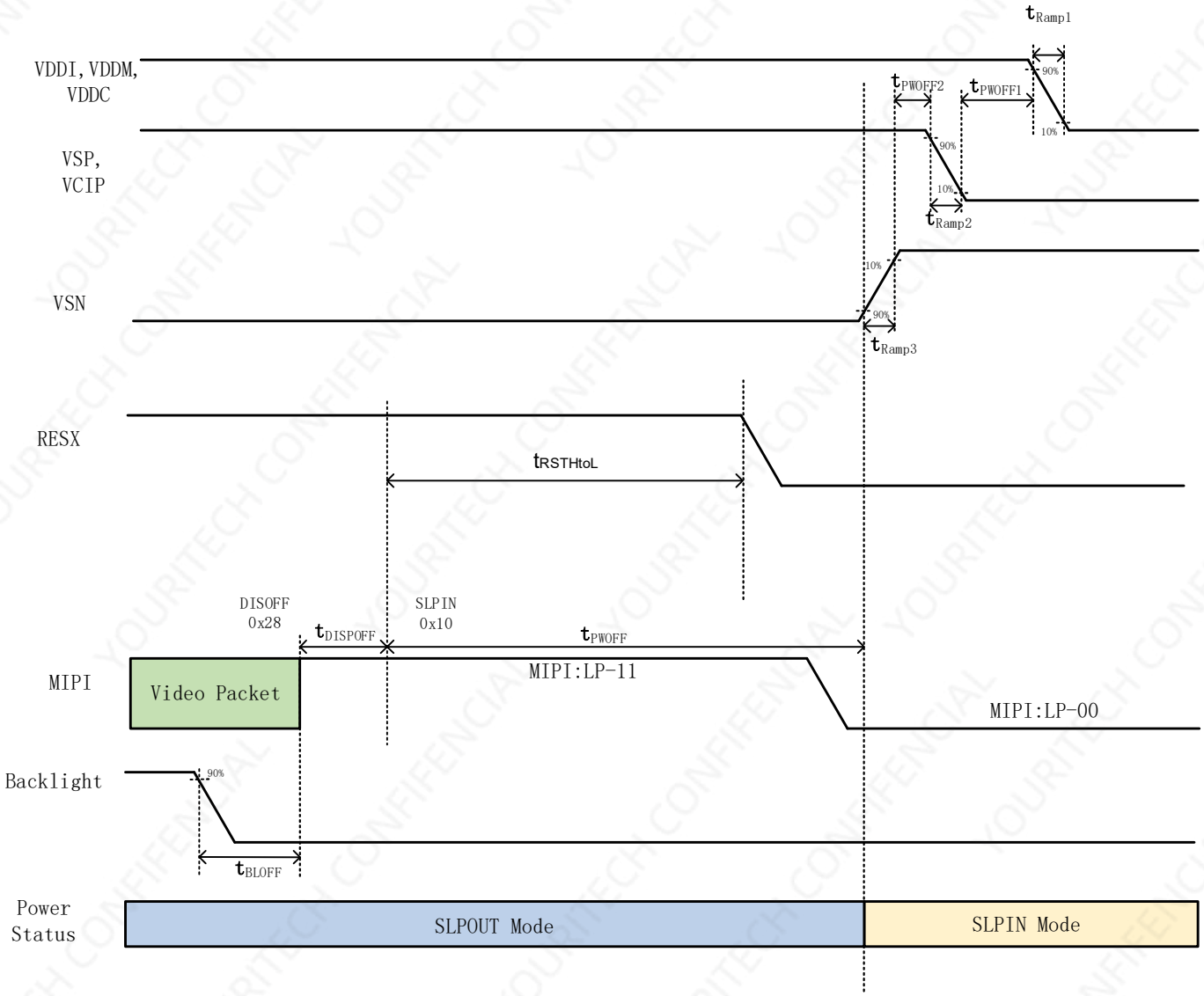
5.2 Power OFF Sequence

The power off sequence timing for different power input modes and interfaces are shown as below table.

< Table 14. Power OFF Sequence Specifications >

Symbol	Value			Unit	Remark
	Min	Typ	Max		
tPWOFF1	0	5	-	ms	
tPWOFF2	0	5	-	ms	
tPWOFF3	0	5	-	ms	
tPWOFF4	0	5	-	ms	
tramp1	0.2	-	20	ms	VDDI, VDDM, VDDC
tramp2	0.2	-	20	ms	VCIP, VSP
tramp3	0.2	-	20	ms	VSN
tramp4	0.2	-	-	ms	5Power: VGL
tramp5	0.2	-	-	ms	5Power: VGH
tPWOFF	120	-	-	ms	
tMIPI_LP11	0	-	tPWOFF	ms	
tDISPOFF	50	-	tPWOFF	ms	
tRSTHtoL	50	-	tPWOFF	ms	
tVideo_OFF	0	-	tPWOFF	ms	
tBLOFF	0	-	-	ms	

< Figure 10 Power OFF Sequence timings >



6.0 OPTICAL SPECIFICATIONS

6.1 Overview

The test of optical specifications shall be measured in a dark room (ambient luminance <1lux and temperature=25±2℃) with the equipment of luminance meter system (Goniometer system and CS2000/CA310) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and Φ equal to 0°. We refer to Ø=0 (=θ3) as the 3 o'clock direction (the "right"), Ø=90 (=θ12) as the 12 o'clock direction ("upward"), Ø=180 (=θ9) as the 9 o'clock direction ("left") and Ø=270(=θ6) as the 6 o'clock direction ("bottom"). While scanning θ and/or Ø, the center of the measuring spot on the Display surface shall stay fixed.

The backlight should be operating for 30 minutes prior to measurement.

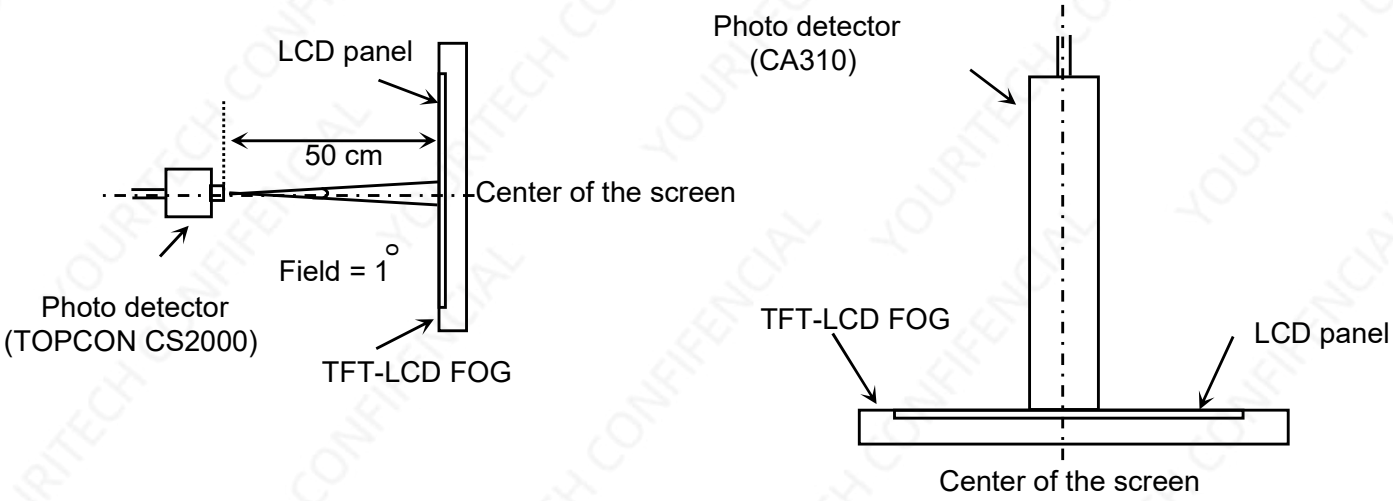
6.2 Optical Specifications

<Table 15. Optical Specifications> [Ta=25±2℃]

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle range	Horizontal	Θ_3	CR > 10	80	85	-	Deg.	Note6.1
		Θ_9		80	85	-	Deg.	
	Vertical	Θ_{12}		80	85	-	Deg.	
		Θ_6		80	85	-	Deg.	
Contrast ratio		CR	Θ = 0°	1000	1200	-	-	
LCM Luminance				1700	2000	-		nits
Color Gamut	NTSC	CIE1931	Θ = 0°	55	60	-	%	CF@C Light Note 6.4
Chroma@CIE 1931	Red	(Rx,Ry)	Θ = 0°	Typ - 0.03	(0.638,0.318)	Typ + 0.03	-	
	Green	(Gx,Gy)	Θ = 0°		(0.295,0.576)		-	
	Blue	(Bx,By)	Θ = 0°		(0.146,0.133)		-	
	White	(Wx,Wy)	Θ = 0°		(0.305,0.338)		-	
Response Time		Tr+Tf	Ta= 25° C Θ = 0°	-	30	35	ms	Note 6.5
Uniformity				70	75			75

Note 6.1: Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see Figure 11).

<Figure 11. Viewing Angle Range Is Defined As Follows>



View angel range, uniformity, etc. measurement setup

Flicker, measurement setup

Note 6.2: Contrast measurements shall be made at viewing angle of Θ=0° and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. Luminance Contrast Ratio (CR) is defined mathematically.

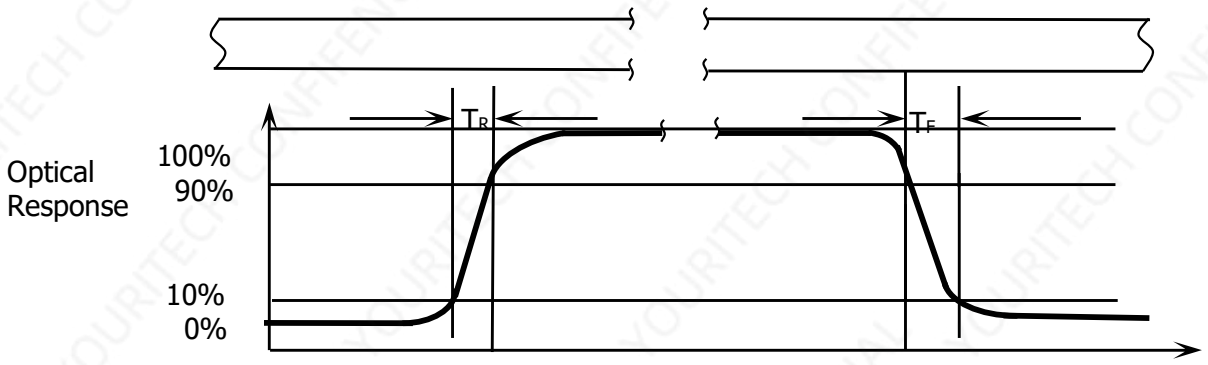
$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

Note 6.3: Transmittance is the Value with Polarizer(HC+Clear)&silicate BLU（Film structure is on Table16）.

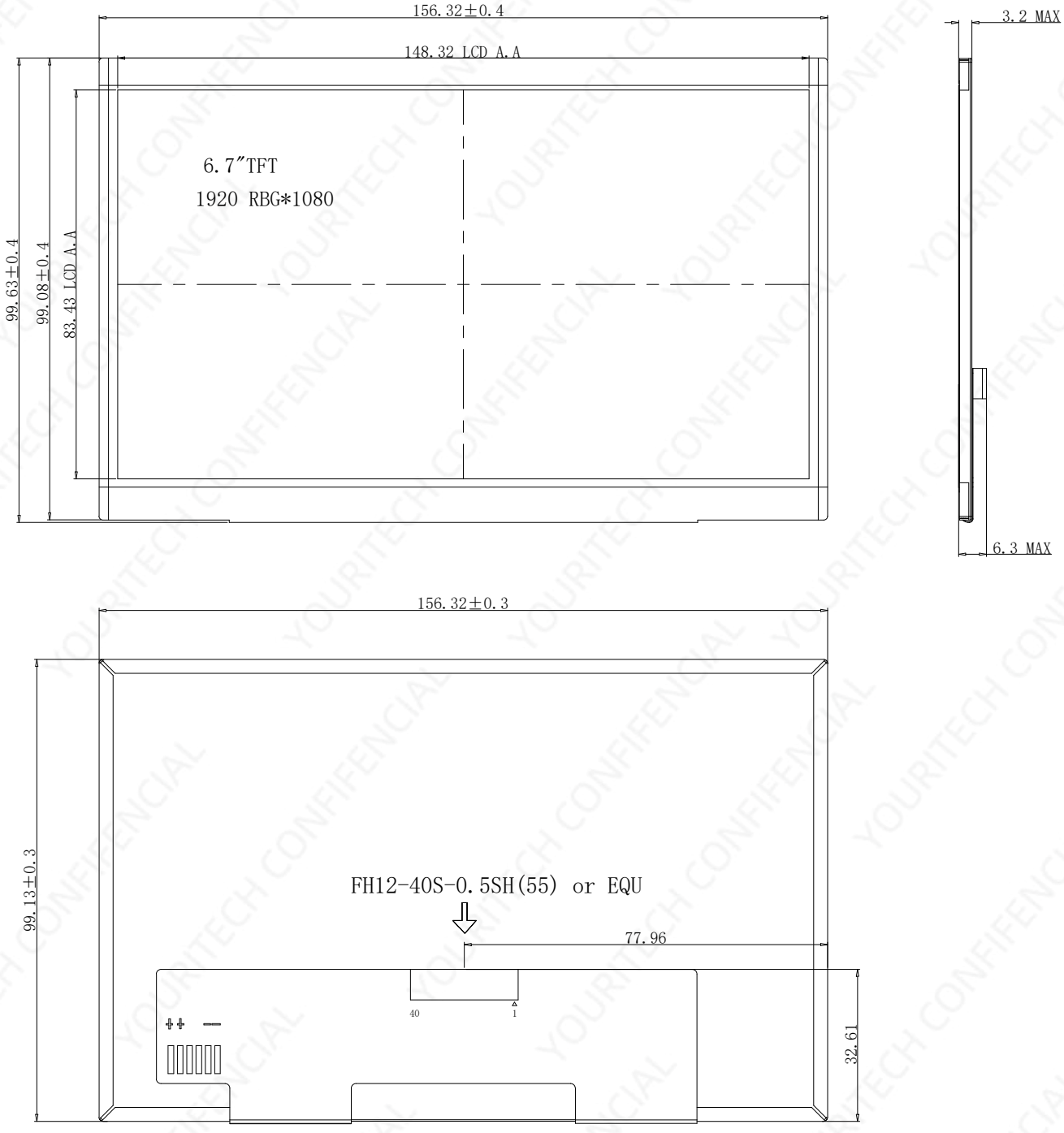
Note 6.4: The color chromaticity coordinates specified in Table 5 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

Note 6.5: The electro-optical response time measurements shall be made as Figure 12 by switching the “data” input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Tf.

<Figure 12. Response Time Testing>



7.0 Outline Drawing



8.0 Reliability Test

<Table 17. Reliability Test Parameters>

No	Items	Conditions	Remark
1	High Temperature Storage test(HTS)	80℃, 240hrs, Non-operational	Note 7.1
2	Low Temperature Storage test(LTS)	-30℃, 240hrs, Non-operational	
3	High Temperature Operating test(HTO)	80℃, 240hrs, operational	
4	Low Temperature Operating test(LTO)	-30℃, 240hrs, operational	
5	Thermal Humidity Operating test(THO)	60℃/90%RH, 240hrs, operational	
6	Thermal Cycle Storage test(TST)	-30~80℃, 100cycles, 1hr/cycle, Non-operational	
7	Image Sticking	5*5 Pattern, 1hr 25℃±2℃ check pattern Gray 127, after 3 min, the mura must be disap peared completely	

Note 7.1:

①The test result shall be evaluated after the sample has been left at room temperature and humidity for 2 hours.

②The BOE reliability test is based on GH8323-i1 IC;

③Other ICs can only be used after the reliability test is passed.

④Suitable operating time: under 12 hours a day.（ Please contract BOE in advance for 7*24hrs or more than suggested Operating time ）Long-term lighting products recommended regular shutdown