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MODULE NO (模组型号): ET068BA01-GX

Product (产品名称): 6.86 寸模组

CUSTOMER (客户名称): _____

APPROVED BY CUSTOMER 客户签署栏	
Approved by 审核	Remark 备注

YOURITECH		
Prepared by 制作	Checked by 检查	Approved by 审核



(√) Preliminary specification
() Final specification

REV.	ECN NO.	DESCRIPTION OF CHANGES	DATE	PREPARED
P0	-	Initial Release	2023.08.08	ChauncyTan



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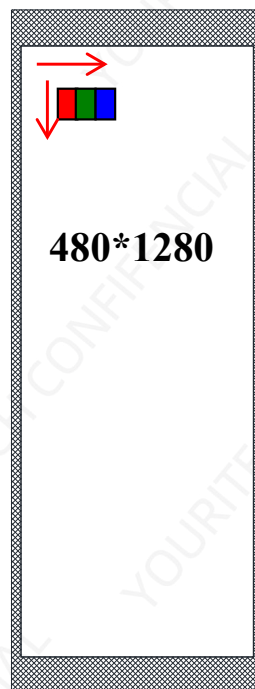
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1. GENERAL DESCRIPTION

1.1 Introduction

ET068BA01-GX is a color active matrix thin film transistor (TFT) 1-liquid crystal display (LCD) Sub Sheet that uses amorphous silicon TFT as a switching device. This TFT LCD panel (Single Chip) has a 6.8 inch diagonally measured active display area with WXGA resolution (480 horizontal by 1,280 vertical pixels array).



Sources IC

MIPI Connector

1.0.2 Features

- 8-bit color depth, display 16.7M colors
- Thin and light weight
- High luminance and contrast ratio, low reflection and wide viewing angle
- RoHS Compliant
- 7*24hrs usage support with dynamic video
- Landscape and Portrait usage support



1.3 Application

- Vehicle Rearview Mirror

1.4 General Specification

< Table 1. General Specifications >

Parameter	Specification	Unit	Remarks
Outline Dimension	66.60(H) x 181.00(V)x 7.15(B)	mm	
Active Area	60.02(H) x 160.59(V)	mm	
Number Of Pixels	480(H) RGB x 1280(V)	pixels	
Pixel Pitch	125.4(H) x 125.4(V)	μm	
Pixel Arrangement	RGB Vertical Stripe		
Display Mode	Normally Black		
Display Colors	16.7M	colors	
Center Luminous Intensity	300	Cd/m ²	
Viewing Angle(CR>10)	85:85:85:85 (typ.)		
Color Gamut	55% (typ.)		NSTC@C光
Interface	4-Lane MIPI		



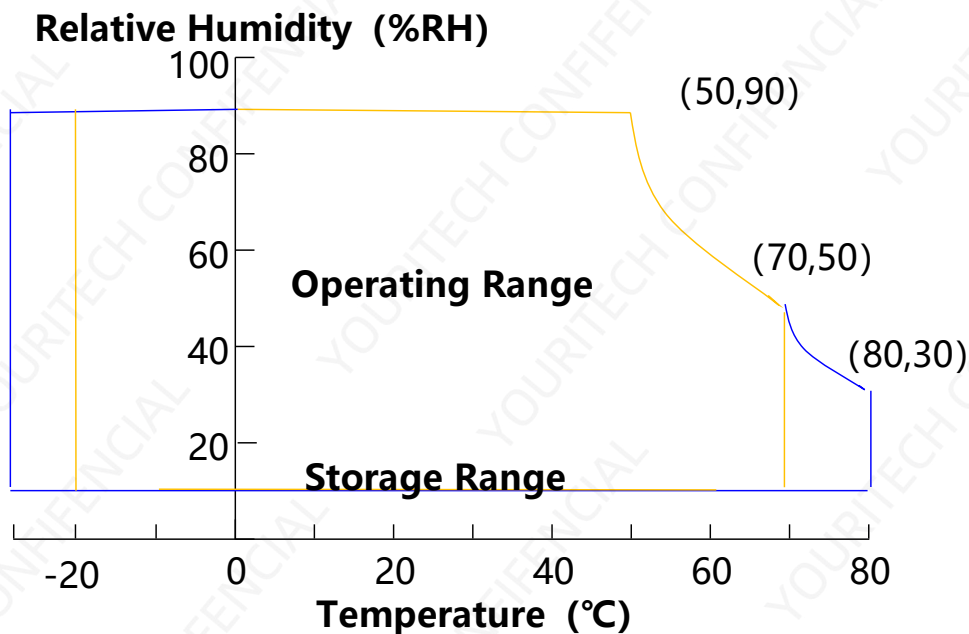
2. ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 2.

< Table 2. Environment Absolute Maximum Ratings> [Ta = 25 ± 2 °C]

Parameter	Symbol	Min.	Max.	Unit	Remark
Power Supply Voltage	VDD	3	3.6	V	Ta = 25 °C
Operating Temperature	T _{OP}	-20	+70	°C	Note 1
Storage Temperature	T _{ST}	-30	+80	°C	
Operating Ambient Humidity	Hop	10	90	%RH	
Storage Humidity	Hst	10	90	%RH	

Note : 1) Temperature and relative humidity range are shown in the figure below.
Wet bulb temperature should be 39 °C max. and no condensation of water.
T_{SUR} : Panel surface Temperature is measured at 50°C Dry Condition



3. ELECTRICAL SPECIFICATIONS

3.1 TFT LCD Module

< Table 3. Open Cell Electrical Specifications >

[Ta =25±2 °C]

Parameter	Symbol	Values			Unit	Notes
		Min.	Typ.	Max.		
Power Supply Voltage	VDD	3.0	3.3	3.6	V	Note 1
Power Supply Ripple Voltage	VRP	-	-	100	mV	
Power Supply Current	IDD	-	30	-	mA	
Analog Operating voltage	VGH	15	15	26	V	
Analog Operating voltage	VGL	-11.5	-5	-4	V	
Analog Operating voltage	VCOM	7.4	7.5	7.6	V	

- Notes : 1. The supply voltage is measured and specified at the interface connector of LCM.
The current draw and power consumption specified is for VBAT=3.2V, Frame rate $f_v=60\text{Hz}$ and Clock frequency = 50MHz. Test Pattern of power supply current
a) Typ : Mosaic 6 x 8 Pattern(L0/L255) b) Max : White

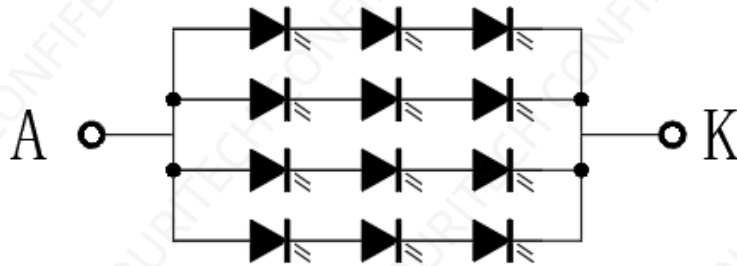


3.2 LED driver

< Table 4. LED Driving guideline specifications >

Ta=25+/-2°C

Parameter	Symbol	Values			Unit	Notes
		Min.	Typ.	Max.		
BLU Supply Voltage	Vled		9.3		V	
BLU Supply Current	Iled		120		mA	
Number of LED	-	12			Piece	



4. INTERFACE CONNECTION

4.1 Interface Input Signal & Power

< Table5. Pin Assignment for **open cell** Connector >

Pin No	Symbol	Description	Pin No	Symbol	Description
1	GND	Ground	21	NC	No Connect
2	D0P	MIPI data input	22	NC	No Connect
3	D0N	MIPI data input	23	NC	No Connect
4	GND	Ground	24	RESET	RESET pin
5	D1P	MIPI data input	25	STBYB	Select standby mode
6	D1N	MIPI data input	26	NC	No Connect
7	GND	Ground	27	GND	Ground
8	CLKP	MIPI clock input	28	LEDK	LED Negative
9	CLKN	MIPI clock input	29	LEDK	LED Negative
10	GND	Ground	30	GND	Ground
11	D2P	MIPI data input	31	NC	No Connect
12	D2N	MIPI data input	32	GND	Ground
13	GND	Ground	33	GND	Ground
14	D3P	MIPI data input	34	NC	No Connect
15	D3N	MIPI data input	35	LEDA	LED Positive
16	GND	Ground	36	LEDA	LED Positive
17	GND	Ground	37	GND	Ground
18	IOVCC	Power supply for digital circuits +1.8V input	38	VCC	Power supply for digital circuits +3.3V input
19	IOVCC	Power supply for digital circuits +1.8V input	39	VCC	Power supply for digital circuits +3.3V input
20	NC	No Connect	40	NC	No Connect



5. Interface timing Parameter

5.1 MIPI AC Characteristics

High Speed Mode

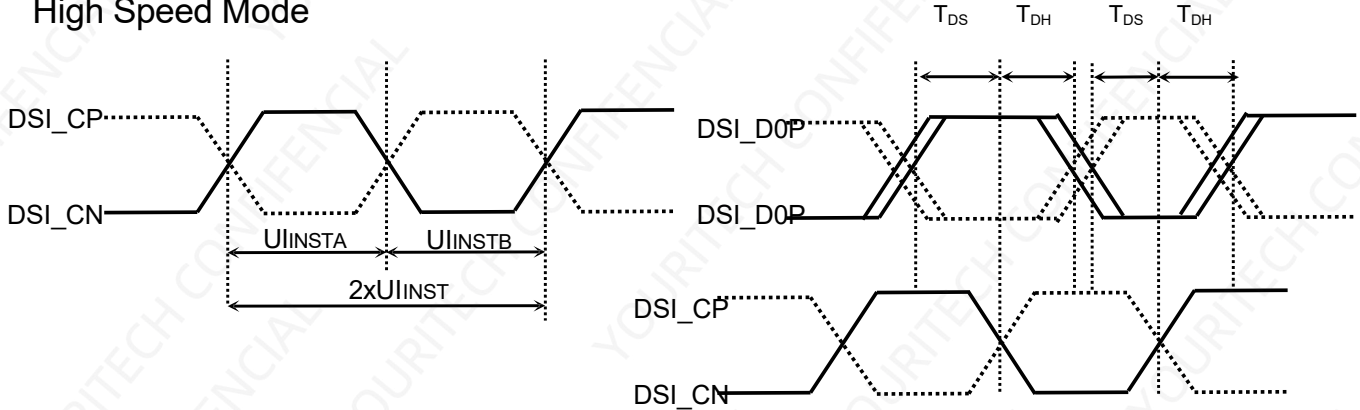


Figure 5-1: DSI clock timing Characteristics

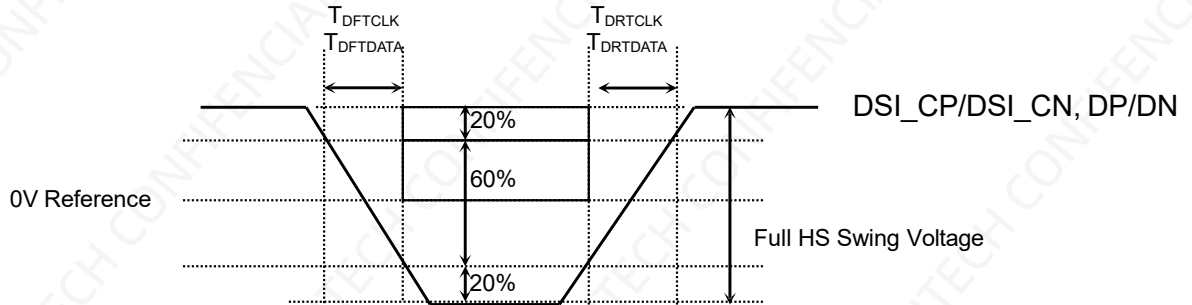


Figure 5-2: Rising and falling time on clock and data channel

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, $T_A = -30$ to 70°C)

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Double UI instantaneous	$2xU_{INST}$	4LANE : 3.30 3LANE : 2.85 @ VDDD=1.8V	-	25	ns
	UI instantaneous	U_{INSTA} U_{INSTB}	4LANE : 1.67 3LANE : 1.43 @ VDDD=1.8V	-	12.5	ns
DP/DN	Data to clock setup time	T_{DS}	$0.15xUI$	-	-	ps
	Data to clock hold time	T_{DH}	$0.15xUI$	-	-	ps
DSI_CP/ DSI_CN	Differential rise time for clock	T_{DRTCLK}	150	-	$0.3UI$	ps
	Differential fall time for clock	T_{DFTCLK}	150	-	$0.3UI$	ps
DP/DN	Differential rise time for data	$T_{DRTDATA}$	150	-	$0.3UI$	ps
	Differential fall time for data	$T_{DFTDATA}$	150	-	$0.3UI$	ps

Table 7-3: DSI High Speed Mode Characteristics



5. Interface timing Parameter

Low Power Mode

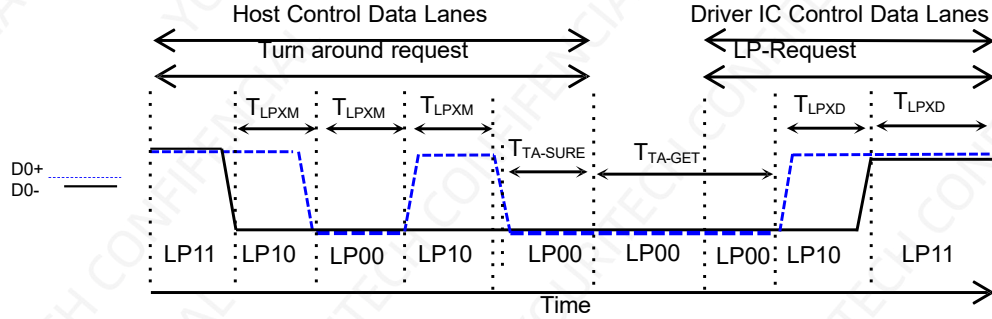


Figure 5-3: BTA from HOST to Display Module Timing

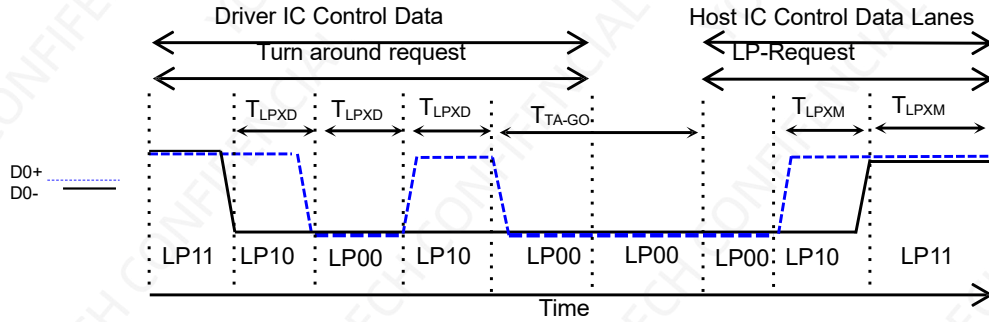


Figure 5-4: BTA from Display Module Timing to HOST

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V, $T_A = -30$ to 70°C)

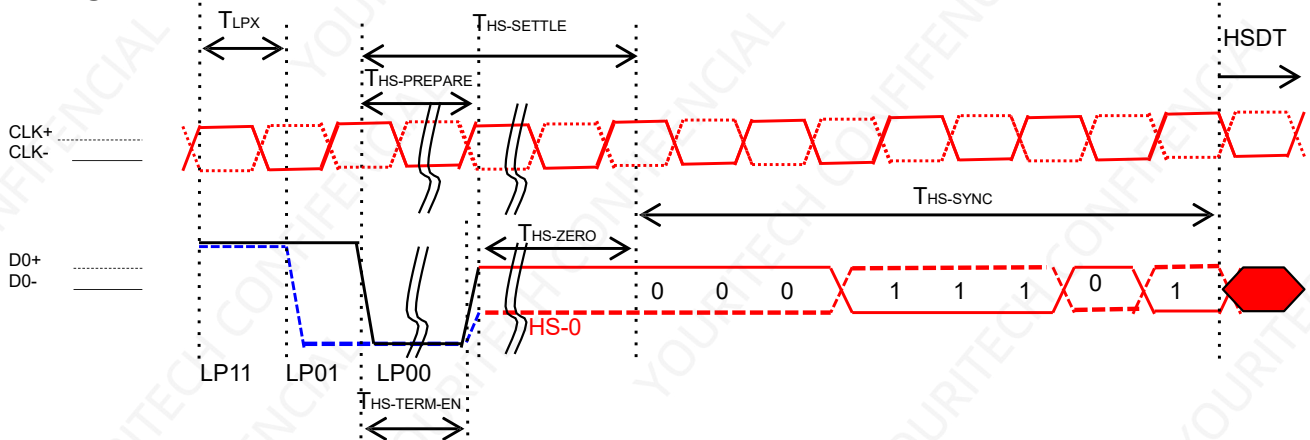
Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11 Host → Display module	T_{LPXM}	50	-	-	ns
	Length of LP-00/LP01/LP10/LP11 Display module → Host	T_{LPXD}	50	-	-	ns
	Time-out before the MPU start driver	$T_{TA-SURE}$	T_{LPXD}	-	$2 \times T_{LPXD}$	ns
	Time to drive LP-00 by display module	T_{TA-GET}	$5 \times T_{LPXD}$	-	-	ns
	Time to drive LP-00 after turnaround request Host	T_{TAGO}	$4 \times T_{LPXD}$	-	-	ns

Table 5-5: DSI Low Power Mode Characteristics



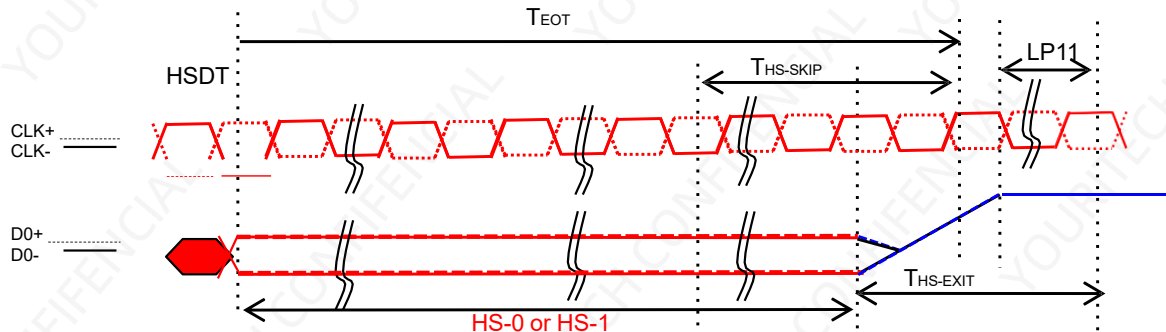
5. Interface timing Parameter

DSI BURSTS



Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11	T _{LPX}	50	-	-	ns
	Time to Driver LP-00 to prepare for HS transmission	T _{HS-PREPARE}	40+4UI	-	85+6UI	ns
	Time to enable data receiver line termination	T _{HS-TERM-EN}	-	-	35+4xUI	ns
	Time to drive LP-00 by display module	T _{TA-GET}	5xT _{LPXD}	-	-	ns
	Time to drive LP-00 after turnaround request Host	T _{TAGO}	4xT _{LPXD}	-	-	ns

Table 5-6: DSI Low Power Mode to High Speed Mode Timing



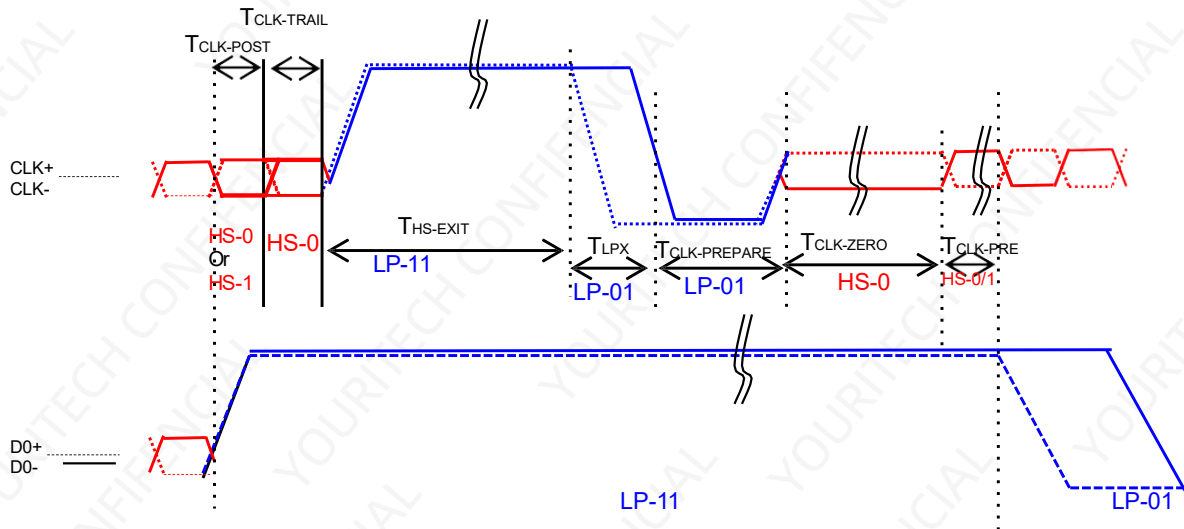
NOTE:
If the last bit is HS-0, the transmitter changes from HS-0 to HS-1
If the last bit is HS-0, the transmitter changes from HS-1 to HS-0

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Time-Out at Display Module to Ignore Transition Period of EoT	T _{HS-SKIP}	40	-	55+4xUI	ns
	Time to Driver LP-11 after HS Burst	T _{HS-EXIT}	100	-	-	ns

Table 5-7: DSI Low Power Mode to High Speed Mode Timing



5. Interface timing Parameter



Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Time that the MCU shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	T _{CLK-POST}	60+52xUI	-	-	ns
	Time to drive HS differential state after last payload clock bit of a HS transmission burst	T _{CLK-TRAIL}	60	-	-	ns
	Time to drive LP-11 after HS burst	T _{HS-EXIT}	100	-	-	ns
	Time to drive LP-00 to prepare for HS transmission	T _{CLK-PREPARE}	38	-	95	ns
	Time-out at Clock Lane Display Module to enable HS Termination	T _{CLK-TERM-EN}	-	-	38	ns
	Minimum lead HS-0 drive period before starting Clock	T _{CLK-PREPARE} + T _{CLK-ZERO}	300	-	-	ns
	Time that the HS clock shall be driven prior to any associated data Lane beginning the transition from LP to HS mode	T _{CLK-PRE}	8xUI			

Table 5-8: Clock Lanes High Speed Mode to/from Low Power Mode Timing



5. Interface timing Parameter

< Table 5. Timing Parameter >

Item			Symbol	min	typ	max	UNIT
LCD	Frame Rate		-	-	60	-	Hz
	Pixels Rate		-		50		MHz
Timing	Horizontal	Horizontal total time	tHP		630		t _{CLK}
		Horizontal Active time	tHadr	480			t _{CLK}
		Horizontal Pulse Width	tHsync		20		t _{CLK}
		Horizontal Back Porch	tHBP		80		t _{CLK}
		Horizontal Front Porch	tHFP		50		t _{CLK}
	Vertical	Vertical total time	tvp		1326		t _H
		Vertical Active time	tVadr	1280			t _H
		Vertical Pulse Width	tVsync		8		t _H
		Vertical Back Porch	tVBP		8		t _H
		Vertical Front Porch	tVFP		30		t _H
Lane				-	4	-	Lane



6. POWER SEQUENCE

Power On Timing of External Power IC

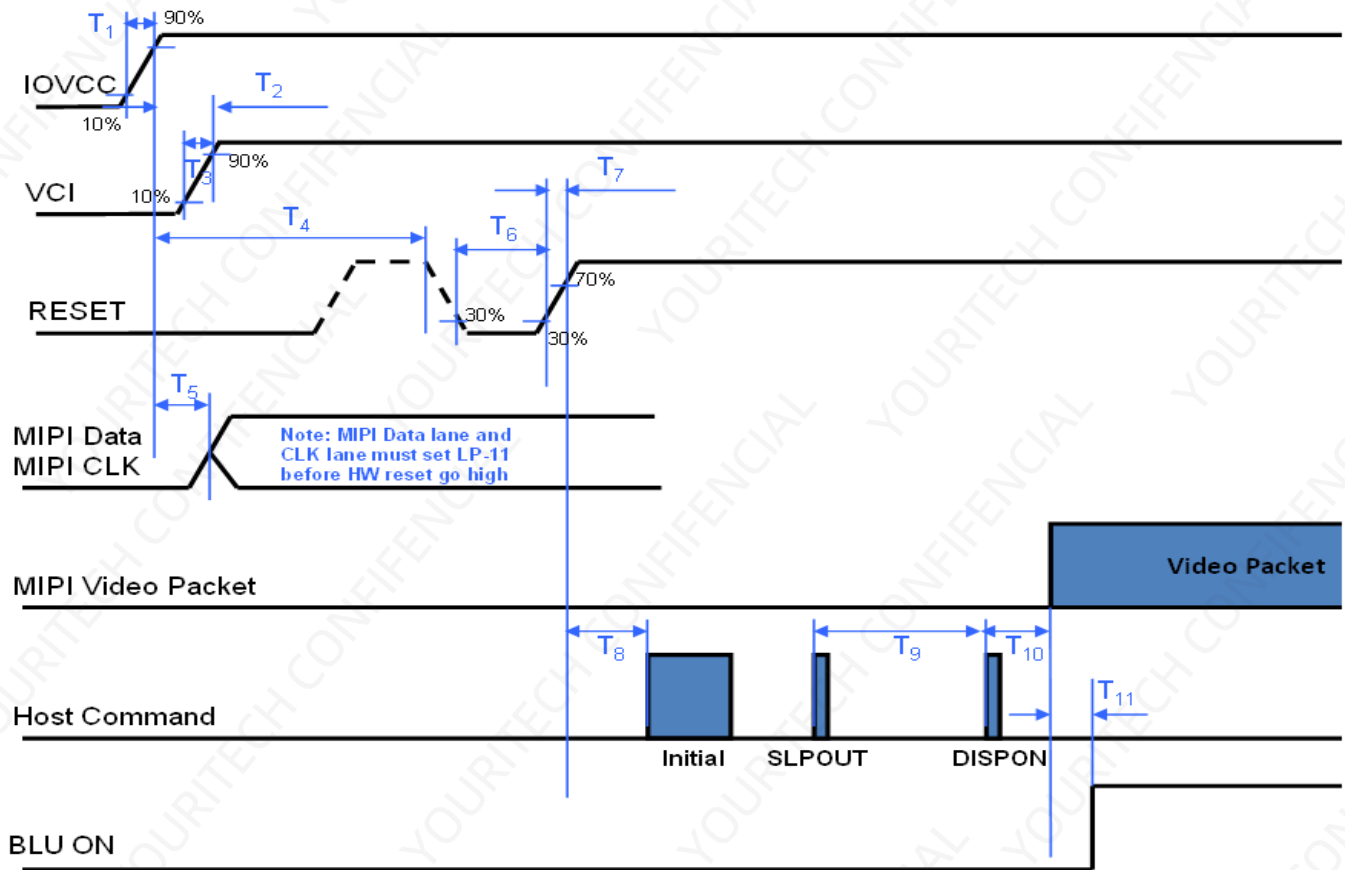


Figure 6-1: DSI Power On Sequence of Power IC Mode

	Min.	Typ.	Max.	Unit
T1	0.01	-	10	ms
T2	No Limit			ms
T3	0.01	-	10	ms
T4	1	-	-	ms
T5	1	-	-	ms
T6	10	-	-	us
T7	No Limit			ns
T8	15	-	-	ms
T9	120	-	-	ms
T10	No Limit			ms
T11	100	150	-	ms

Table 6-1: DSI Power On Timing of Power IC Mode



6. POWER SEQUENCE

Power Off Timing of External Power IC

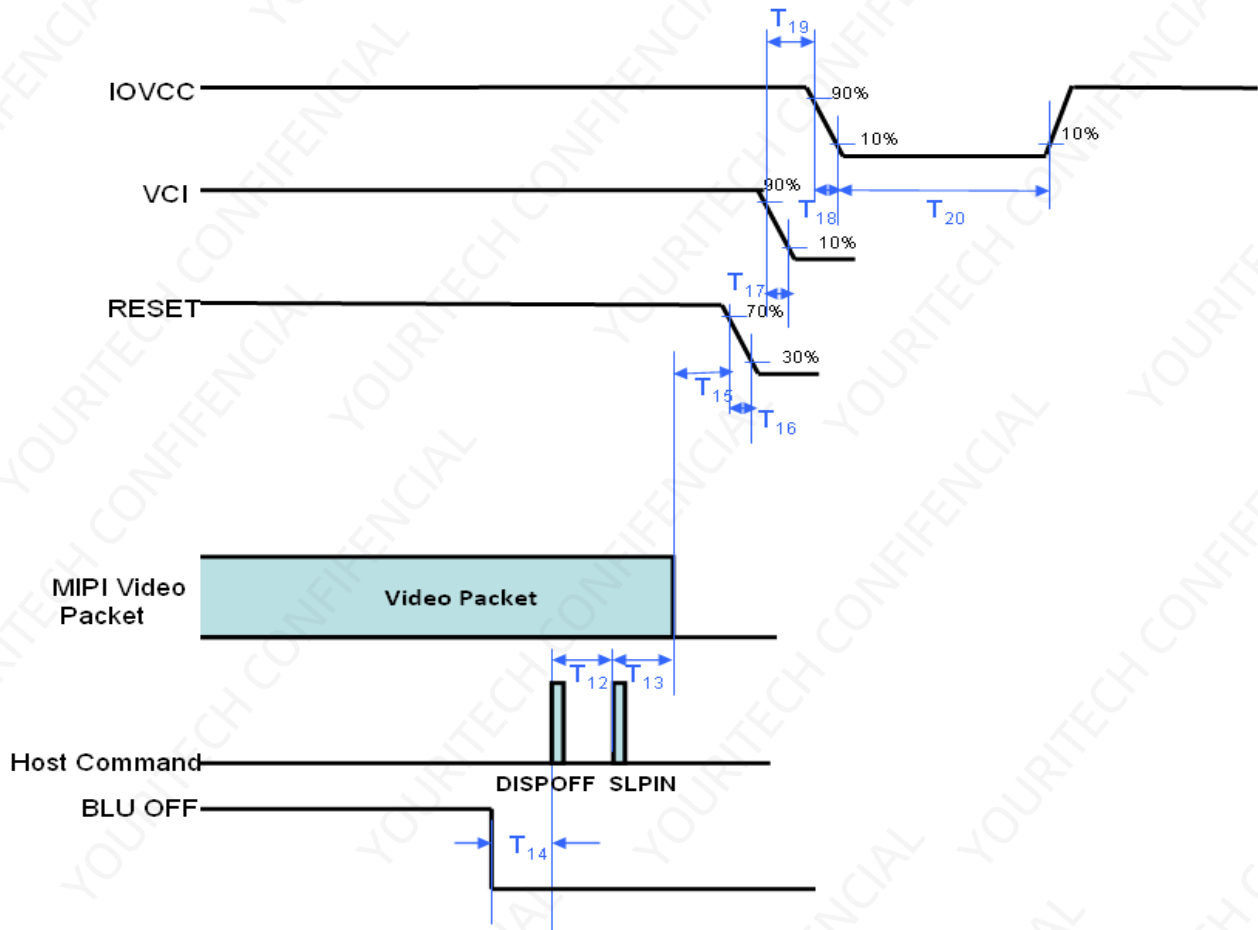


Figure 6-2: DSI Power Off Sequence of Power IC Mode

	Min.	Typ.	Max.	Unit
T12	2	-	-	Frame
T13	2	-	-	Frame
T14	40	100	-	ms
T15	10	-	-	ms
T16	No Limit			ms
T17	No Limit			ms
T18	No Limit			ms
T19	No Limit			ms
T20	100			ms

Table 6-2: DSI Power Off Timing of Power IC Mode



7. OPTICAL SPECIFICATION

7.1 Overview

The test of view angle range shall be measured in a dark room (ambient luminance $\leq 1\text{lux}$ and temperature = $25\pm 2^\circ\text{C}$) with the equipment of Luminance meter system (Goniometer system and TOPCON CS2000/CA310) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and Φ equal to 0° . We refer to $\theta\Phi=0$ ($=\theta_3$) as the 3 o'clock direction (the "right"), $\theta\Phi=90$ ($=\theta_{12}$) as the 12 o'clock direction ("upward"), $\theta\Phi=180$ ($=\theta_9$) as the 9 o'clock direction ("left") and $\theta\Phi=270$ ($=\theta_6$) as the 6 o'clock direction ("bottom"). While scanning θ and/or Φ , the center of the measuring spot on the Display surface shall stay fixed. The luminance, color and uniformity (etc) should be tested by CS2000/CA310. The backlight should be operating for 10 minutes prior to measurement. VDD shall be $3.3 \pm 0.3\text{V}$ at 25°C . Optimum viewing angle direction is 6 'clock

<Table 7. Optical Specifications>

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle Range	Horizontal	Θ_3	CR > 10	80	85	-	Deg.	
		Θ_9		80	85	-	Deg.	
	Vertical	Θ_{12}		80	85	-	Deg.	
		Θ_6		80	85	-	Deg.	
Contrast Ratio		CR	$\Theta = 0^\circ$	800	900	-		
Center Luminous Intensity				350	300		cd/m ²	
Reproduction of color		Rx	$\Theta = 0^\circ$	Typ. +0.03	(0.631)	Typ. +0.03		
		Ry			(0.318)			
		Gx			(0.29)			
		Gy			(0.543)			
		Bx			(0.143)			
		By			(0.129)			
		Wx			(0.305)			
		Wy			(0.330)			
Color Gamut			$\Theta = 0^\circ$	50	55	-	%	
Response Time	Tr	Ta= 25°C $\Theta = 0^\circ$	-	30	35	ms		
	Tf		-			ms		
	Tgray		-	-	-	ms		



- Notes :
1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see FIGURE 1).
 2. Contrast measurements shall be made at viewing angle of $\Theta = 0$ and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state . (see FIGURE 2)
 - 2) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. The color chromaticity coordinates specified in Table 5. shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.
4. The electro-optical response time measurements shall be made as FIGURE 2 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is T_r , and 90% to 10% is T_d .



7.2 Optical measurements

Figure 1: The definition of Viewing Angle

Refer to the graph below marked by θ and ϕ .

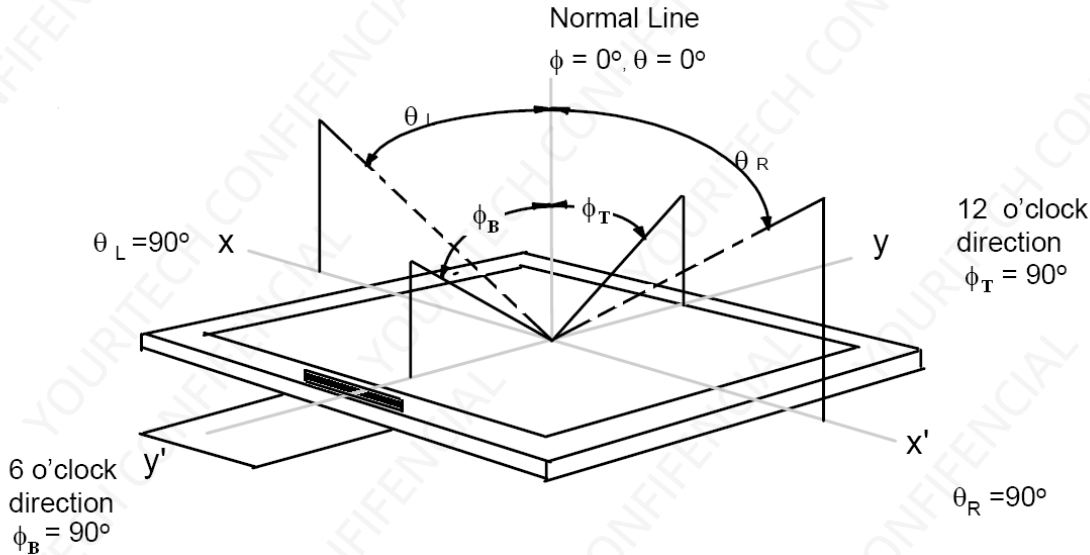
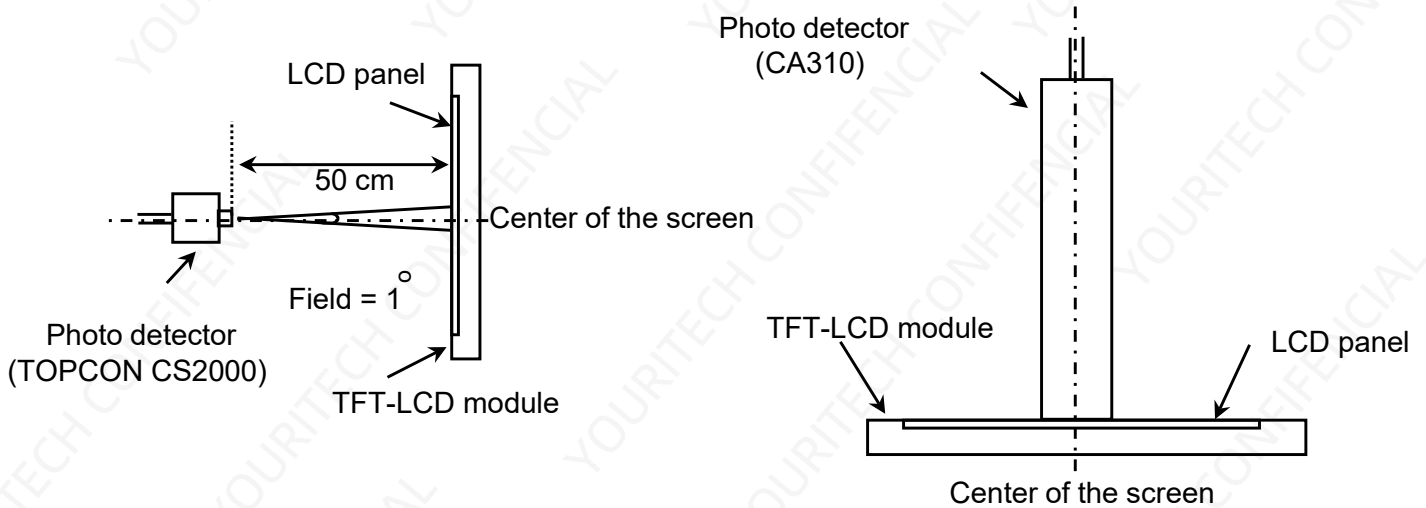


Figure 2. Measurement Set Up

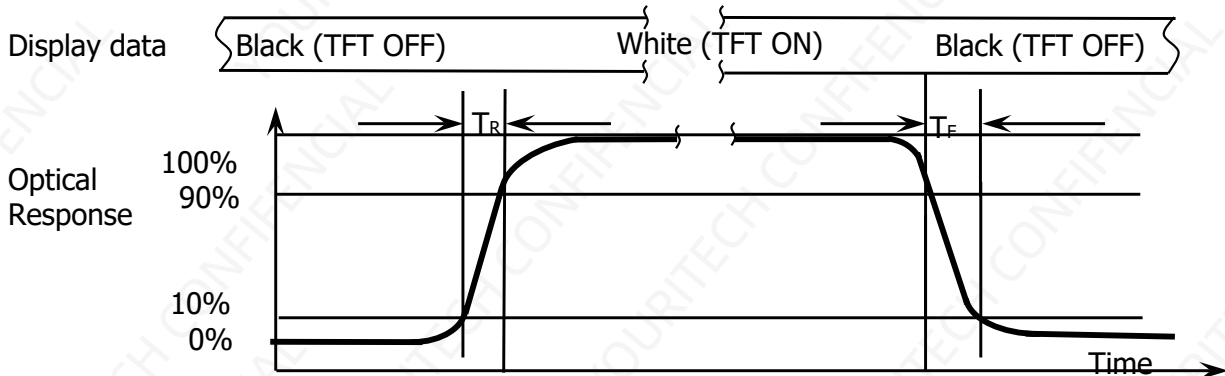


View angel range, uniformity, etc. measurement setup

Flicker, measurement setup



Figure 3. Response Time Testing



The electro-optical response time measurements shall be made as shown in FIGURE 3 by switching the “data” input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is T_r and 90% to 10% is T_d .

Response time of gray to gray:

Response time T_g is the average time required for display transition by switching the input signal as below table and is based on Frame rate $f_v = 60\text{Hz}$ to optimize. Each time in below table is defined as Figure 2 and shall be measured by switching the signals for “any level of gray (bright) ” and any level of gray (dark)

Measured Response Time		Target																
		0	15	31	47	63	79	95	111	127	143	159	175	191	207	223	239	255
Start	0																	
	15																	
	31																	
	47																	
	63																	
	79																	
	95																	
	111																	
	127																	
	143																	
	159																	
	175																	
	191																	
	207																	
	223																	
	239																	
255																		



Figure 4:

Viewing direction is normal user viewing direction which is vertical to the display surface

- The polarizer which is closer to viewer is defined as Front Polarizer
- The polarizer which is on the rear side of viewer is defined as Rear Polarizer
- The X axis is defined as parallel line to top & bottom sidelines of the Active Area
- PdF which is marked in blue arrow is polarization degree of Front polarizer
- PdR which is marked in red arrow is polarization degree of Back polarizer
- The polarization degree parameter must be indicated in range of 0deg to 180deg according to above definition

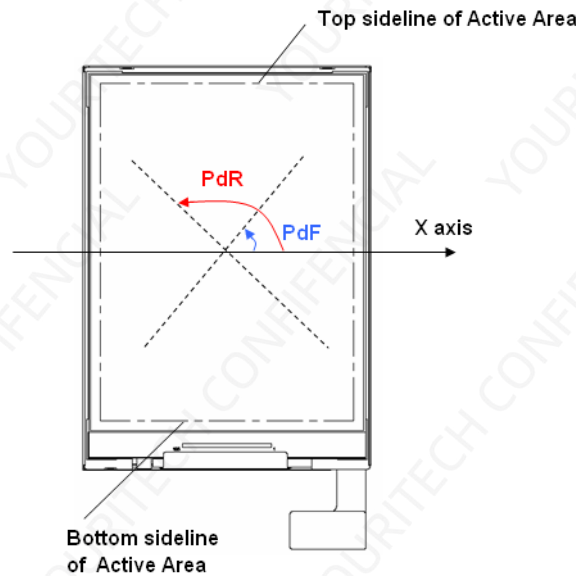
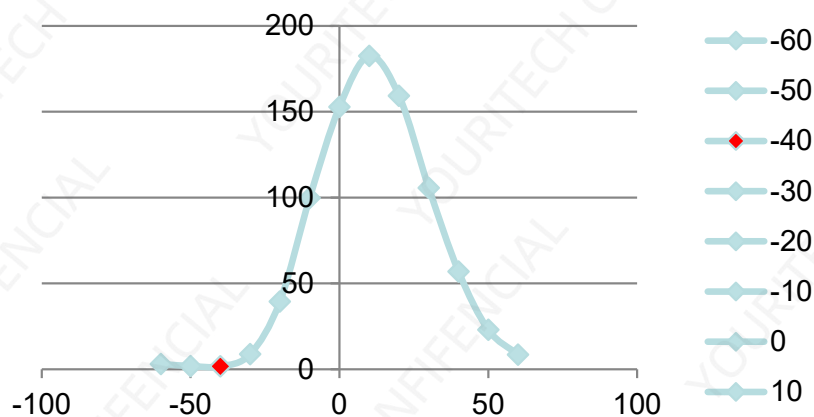


Figure.5:

Using luminance test method.

- Test pattern : 128 gray
- If the viewing direction is 12 o' clock ,then test the luminance while $\theta = -60^\circ, \theta = -50^\circ, \theta = -40^\circ, \theta = -30^\circ, \theta = -20^\circ, \theta = -10^\circ, \theta = 0^\circ, \theta = 10^\circ, \theta = 20^\circ, \theta = 30^\circ, \theta = 40^\circ, \theta = 50^\circ, \theta = 60^\circ$. The luminance test as figure below:



8. MECHANICAL CHARACTERISTICS

8.1 Dimensional Requirements

As shown in Table 8.

< Table 8 Dimensional Parameters >

Parameter	Specification	Unit
Dimensional outline	60.02(H) x 160.59(V)	mm
Active area	480(H) RGB x 1280(V)	mm
Pixel pitch	125.4(H) x 125.4(V)	μm
Number of pixels	480(H) RGB x 1280(V) 1 pixel = R + G + B dots)	pixels



9. RELIABILITY TEST

The Reliability test items and its conditions are shown in below.

<Table 9. Reliability test>

No	Test Items	Conditions
1	High temperature storage test	Ta = 80°C, 72 hrs
2	Low temperature storage test	Ta = -30 °C, 72 hrs
3	High temperature operation test	Ta = 70°C, 72 hrs
4	Low temperature operation test	Ta = -20 °C, 72 hrs
5	High temperature & high humidity operation test	Ta = 60 °C, 90%RH, 72 hrs
6	Thermal shock	Ta = -30 °C ↔ 80°C (0.5 hr), 50 cycle

Note : After the reliability test, the product only guarantee function normally without any fatal defect (non-display, line defect, abnormal display etc). All the cosmetic specification is judged before the reliability test.



10. Handling & Cautions

Please pay attention to the followings when you use this TFT LCD open cell (OC) .

10.1 Mounting Precautions

- Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
- You must mount an OC using specified mounting holes (Details refer to the drawings).
- You should consider the mounting structure so that uneven force (ex. Twisted stress, Concentrated stress) is not applied to the OC. And the case on which an OC is mounted should have sufficient strength so that external force is not transmitted directly to the OC.
- Do not apply mechanical stress or static pressure on OC; Abnormal display cause by pressing some parts of OC during assembly process, do not belong to product failure, the press should be agreed by two sides.
- Determine the optimum mounting angle, refer to the viewing angle range in the specification for each model.
- Do not apply mechanical stress or static pressure on OC, and avoid impact, vibration and falling.
- Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
- Protection film for polarizer on the OC should be slowly peeled off before display.
- Be careful to prevent water & chemicals contact the OC surface.
- You should adopt radiation structure to satisfy the temperature specification.
- Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment.

Do not touch the surface of polarizer for bare hand or greasy cloth.(Some cosmetics are detrimental to the polarizer.)



- When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzine. Normal-hexane & alcohol is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene , because they cause chemical damage to the polarizer.
- Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
- This OC has its circuitry PCBs on the front or rear side and Driver IC, should be handled carefully in order not to be stressed.
- Avoid impose stress on PCB and Driver IC during assembly process ,Do not drawing, bending, COF package & wire.
- Do not disassemble the OC.

10.2 Operating Precautions

- Do not connect or disconnect the cable to/from the OC at the "Power On" Condition.
- When the OC is operating, do not lose CLK, ENAB signals. If any one of these signals is lost, the OC would be damaged.
- Obey the supply voltage sequence. If wrong sequence is applied, the OC would be damaged.
- Do not allow to adjust the adjustable resistance or switch.
- The electrochemical reaction caused by DC voltage will lead to LCD open cell degradation, so DC drive should be avoided.
- The LCD panel use C-MOS LSI drivers, so customers are recommended that any unused input terminal would be connected to Vdd or Vss, do not input any signals before power is turn on, and ground you body, work/assembly area, assembly equipment to protect against static electricity.
- Do not exceed the absolute maximum rating value. (supply voltage variation, input voltage variation, variation in part contents and environmental temperature, and so on) Otherwise the OC may be damaged.
- OC has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference.



