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MODEL NO : ET068BA03-T

MODEL VERSION: 01

SPEC VERSION : 1.0

ISSUED DATE: 2022-05-09

□Preliminary Specification

■Final Product Specification

Customer :_____

Approved by	Notes

Youri Confirmation

Prepared by	Reviewed by	Approved by
John	Johnny	Wang

1. Introduction

1.1 Scope of application

LCD specification: Dots 480xRGBx1280
As to basic specification of the driver IC, refer to the IC (ICNL9707) specification and data book.
All material & processing of the LCD module should be Lead Free.

1.2 TFT features:

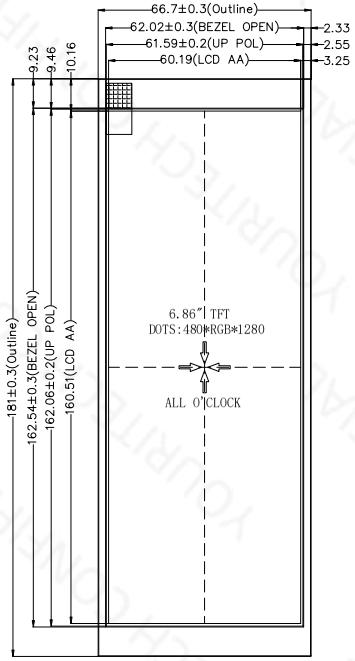
Structure: TFT PANNEL+IC +FPC+BL;
ALL Viewing Type LCD
480 dot-segment and 1280 dot-common outputs;
16.7M Color can be selected by software;
White LED back light;
4lane MIPI interface

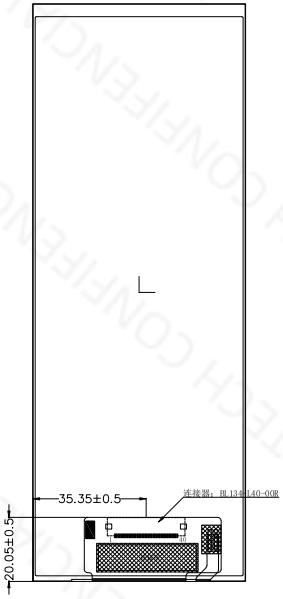
1.3 Applications:

2. LCM General specification

ITEM	Sandard value	Unit
LCD Type	Normally Black	--
Drive element	TFT active matrix	--
Number of pixels	480*3RGB(H)X1280(V)	Dots
Pixel arrangement	RGB Vertical Stripe	--
Pixel Pitch (W*H)	0.12546(H) X 0.12546(V)	mm
Active area	60.19(H) x 160.51(V)	mm
Viewing direction	ALL O'CLOCK	-
TFT Driver IC	ICNL9707	
TFT interface	4lane MIPI interface	-
Approx. Weight	TBD	g
LCM Size(W*H*T)	66.70(W) ×181.00(H) ×4.80(T)	mm
Touch structure	--	
Touch Driver IC	--	-
Touch Interface	--	

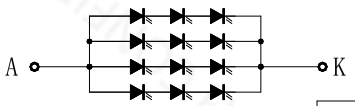
REV	DESCRIPTION	DRG DATE	DRAWN BY
	First Desing	2022.04.21	





PIN	DESCRIPTION
1	GND
2	D0P
3	D0N
4	GND
5	D1P
6	D1N
7	GND
8	CLKP
9	CLKN
10	GND
11	D2P
12	D2N
13	GND
14	D3P
15	D3N
16	GND
17	GND
18	IOVCC
19	IOVCC
20	NC
21	SDA-NC
22	SCL-NC
23	NC
24	RSTB
25	STBYB(NC)
26	NC
27	GND
28	K
29	K
30	GND
31	NC
32	GND
33	GND
34	NC
35	A
36	A
37	GND
38	VDD-3V3
39	VDD-3V3
40	NC

LED CIRCUIT DIAGRAM



NOTES:
1. DISPLAY TYPE: 6.86", 480*1280 TFT LCD
2. DISPLAY MODE: transmissive Normally Black
3. VIEWING DIRECTION: ALL
4. DRIVER IC:ICNL9707
5. LCM (White 9 AVG 1/9) :
   Brightness: 500cd/m² (MIN)、600cd/m² (TYP) 、700cd/m² (MAX)
   Uniformity:80%(MIN)
6. BACK LIGHT: 12 chip white LEDs If=180mA(MIN)、200mA(TYP)、240mA(MAX),Vf=8.4-9.6V
7. OPERATING TEMP: -20° C TO 70° C,STORAGE TEMP: -30° C TO 80° C
8. * Critical Parameter,( ) ref Parameter,[ ] cpk Parameter
   Unspecified Tolerances:±0.20mm
   Modification mark:
9. SUGGESTION:TP window size unilateral increase 0.3~0.5mm than LCM A.A
10. REQUIREMENTS ENVIRONMENTAL PROTECTION: RoHS

深圳市优瑞泰克科技有限公司

PART NO.:	ET068BA03-T	MODULE NO.:	00
DRAWN BY:	LIU	DATE:	PROJECTION:
CHECKED BY:		DATE:	SCALE:N.T.S UNIT: mm
APPROVED BY:		DATE:	SHEET: 1 OF 1

3.Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
LCM Operating Temperature	T_{OPR}	-20	+70	°C
LCM Storage Temperature	T_{STG}	-30	+80	°C
Humidity	RH	-	90	%

4.Electrical Characteristics

4.1 TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage for I/O	VDDIO	1.65	1.8	3.3	V
Supply Voltage for(DC/DC)	VDD	2.7	3.3	3.6	V
Current Consumption	I_{DD}	--	160	--	mA
	$I_{DD-SLEEP}$	--	100	--	uA

4.2 Back-Light Unit Characeristics

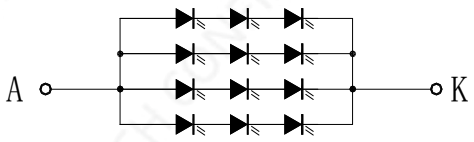
The back-light system is an edge-lighting type with 12 white LEDs. The characteristics of the back-light are shown in the following tables.

Characteristics	Symbol	Min.	Type	Max.	Unit	Notes
Forward Voltage	V_F	8.4	--	9.6	V	-
Forward current	I_F	180	200	240	mA	-
Luminance(With LCD)	Lv	500	600	700	cd/m^2	-
LED life time	N/A	----	30,000	--	Hr	Note 1

Note:

(1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=50mA/LED. The LED life time could be decreased if operating I_L is larger than 60mA/LED.

Backlight circuit diagram shown in below:



5. Module Function Description

Pin No.	Symbol	LCM Functional	Notes
1	GND	Power Ground	
2	D0P	MIPI-DSI Data differential signal input pins	
3	D0N	MIPI-DSI Data differential signal input pins	
4	GND	Power Ground	
5	D1P	MIPI-DSI Data differential signal input pins	
6	D1N	MIPI-DSI Data differential signal input pins	
7	GND	Power Ground	
8	CLKP	MIPI-DSI CLOCK differential signal input pins	
9	CLKN	MIPI-DSI CLOCK differential signal input pins	
10	GND	Power Ground	
11	D2P	MIPI-DSI Data differential signal input pins	
12	D2N	MIPI-DSI Data differential signal input pins	
13	GND	Power Ground	
14	D3P	MIPI-DSI Data differential signal input pins	
15	D3N	MIPI-DSI Data differential signal input pins	
16	GND	Power Ground	
17	GND	Power Ground	
18	IOVCC1.8V	power supply for the I/O circuit（1.65~3.3V）	
19	IOVCC1.8V	power supply for the I/O circuit（1.65~3.3V）	
20	NC	NC	
21	SDA/NC	NC	
22	SCL/NC	NC	
23	NC	NC	
24	RESET	Reset pin. Setting either pin low initializes the LSI	
25	STBYB/NC	NC	
26	NC	NC	
27	GND	Power Ground	
28	LEDK	Power supply for backlight cathode input terminal.	
29	LEDK	Power supply for backlight cathode input terminal.	
30	GND	Power Ground	
31	NC	NC	
32	GND	Power Ground	
33	GND	Power Ground	
34	NC	NC	
35	LEDA	Power supply for backlight anode input terminal.	
36	LEDA	Power supply for backlight anode input terminal.	
37	GND	Power Ground	
38	VDD3.3V	power supply for DC/DC circuit(2.7~3.6V)	
39	VDD3.3V	power supply for DC/DC circuit(2.7~3.6V)	
40	NC	NC	

6. Timing Characteristics

Power ON Sequence

Hardware Reset would be applied when power on. The RESX is held at "H" by the host after both VCI and IOVCC have been applied. Otherwise, correct functionality will not be guaranteed. If RESX is held to "L" by the host during Power On, it must keep "L" at least 10μsec after both VCI and IOVCC applied. The power on sequence for different power input modes are shown below.

Table 1 Power ON Sequence Timing

Symbol	Description	Value			Unit	Remark
		Min.	Typ.	Max.		
T_{on1}	Delay time of IOVCC to VCI	0			ms	
T_{on2}	Delay time of IOVCC to VSP	0			ms	
T1	IOVCC rising time	-		2	ms	
T2	Delay time of IOVCC to valid RESX to "H"	10			ms	
T3	Delay time of RESX "H" to initial code ready	20			ms	
T4	Delay time of IOVCC (HS_VCC) to MIPI bus ready	0		T2	ms	
T5	RESX "L" period	10			us	
T6	Delay time of initial code reloaded to video packet transmit	120			ms	

Power on sequence: PCCS [1:0] = [1,0]

Applied Power: IOVCC, VCI

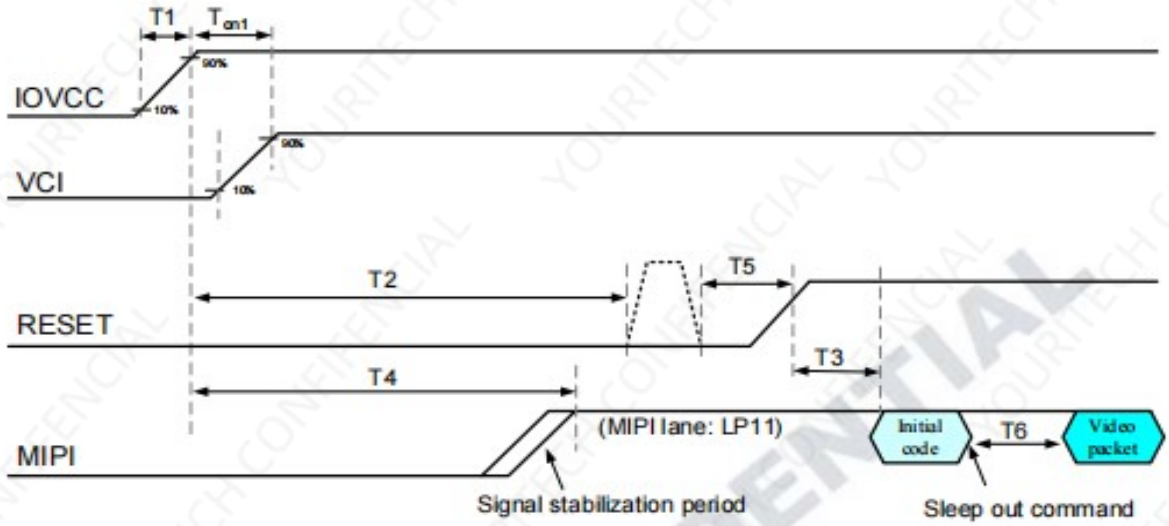


Figure 1 Power on sequence at PCCS[1:0]=[1,0] mode

Note1: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

Power OFF Sequence

Power off sequence for different PCCS-mode applications are shown below:

Table 2 Power OFF Sequence Timing

Symbol	Description	Value			Unit	Remark
		Min.	Typ.	Max.		
T_{off1}	Delay time of VCI to IOVCC	0	-	-	ms	
T_{off2}	Delay time of VSP to IOVCC	0	-	-	ms	
T_{off3}	Delay time of VSN to VSP	0	-	-	ms	
T7	IOVCC falling time	-	-	2	ms	
T8	Delay time of RESX "L" to VCI	0	-	-	us	
T9	Delay time of MIPI LP-00 to valid RESX "L"	0	-	-	us	
T10	Delay time of Sleep-in received to valid RESX "L"	100	-	-	ms	
T11	Delay time of RESX "L" to VSN	0	-	-	ms	

MIPI AC Characteristics

High Speed Mode - Clock Timings

Figure 4-5 Clock Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
CLK P/N	2xUIINST	Double UI instantaneous	4		18.2	nS	
CLK P/N	UIINSTA, UIINSTB	UI instantaneous Half	2		9.1	nS	1

Note 1: UI = UIINSTA = UIINSTB

High Speed Mode - Clock / Data Timings

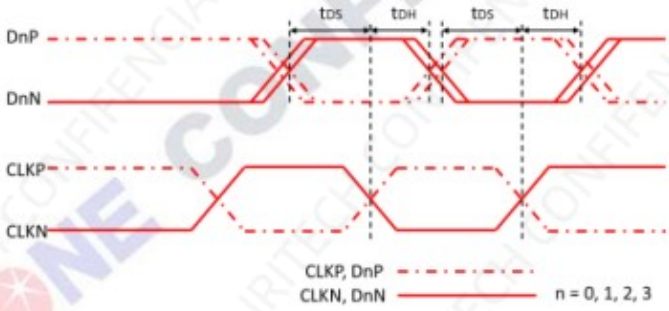


Figure 4-6 DSI Clock / Data Timings

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
Dn P/N (n=0,1,2 and 3)	tDS	Data to Clock Setup time	0.15*UI			UI	
	tDH	Clock to Data Hold time	0.15*UI			UI	

High Speed Mode - Rising and Falling Timings

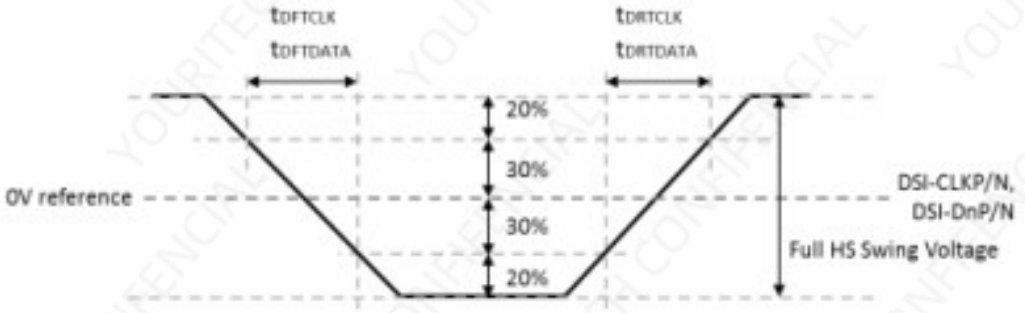


Figure 4-7 Rsing and Falling Timings

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150pS		0.3*UI		2,3
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N	150pS		0.3*UI		1,2,3
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150pS		0.3*UI		2,3
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N	150pS		0.3*UI		1,2,3

***Note* 1:** DnP/N, n =0,1,2 and 3

***Note* 2:** The display module has to meet timing requriements,which are defined for the transmitter (MCU) on MIPI D-PHY standard.

***Note* 3:** DSI-CLK+ = CLKP, DSI-CLK- =CLKN, DSI-D0+ =D0P, DSI-D0- =D0N

Low Speed Mode - Bus Turn Around

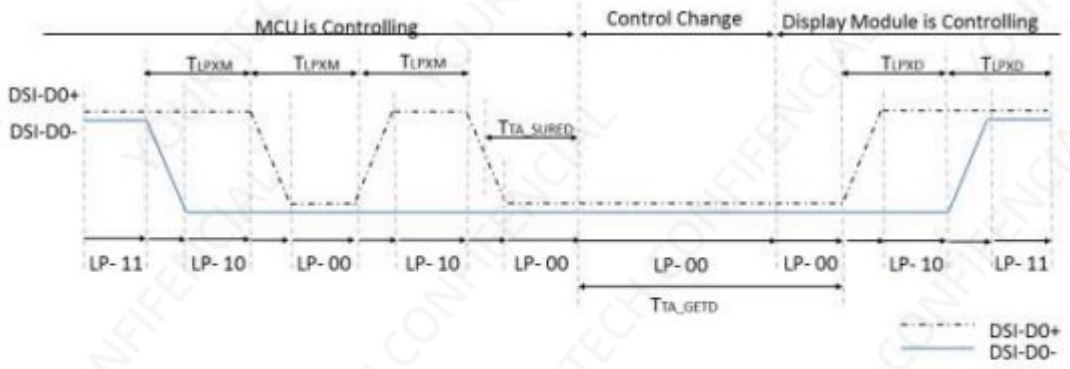


Figure 4-8 Bus Turnaround (BTA) from MCU to display module Timing

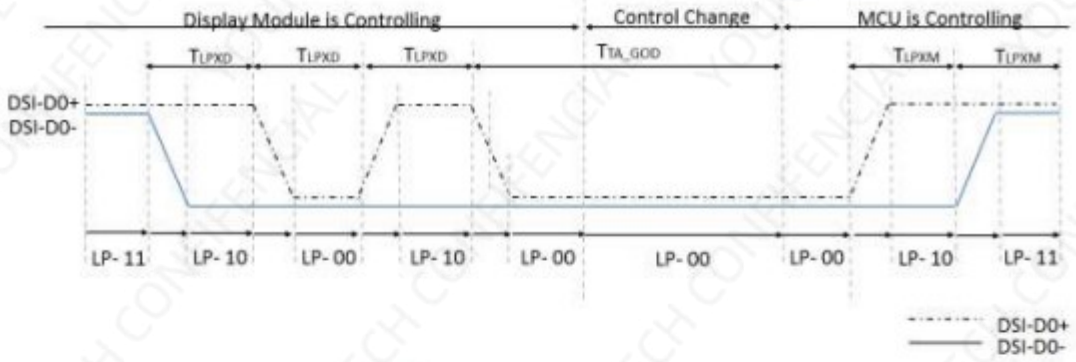


Figure 4-9 Bus Turnaround (BTA) from Display module to MCU Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
D0P/N	T_{LPXM}	Length of LP-00,LP-01,LP-10 or LP11 periods MCU to Display Module	50		75	nS	1
D0P/N	T_{LPXD}	Length of LP-00,LP-01,LP-10 or LP11 periods Display Module to MCU	50		75	nS	1
D0P/N	T_{TA_SURED}	Time-out before the Display Module starts driving	T_{LPXD}		2* T_{LPXD}	nS	1
D0P/N	T_{TA_GETD}	Time to drive LP-00 by Display Module	5* T_{LPXD}			nS	1
D0P/N	T_{TA_GOD}	Time to drive LP-00 after turnaround request -MCU	4 * T_{LPXD}			nS	1

Note 1: D0P = DSI-D0+, D0N = DSI-D0-

Data Lanes from Low Power Mode to High Speed Mode

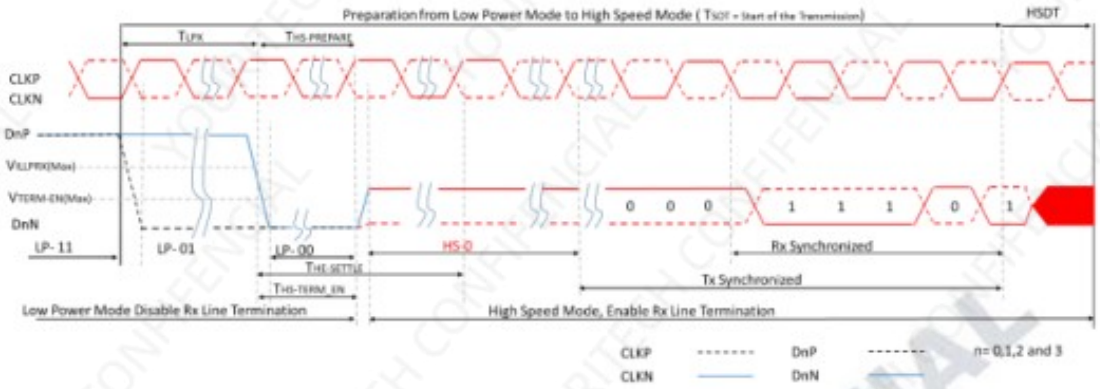
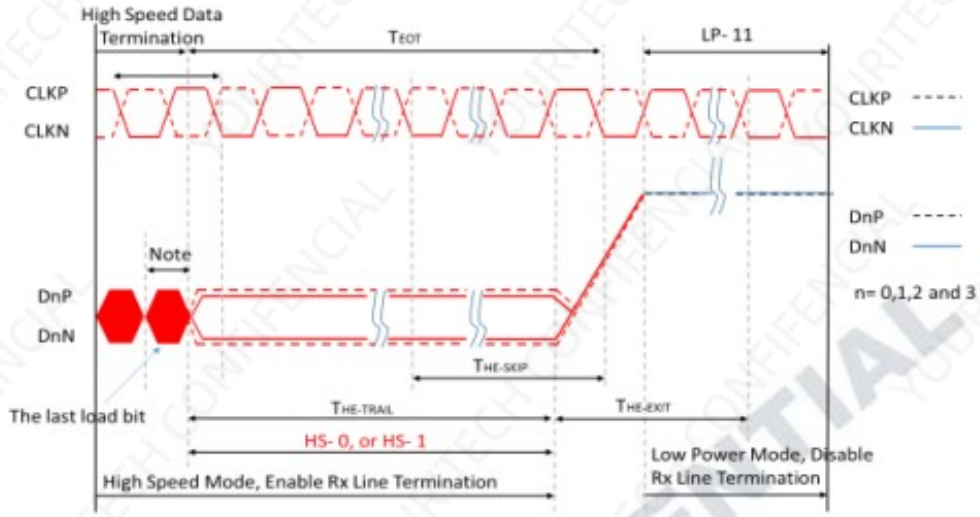


Figure 4-10 Data Lanes from Low Power Mode to High Speed Mode Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
DnP/N	TLPX	Length of any Low Power State Period	50			nS	1
DnP/N	THS-PREPARE	Time to drive LP-00 to prepare for HS Transmission	40+4*UI		85+6*UI	nS	1
DnP/N	THS-TREM-EN	Time to enable Data lane Receiver line termination measured from when Dn crosses VILMAX			35+4*UI	nS	1

Note 1: DnP/N, n=*0,1,2 and 3*

Data Lanes from High Speed Mode to Low Power Mode



Note:
If the last load bit is HS- 0, the transmitter changes from HS- 0 to HS- 1.
If the last load bit is HS- 1, the transmitter changes from HS- 1 to HS- 0

Figure 4-11 Data Lanes from High Speed Mode to Low Power Mode Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
DnP/N	THS-SKIP	Time-Out at Display Module to ignore transition period of EoT	40		55+4*UI	nS	1
DnP/N	THS-EXIT	Time to drive LP-11 after HS burst	100			nS	1

Note 1: DnP/N, n=*0,1,2 and 3*

DSI Clock Burst – High speed mode to /from Low Power Mode

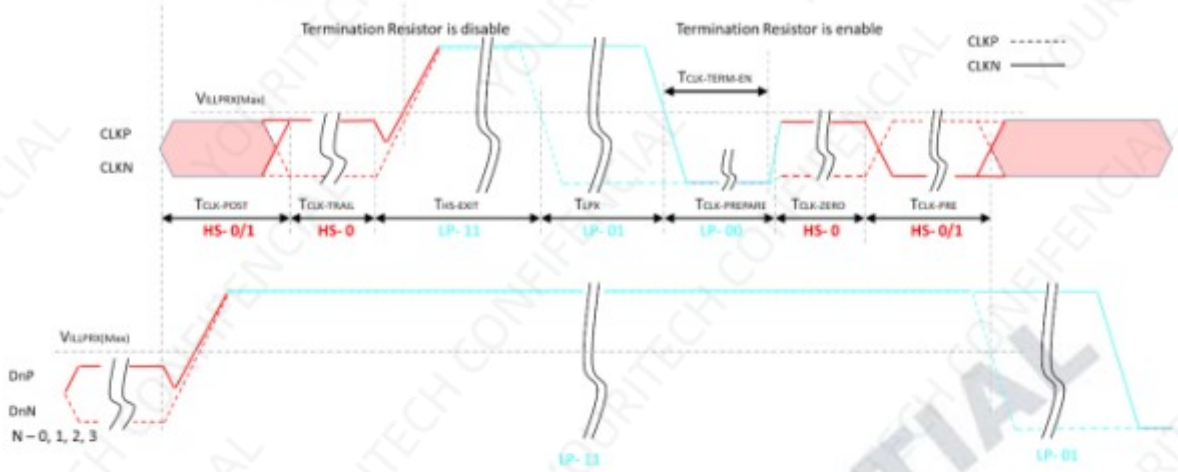


Figure 4-12 Clock Lane –High speed mode to / from Low Power Mode Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
CKP/N	$T_{CK\text{-}POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52*UI			nS	
CKP/N	$T_{CLK\text{-}TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60			nS	
CKP/N	$T_{HS\text{-}EXIT}$	Time to drive LP-11 after HS burst	100			nS	
CKP/N	$T_{CLK\text{-}PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38		95	nS	
CKP/N	$T_{CLK\text{-}TERM\text{-}EN}$	Time-out at Clock Lane to enable HS termination			38	nS	
CKP/N	$T_{CLK\text{-}PREPARE}$+ $T_{CLK\text{-}ZERO}$	Minimum lead HS-0 drive period before starting Clock	300			nS	
CKP/N	$T_{CLK\text{-}PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8*UI			nS	

Reset Input Timing

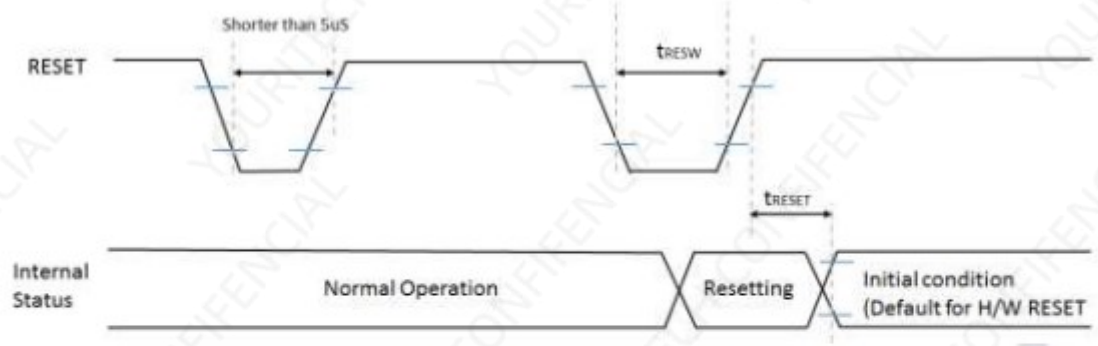


Figure 4-13 Reset Input Timing

Table 4-2 Reset Input Timing

Signal	Symbol	Parameter	Description	Specification			Unit	Notes
				MIN	TYP	MAX		
RESET	tRESW	Reset "L" pulse width		10			uS	1
	tRESET	Reset complete time	When reset applied during Sleep in mode			5	mS	2
			When reset applied during Sleep Out mode			120	mS	5

***Note* 1:** Condition : Ta =25℃

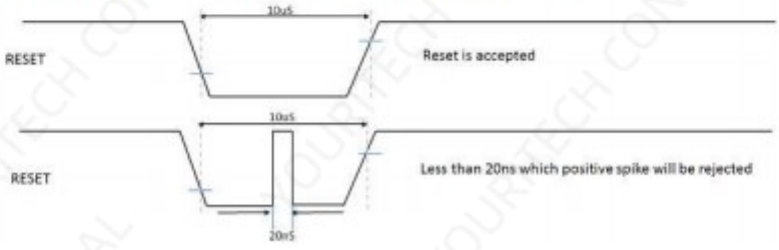
***Note* 2:** Spike due to an electrostatic discharge on RESET line does not cause irregular system reset according to the table below.

RESET Pulse	Action
Less than 5us	Reset Rejected
More than 10uS	Reset
Between 5us and 10uS	Reset Start

***Note* 2:** During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120ms, when Reset Starts in sleep out mode. The display remains the blank state in sleep in mode) and then return to Default condition for H/W RESET.

Note3: During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W RESET complete time (tRESET) within 5ms after a rising edge of RESET.

***Note 4*:** Spike Rejection also applies during a valid reset pulse as shown below:



***Note 5*:** It is necessary to wait 5ms after releasing RESET when sending commands, and Sleep Out command can not be sent within 120ms.

7. Optical Characteristics

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle range	Horizontal	Θ_3	CR > 10	70	80	-	Deg.	Note 1
		Θ_9		70	80	-	Deg.	
	Vertical	Θ_{12}		70	80	-	Deg.	
		Θ_6		70	80	-	Deg.	
Contrast ratio		CR	Θ = 0°	1000	1500	-	-	Note 2
Transmittance		Tr		3.56	4.1	-	%	-
White Chromaticity		Wx		-0.03	0.295	+0.03	-	CF@C light Note 3
		Wy			0.330			
Reproduction of color (C light)	Red	R_x			0.656			
		R_y			0.325			
	Green	G_x			0.258			
		G_y			0.586			
	Blue	B_x			0.134			
		B_y			0.117			
Response Time (Rising + Falling)		$T_r + T_f$	Ta= 25° C Θ = 0°	-	25	35	ms	Note 4
Flicker		FLK	Panel Center	-	15	20	%	Note5

Note :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o' clock direction with respect to the optical axis which is normal to the LCD surface (s ee FIGURE 1).

2. Contrast measurements shall be made at viewing angle of θ= 0° and at the center o f the LCD surface. Luminance shall be measured with all pixels in the view field set f irst to white, then to the dark (black) state (see FIGURE 1). Luminance Contrast Rat io (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. The color chromaticity coordinates specified in the above table shall be calculated f rom the spectral data measured with all pixels first in red, green, blue and white. Me asurements shall be made at the center of the panel.

4. The electro-optical response time measurements shall be made as FIGURE 2 show n in Appendix. The times needed for the luminance to change from 10% to 90% is T r, and 90% to 10% is Tf.

5. The flicker should be tested after MTP written.
Measure equipment：CA310. The probe needs to be aligned with the screen center, as close as possible but cannot on the screen.
Test pattern: 1Line Flicker.

Test pattern

Optical measurements

Figure1 Measurement Set Up

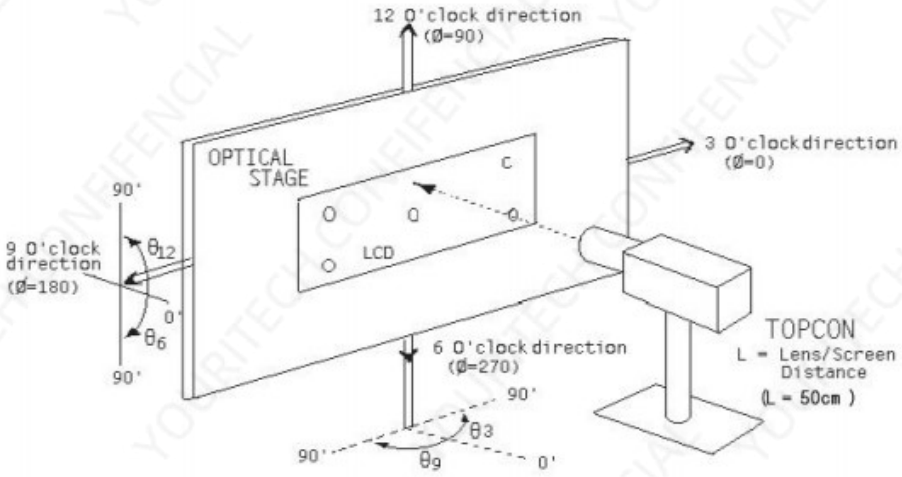
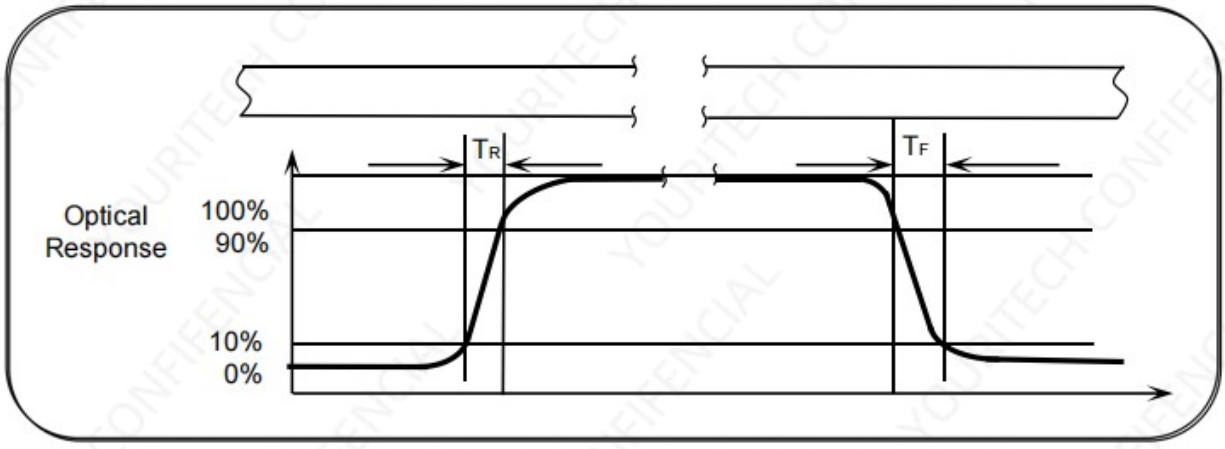


Figure2 Response Time Testing



8. Reliability Test Item

No.	Test Item	Test Condition	Notes
1	High Temp. Storage	+80°C / 96H	1. Functional test isOK. Missing Segment,short, unclear segment non-display,display abnormally and liquid crystal leakare un-allowed. 2. No low temperature bubbles,end seal loose andfall, frame rainbow.
2	Low Temp. Storage	-30°C / 96H	
3	High Tempe. Operating	+70°C / 96H	
4	Low Tempe. Operating	-20°C / 96H	
5	High Temperature /Humidity storage	50°C x 90%RH /96H	
6	Thermal and cold shock	Static state，-20℃（30min）~70℃（30min），50 cycles	

9. Packing Method----TBD

- END -