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Custom Display

Production Custom designs Installation

Mechanical design



SPECIFICATION FOR LCM Module

MODULE No:	ET070BA01-K
CUSTOMER:	

YOURITECH	INITIAL	DATE
PREPARED BY		
CHECKED BY		
APPROVED BY		

CUSTOMER	INITIAL	DATE
APPROVED BY		



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* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This module is composed of a Transmissive type TFT-LCD Panel, driver circuit, back-light unit. The resolution of a 7.0" TFT-LCD contains 280x1424 pixels, and can display up to 16.7M colors.

* Features

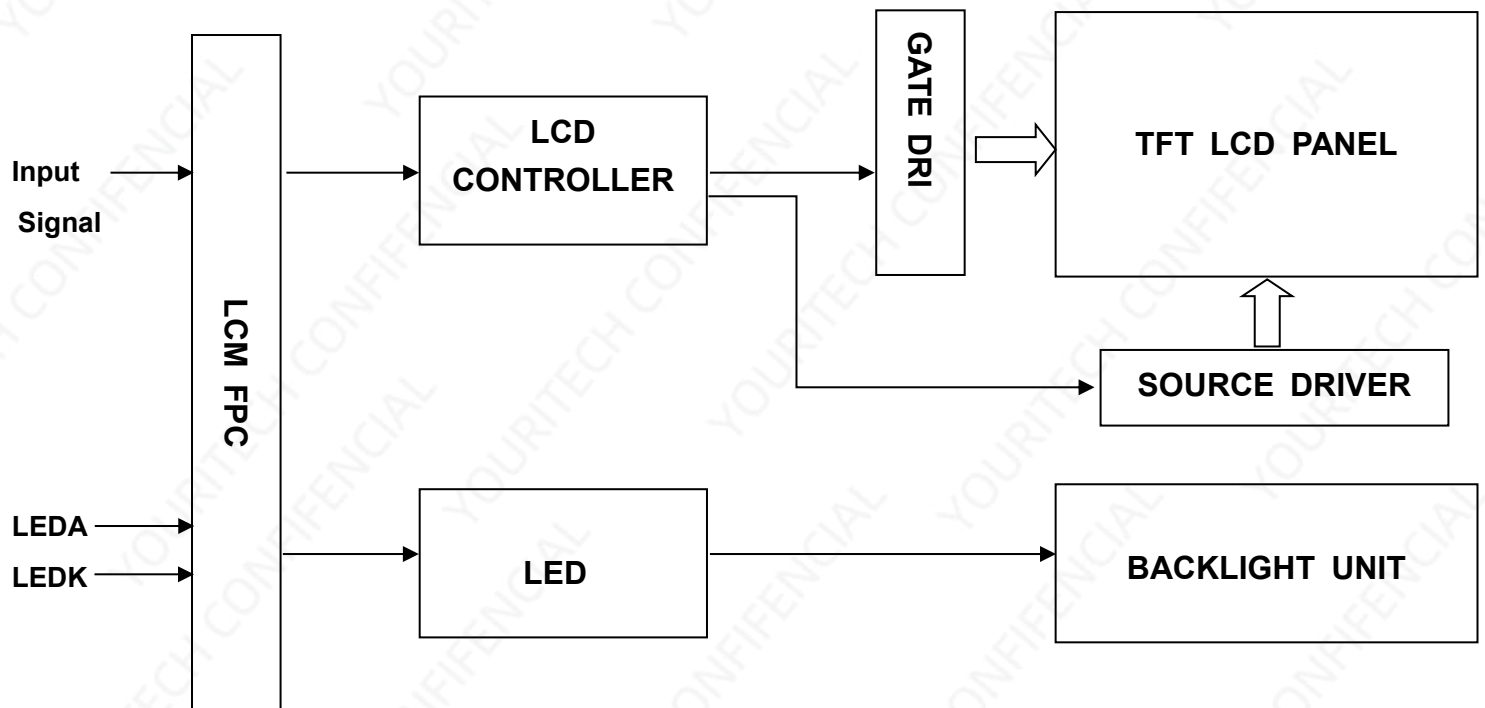
General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	33.60(H)*170.88(V) (7.0inch)	mm	-
Driver element	TFT active matrix	-	-
Display colors	16.7M	colors	-
Number of pixels	280(RGB)*1424	dots	-
TFT Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.0012(H)*0.0012(V)	mm	-
Viewing angle	ALL	o'clock	-
TFT Controller IC	OTA7290N	-	-
LCM Interface	4-lane MIPI	-	-
Display mode	Transmissive/Normally Black	-	-
Operating temperature	-20~+70	℃	-
Storage temperature	-30~+80	℃	-

* Mechanical Information

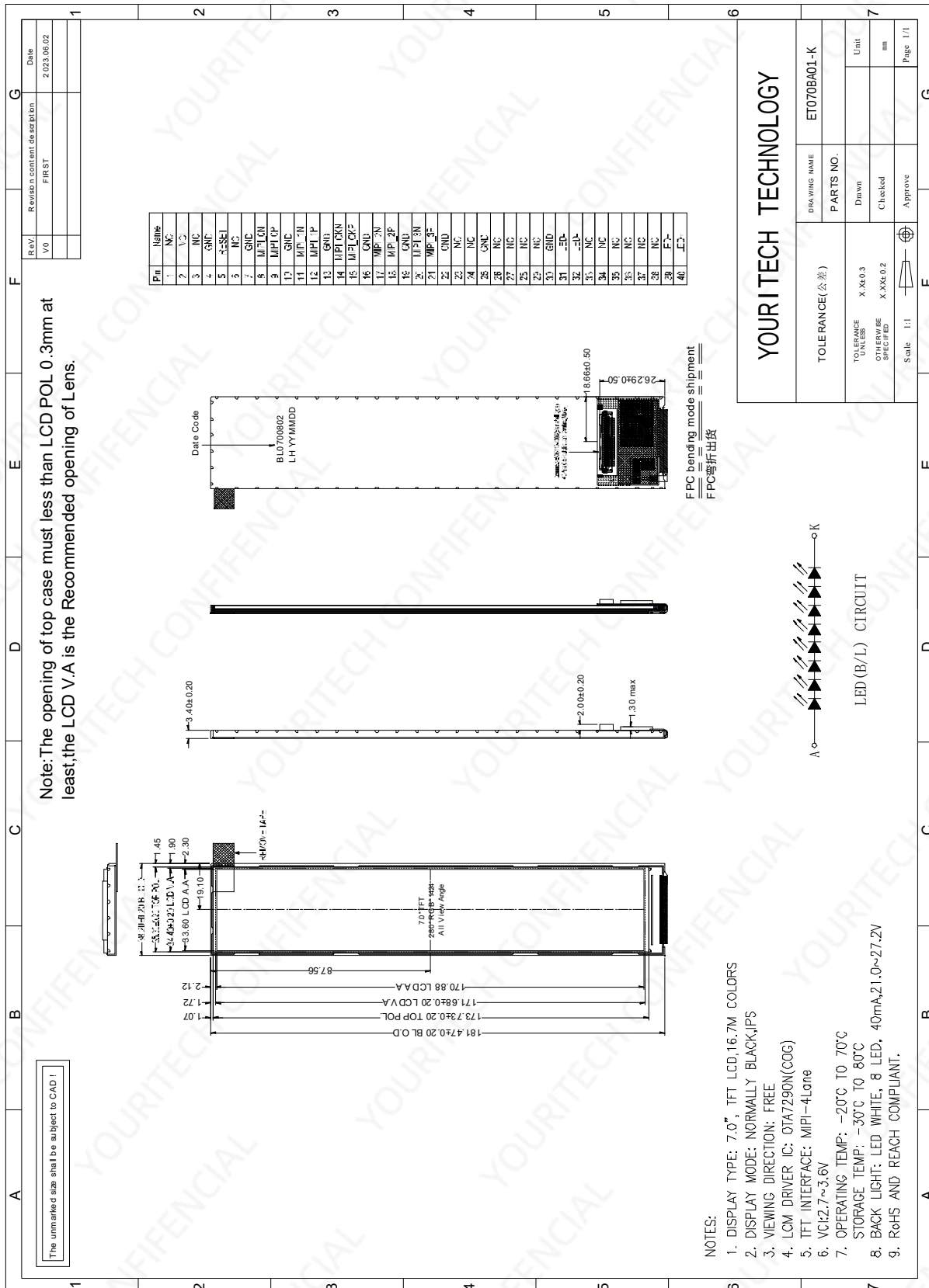
Item		Min.	Typ.	Max.	Unit	Note
FOG size	Horizontal(H)		38.20		mm	-
	Vertical(V)		181.47		mm	-
	Depth(D)		3.40		mm	-
Weight			46		g	-



1. Block Diagram



2. Outline dimension



3. Input terminal Pin Assignment

NO.	SYMBOL	DISCRIPTION	I/O
1	NC	--	--
2	VCI	Power supply for digital circuits	P
3	NC	--	--
4	GND	Ground	P
5	RESET	Global reset pin. Active low to enter reset state.	I
6	NC	--	--
7	GND	Ground	P
8	MIPI_0N	- MIPI DSI differential data pair. (Data lane 0)	I
9	MIPI_0P		
10	GND	Ground	P
11	MIPI_1N	- MIPI DSI differential data pair. (Data lane 1)	I
12	MIPI_1P		
13	GND	Ground	P
14	MIPI_CKN	- MIPI DSI differential clock pair	I
15	MIPI_CKP		
16	GND	Ground	P
17	MIPI_2N	- MIPI DSI differential data pair. (Data lane 2) Leave it open or fix to L GND level when not in use.	I
18	MIPI_2P		
19	GND	Ground	P
20	MIPI_3N	- MIPI DSI differential data pair. (Data lane 3) Leave it open or fix to GND level when not in use.	I
21	MIPI_3P		
22	GND	Ground	P
23	NC	--	--
24	NC	--	--
25	GND	Ground	P
26	NC	--	--
27	NC	--	--
28	NC	--	--
29	NC	--	--
30	GND	Ground	P
31	LED-	LED Cathode	P



32	LED-		
33	NC	--	--
34	NC	--	--
35	NC	--	--
36	NC	--	--
37	NC	--	--
38	NC	--	--
39	LED+	LED Anode	P
40	LED+		



4. LCD Optical Characteristics

4.1 Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit.	Note
Contrast Ratio		CR	Normal viewing angle	800	1000	--		(1)(2)
Response time	Rising	T _R +T _F		--	30	40	msec	(1)(3)
	Falling							
Color Gamut		S(%)		45	53.59	--	%	
solor Filter Chromacicity	White	W _X		-0.04	0.3099	+0.04		(1)(4) CF glass
		W _Y			0.3229			
	Red	R _X			0.6192			
		R _Y			0.3618			
	Green	G _X			0.3538			
		G _Y			0.5626			
	Blue	B _X			0.1451			
		B _Y			0.0816			
Viewing angle	Hor.	Θ _L	CR>10	75	80	--		(1)(4)
		Θ _R		75	80	--		
	Ver.	Θ _U		75	80	--		
		Θ _D		75	80	--		
Option View Direction		ALL						

*The data comes from the LCD specification.

Measuring Condition

Measuring surrounding : dark room

Ambient temperature : $25\pm 2^\circ\text{C}$

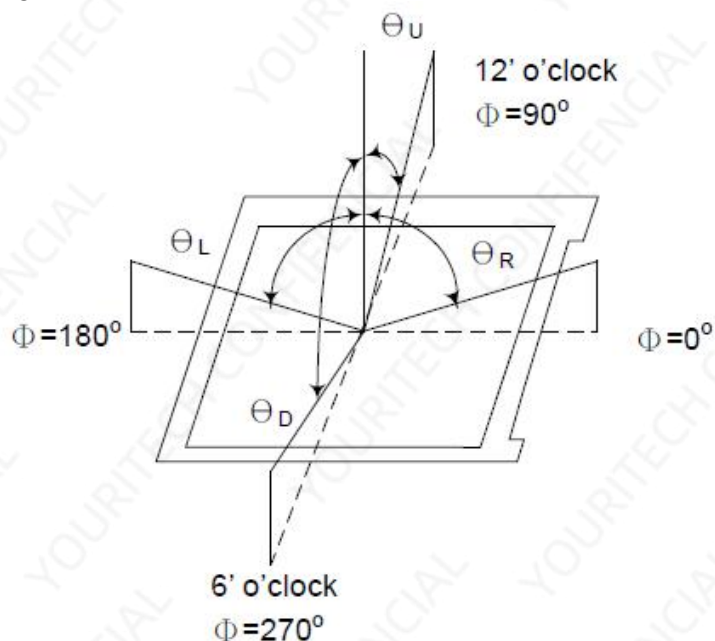
15min. warm-up time.

Measuring Equipment

FPM520 , which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.



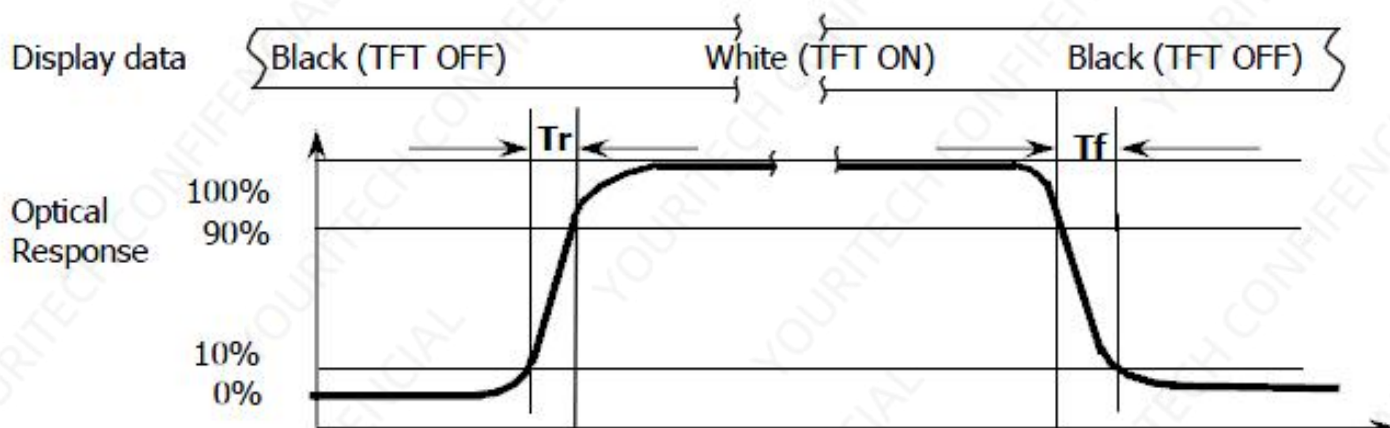
Note (1): Definition of Viewing Angle :



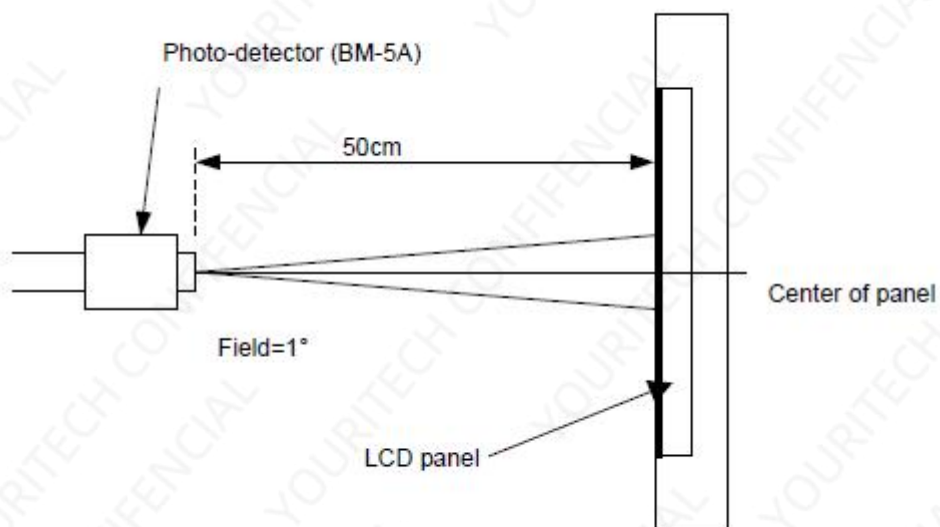
Note (2): Definition of Contrast Ratio(CR) :measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note (3): Response Time



Note (4): Definition of optical measurement setup



5. TFT Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 VSS=0V)

Characteristics	Symbol	Min.	Max.	Unit	Note
Digital Supply Voltage	VCI	-0.5	4.0	V	Note1
Operating temperature	T _{OP}	-20	+70	°C	
Storage temperature	T _{ST}	-30	+80	°C	

NOTE1: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VCI	3.0	3.3	3.6	V	--
Normal mode Current consumption	IDD	--	90	180	mA	--
Level input voltage	V _{IH}	0.7 VCI	--	VCI	V	--
	V _{IL}	-0.3	--	0.3 VCI	V	--
Level output voltage	V _{OH}	0.8* VCI	--	VC	V	--
	V _{OL}	GND	--	0.2 VCI	V	--



5.3 LED Backlight Characteristics

The back-light system is edge-lighting type with 8 chips White LED

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I_F	20	40	--	mA	
Forward Voltage	V_F	--	25.60	--	V	--
LCM Luminance IF=40mA	L_V	600	650	--	cd/m2	Note3
LED life time	Hr	50000			Hour	Note1,2
Uniformity	AVg	80	--	--	%	Note3

Note1: LED life time (Hr) can be defined as the time in which it continues to operate under the condition:

$T_a=25\pm3\text{ }^{\circ}\text{C}$, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The “LED life time” is defined as the module brightness decrease to 50% original brightness at

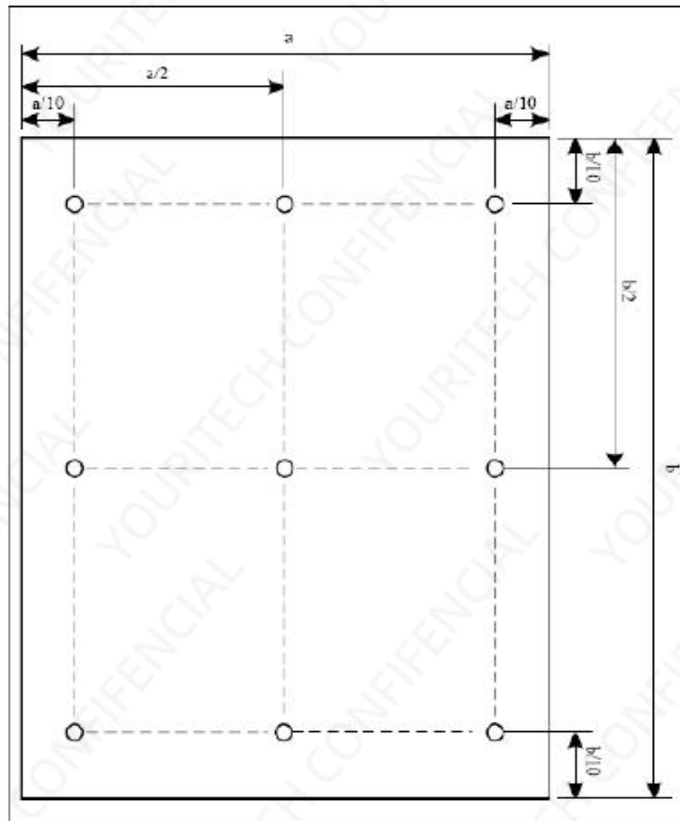
$T_a=25^{\circ}\text{C}$ and $I_L=40\text{mA}$. The LED lifetime could be decreased if operating I_L is larger than 40mA. The constant current driving method is suggested.



LED(B/L) CIRCUIT



NOTE 3: Luminance Uniformity of these 9 points is defined as below:



$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$



6. DC Characteristics

6.1 System characteristics

(VCC=1.5V, VDD=3.3V, AVDD=12V, VSS=VSSA=0V, TA=-20 to +85°C)

Parameter	Symbol	MIN.	Typ.	MAX.	UNIT	Conditions
VDD Input low voltage level	Vil1	0	-	0.3*VDD	V	For the VDD domain inputs.
VDD Input high voltage level	Vih1	0.7*VDD	-	VDD	V	For the VDD domain inputs.
VCC Input low voltage level	Vil2	0	-	0.2*VCC	V	For the VCC domain inputs.
VCC Input high voltage level	Vih2	0.8*VCC	-	VCC	V	For the VCC domain inputs.
I2C Low level input voltage	Vil3	1.65		VDD	V	For SDA/SCL inputs
I2C High level input voltage	Vih3	0		0.2	V	For SDA/SCL inputs
Input leakage current	Ii	-	-	+/- 1	μA	For the digital, I/O circuit (Not include the pull-up/down current)
Output high voltage level	Voh	0.8*VDD	-	-	V	For VDD domain outputs, Ioh = 400uA
Output low voltage level	Vol	-	-	0.2*VDD	V	For VDD domain outputs, Iol = 400uA
Differential input leakage Current	I _{DIFF}	-10		+10	uA	For DxP, DxN, CLKP, CLKN (With steady state inputs)
Pull low/high resistor	Ri	100K	250K	500K	ohm	For the digital Input pin VDD=3.3, VCC=1.5
Output Voltage deviation	VOD1		±20	±35	mV	Vo = AGND+0.2V ~ AGND+1.5V Vo = HAVDD-0.2V ~ HAVDD-1.5V Vo = HAVDD+0.2V ~ HAVDD+1.5V
Output Voltage deviation	VOD2		±15	±20	mV	Vo = AGND+0.2V ~ AGND+1.5V Vo = AGND+1.5V ~ HAVDD-1.5V Vo = HAVDD+1.5V ~ AVDD-1.5V
Output Voltage Offset between Chips	VOC			±20		Vo = AGND+1.5V ~ HAVDD-1.5V Vo = HAVDD+1.5V ~ AVDD-1.5V
Input level of V1 ~ V7	Vref1	HAVDD+0.2	-	AVDD-0.2	V	Gamma positive voltage input
Input level of V8 ~ V14	Vref2	0.2	-	HAVDD-0.2	V	Gamma negative voltage input
Dynamic Range of Output	Vdr	0.2	-	AVDD-0.2	V	S0 ~ S1802
Sinking Current of Outputs	IOLy	80	-	-	μA	S0 ~ S1802
Driving Current of Outputs	IOHy	80	-	-	μA	S0 ~ S1802
Digital Operation current	Idd	-	TBD	-	mA	
Digital Stand-by current	Ist1	-	1.15	2.5	mA	
Analog Operation current	Idda	-	TBD	-	mA	
Analog Stand-by current	Ist2	-	3.5	6.9	mA	



6.2 MIPI DC Characteristics

HS Receiver DC Specification

Parameter	Symbol	Rating			Unit	Note
		Min	Typ	Max		
Operation Voltage	VDD	1.5-10%	1.5	1.5+10%	mV	
Differential Input Voltage	VID	70	200	260	mV	
Common Mode Voltage	V _{CMRX(DC)}	70	-	330	mV	
Differential Input High Threshold Voltage	V _{TH}	-	-	70	mV	
Differential Input Low Threshold Voltage	V _{TL}	-70	-	-	mV	
Singled-ended input high voltage	V _{IHHS}	-	-	460	mV	
Singled-ended input low voltage	V _{ILHS}	-40	-	-	mV	
Singled-ended threshold for HS termination enable	V _{TERM-EN}	-	-	450	mV	
Differential input impedance	Z _{ID}	80	100	125	ohm	
Pin leakage current	I _{LEAK}	-10	-	10	uA	
Common-mode interference beyond 450MHz	ΔV _{CMRX(HF)}	-	-	100	mV	
Common-mode interference 50MHz - 450MHz	ΔV _{CMRX(LF)}	-50	-	50	mV	
Common-mode termination	C _{CM}	-	-	60	pF	
Embedded Termination	R _T	90	100	110	ohm	2bits RT_SEL[1: 0] for termination resistor selection 00 → 200ohm 10, 01 → 150ohm 11 → 100ohm (default) 1bit ERM _R _EN for termination resistor enable TERM _R _EN=0, termr disable R=(OPEN) TERM _R _EN=1, termr enable

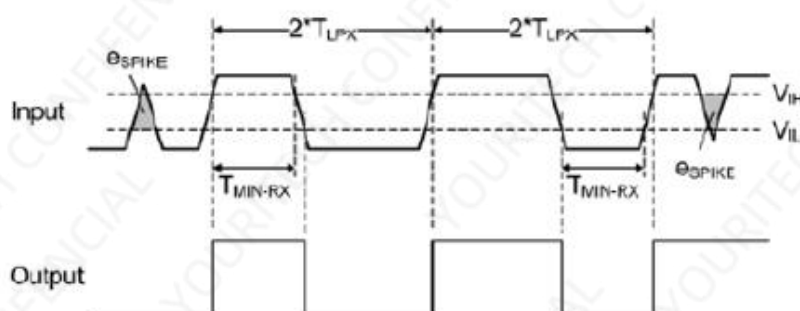
Note:

- (1) Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.
- (2) This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz.



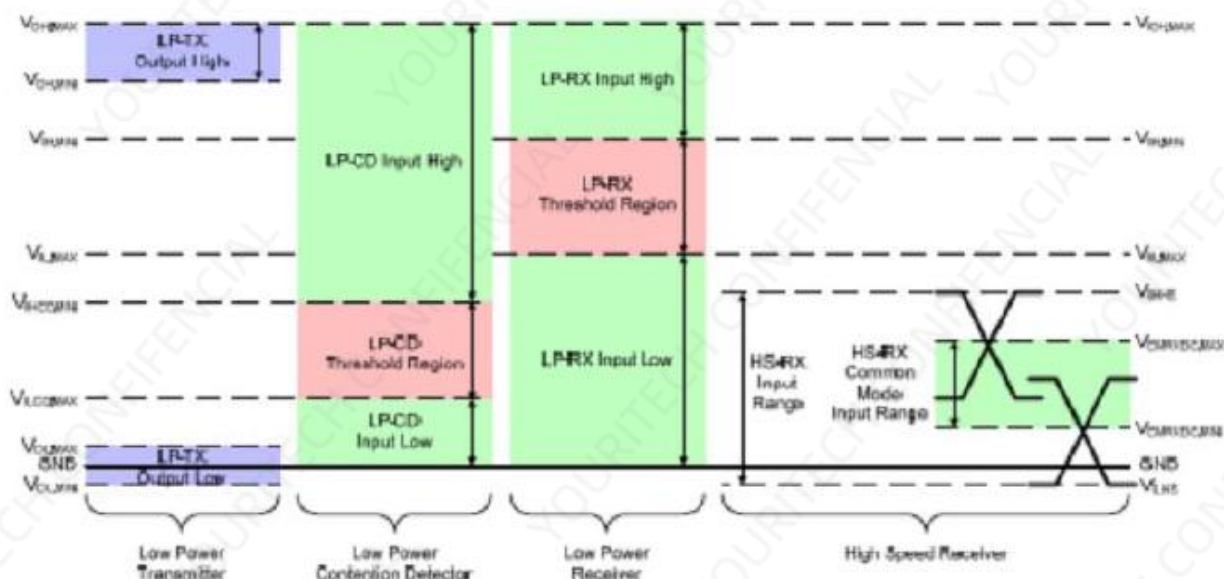
LP Receiver DC Specification

Parameter	Symbol	Rating			Unit	Note
		Min	Typ	Max		
Logic 1 input voltage	V_{IH}	880	-	-	mV	
Logic 0 input voltage, not in ULP State	V_{IL}	-	-	550	mV	
Input hysteresis	V_{HYST}	25	-	-	mV	



Line Contention Detection

Parameter	Symbol	Rating			Unit	Note
		Min	Typ	Max		
Logic 1 contention threshold	V_{IHCD}	450	-	-	mV	
Logic 0 contention threshold	V_{ILCD}	-	-	200	mV	



Input Characteristics

Parameter	Symbol	Rating			Unit	Note
		Min	Typ	Max		
Pin signal voltage range	V_{PIN}	-50		1350	mV	
Pin leakage current	I_{LEAK}	-10		10	uA	
Ground shift	$V_{GND SH}$	-50		50	mV	
Transient pin voltage level	$V_{PIN(ABS MAX)}$	-0.15		1.45	V	
Maximum transient time above $V_{PIN(max)}$ or below $V_{PIN(min)}$	$TV_{PIN(ABS MAX)}$			20	ns	

Note:

- (1) When the pad voltage is in the signal voltage range from $V_{GND SH}$, MIN to $VOH + V_{GND SH}$, MAX and the Lane Module is in LP receive mode.
- (2) The voltage overshoot and undershoot beyond the V_{PIN} is only allowed during a single 20ns window after any LP-0 to LP-1 transition or vice versa. For all other situations it must stay within the V_{PIN} range.
- (3) This value includes ground shift.



7. AC Characteristics

7.1 System AC Characteristics

(VDD=3.3V, AVDD=12V, VSS=VSSA=0V, TA=-20 to +85°C)

Parameter	Symbol	MIN.	Typ.	MAX.	UNIT	Conditions
VDD Power On Slew rate	T	-	-	20	ms	From VSS to 90% VDD
RSTB pulse width	T	10	-	-	us	

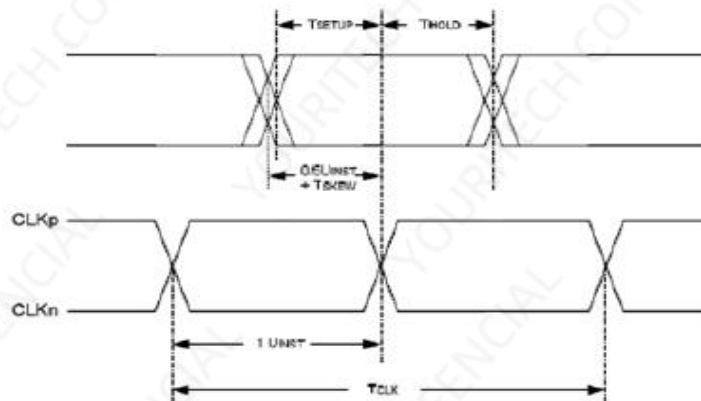
7.2 MIPI AC Chrematistics

HS Receiver AC Timing Characteristics

Parameter	Symbol	Rating			Unit	Note
		Min	Typ	Max		
Bandwidth per lane	-	-	-	1000	Mbps	Bandwidth selected by register 'speedup' Speedup=0 → Max=550Mbps Speedup=1 → Max=1000Mbps
Operation frequency	-	-	-	500	MHz	
UI instantaneous	UI _{INST}	1	-	12.5	ns	1
Data to Clock Skew	T _{skew}	-0.15	-	0.15	UI _{INST}	
Inter-lane static skew	T _{skew-lane}	-	-	UI _{INST} /50	UI _{INST}	
Data to Clock Setup Time	T _{SETUP}	0.25	-	-	UI _{INST}	2
Data to Clock Hold Time	T _{HOLD}	0.25	-	-	UI _{INST}	
Common-mode interference beyond 450MHz	ΔV _{CMRX(HF)}	-	-	100	mV	4
Common-mode interference 50MHz- 450MHz	ΔV _{CMRX(LF)}	-50	-	50	mV	3,6
Common-mode termination	C _{CM}	-	-	60	pF	5

Note:

- (1) Total silicon and package delay budget of 0.3*UI_{INST}
- (2) Total setup and hold window for receiver of 0.3*UI_{INST}
- (3) Excluding 'static' ground shift of 50mV
- (4) ΔV_{CMRX} (HF) is the peak amplitude of a sine wave superimposed on the receiver input
- (5) For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.
- (6) Voltage difference compared to the DC average common-mode potential.



LP Receiver AC Timing Characteristics

Parameter	Symbol	Rating			Unit	Note
		Min	Typ	Max		
Input pulse rejection	θ_{SPIKE}	-	-	300	V·ps	1,2,3
Minimum pulse width response	T_{MIN-RX}	20	-	-	ns	
Peak interference amplitude	V_{INT}	-	-	200	mV	
Interference frequency	f_{INT}	450	-	-	MHz	
Logic 1 input voltage	V_{IH}	880	-	-	mV	
Logic 0 input voltage, not in ULP State	V_{IL}	-	-	550	mV	
Logic 0 input voltage, ULP State	$V_{IL-ULPS}$	-	-	300	mV	
Input Hysteresis	V_{HYST}	25	-	-	mV	
Logic 1 contention threshold	V_{IHCD}	450	-	-	mV	
Logic 0 contention threshold	V_{ILCD}	-	-	200	mV	

Note:

- (1) Time-voltage integration of a spike above V_{IL} when being in LP-0 state or below V_{IH} when being in LP-1 state.
- (2) An impulse less than this will not change the receiver state.
- (3) In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.



8.0 Timing for DSI video mode

Parameter	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency	FCLK	--	(36)	--	MHz
Horizontal display area	HDISP	--	280	--	Clock
Horizontal Sync. Width	hpw	5	10	50	Clock
Horizontal Sync. Back Porch	hbp	35	50	100	Clock
Horizontal Sync. Front Porch	hfp	35	50	200	Clock
Vertical display area	VDISP	--	1424	--	Line
Vertical Sync. Width	vs	10	20	50	Line
Vertical Sync. Back Porch	vbp	20	30	100	Line
Vertical Sync. Front Porch	vfp	20	30	200	Line
Frame-Rate	Fr	--	60	--	Hz

Note:

The best frame rate setting : 2 data lanes : 50~60 Hz / 3 data lanes : 50~70 Hz / 4 data lanes : 50~70 Hz.



9. LCD Module Out-Going Quality Level

9.1 VISUAL & FUNCTION INSPECTION STANDARD

9.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

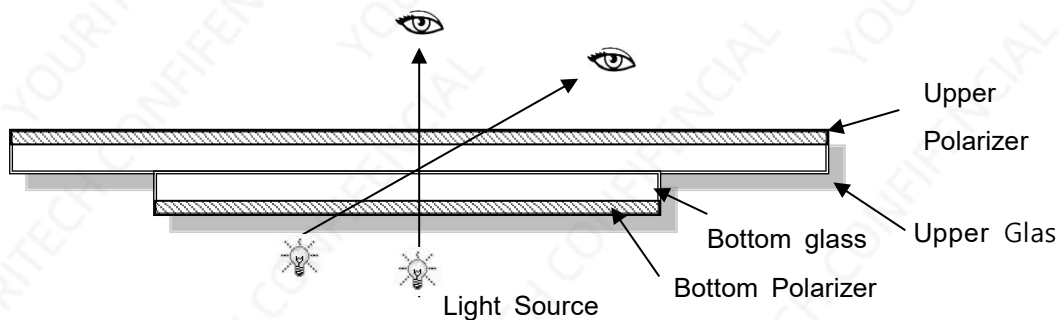
Temperature : $25\pm 5^{\circ}\text{C}$

Humidity : $65\%\pm 10\%\text{RH}$

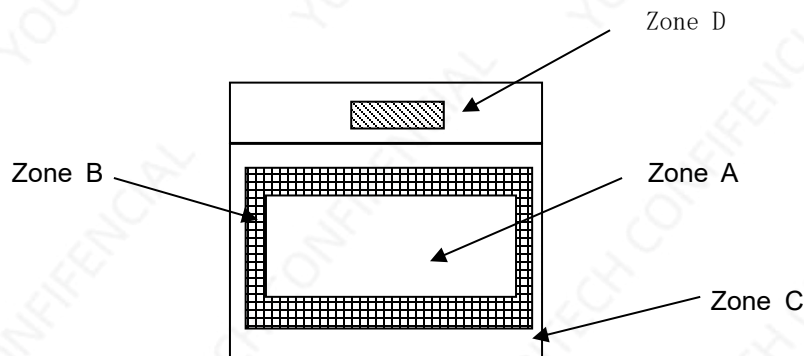
Viewing Angle : Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance:30-50cm



9.1.2 Definition



Zone A : Effective Viewing Area(Character or Digit can be seen)

Zone B : Viewing Area except Zone A

Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer .)

Zone D : IC Bonding Area

Note:As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer



9.1.3 Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class II

AQL:

Major defect	Minor defect
0.65	1.5

LCD: Liquid Crystal Display , LCM: Liquid Crystal Module

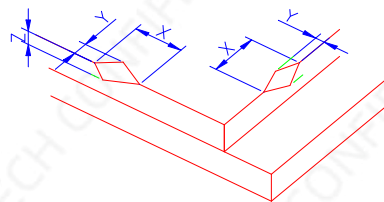
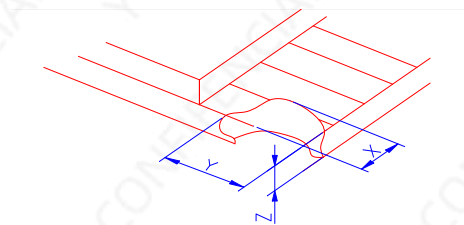
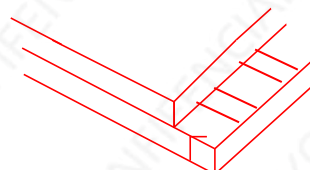
No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. etc...	Major
2	Missing	Missing components and etc...	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed, deformation and etc...	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Spot/Line defect	Light dot, Dim spot, (Note1) Polarizer Air Bubble, Polarizer accidented spot and etc...	
6	Soldering appearance	Good soldering , Peeling off is not allowed and etc...	
7	LCD/Polarizer	Black/White spot/line, scratch, crack, etc.	

Note1: a) Light dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

b) Dim dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.



9.1.4 Criteria (Visual)

Number	Items	Criteria(mm)						
1.0 LCD Crack/Broken NOTE: X: Length Y: Width Z: Height L: Length of IT O, T: Height of LCD	(1) The edge of LCD broken	 <table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>≤3.0mm</td><td><Inner border line of the seal</td><td>≤T</td></tr></table>	X	Y	Z	≤3.0mm	<Inner border line of the seal	≤T
	X	Y	Z					
	≤3.0mm	<Inner border line of the seal	≤T					
(2)LCD corner broken	 <table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr></table>	X	Y	Z	≤3.0mm	≤L	≤T	
X	Y	Z						
≤3.0mm	≤L	≤T						
(3) LCD crack	 Crack Not allowed							



Spot defect

2.0

Φ=(X+Y)/2

① light dot (black/white spot , pinhole, stain, etc.)

Zone Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.15	Ignore	Ignore	
0.15<Φ≤0.25	3(distance ≥ 10mm)		
0.25<Φ≤0.4	2(distance ≥ 10mm)		
Φ>0.4	0		

② Dim spot (light leakage、dent、dark spot, etc)

Zone Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.15	Ignore	Ignore	
0.15<Φ≤0.25	3(distance ≥ 10mm)		
0.25<Φ≤0.4	2(distance ≥ 10mm)		
Φ>0.4	0		

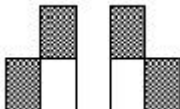
③ Polarizer accidented spot

Zone Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.2<Φ≤0.5	2(distance ≥ 10mm)		
Φ>0.5	0		

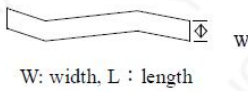
④Polarizer Bubble

Zone Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.2<Φ≤0.4	2(distance ≥ 10mm)		
0.4<Φ≤0.5	1		
Φ>0.5	0		



3.0	LCD Pixel defect	Pixel bad points <table border="1" data-bbox="539 309 1493 1055"> <thead> <tr> <th data-bbox="539 309 730 360">Item</th><th data-bbox="730 309 1241 360">Zone A</th><th data-bbox="1241 309 1493 360">Acceptable Qt</th></tr> </thead> <tbody> <tr> <td data-bbox="539 360 730 521" rowspan="3">Bright dot</td><td data-bbox="730 360 1241 416">Random</td><td data-bbox="1241 360 1493 416">$N \leq 2$</td></tr> <tr> <td data-bbox="730 416 1241 472">2 dots adjacent</td><td data-bbox="1241 416 1493 472">$N \leq 0$</td></tr> <tr> <td data-bbox="730 472 1241 521">3 dots adjacent</td><td data-bbox="1241 472 1493 521">$N \leq 0$</td></tr> <tr> <td data-bbox="539 521 730 689" rowspan="3">Dark dot</td><td data-bbox="730 521 1241 577">Random</td><td data-bbox="1241 521 1493 577">$N \leq 3$</td></tr> <tr> <td data-bbox="730 577 1241 633">2 dots adjacent</td><td data-bbox="1241 577 1493 633">$N \leq 0$</td></tr> <tr> <td data-bbox="730 633 1241 689">3 dots adjacent</td><td data-bbox="1241 633 1493 689">$N \leq 0$</td></tr> <tr> <td data-bbox="539 689 730 999">Distance</td><td data-bbox="730 689 1241 999"> 1. Minimum Distance Between Bright dots. 2. Minimum Distance Between dark dots 3. Minimum Distance Between dark and bright dot. </td><td data-bbox="1241 689 1493 999">5mm</td></tr> <tr> <td colspan="2" data-bbox="539 999 1241 1055">Total bright and dark dot</td><td data-bbox="1241 999 1493 1055">$N \leq 4$</td></tr> </tbody> </table> Note: A) Bright dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern. B) Dark dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture. C) 2 dot adjacent = 1 pair = 2 dots Picture:  2 dot adjacent  2 dot adjacent (vertical)  2 dot adjacent  2 dot adjacent (slant)	Item	Zone A	Acceptable Qt	Bright dot	Random	$N \leq 2$	2 dots adjacent	$N \leq 0$	3 dots adjacent	$N \leq 0$	Dark dot	Random	$N \leq 3$	2 dots adjacent	$N \leq 0$	3 dots adjacent	$N \leq 0$	Distance	1. Minimum Distance Between Bright dots. 2. Minimum Distance Between dark dots 3. Minimum Distance Between dark and bright dot.	5mm	Total bright and dark dot		$N \leq 4$
Item	Zone A	Acceptable Qt																							
Bright dot	Random	$N \leq 2$																							
	2 dots adjacent	$N \leq 0$																							
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Dark dot	Random	$N \leq 3$																							
	2 dots adjacent	$N \leq 0$																							
	3 dots adjacent	$N \leq 0$																							
Distance	1. Minimum Distance Between Bright dots. 2. Minimum Distance Between dark dots 3. Minimum Distance Between dark and bright dot.	5mm																							
Total bright and dark dot		$N \leq 4$																							



4.0	Line defect (LCD /Polarizer backlight black/white line, scratch, stain)  W: width, L : length N : Count	Width(mm)	Length(m m)	Acceptable Qty		
				A	B	C
		$\Phi \leq 0.05$	Ignore	Ignore		Ignore
		$0.05 < W \leq 0.06$	$L \leq 5.0$	$N \leq 3$		
		$0.06 < W \leq 0.08$	$L \leq 4.0$	$N \leq 2$		
$W > 0.08$	Define as spot defect					

5.0	Electronic Components SMT.	Not allow missing parts, solderless connection, cold solder joint, mismatch, The positive and negative polarity opposite
6.0	Display color& Brightness.	1. Color: Measuring the color coordinates, The measurement standard according to the datasheet or samples. 2. Brightness: Measuring the brightness of White screen, The measurement standard according to the datasheet or Samples.
7.0	LCD Mura/Waving/ Hot spot	Not visible through 5% ND filter in 50% gray or judge by limit sample if necessary.

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed



10. Reliability Test Result

Item	Condition	Inspection after test
High Temperature Operating	70°C,96H	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1.Air bubble in the LCD; 2.Non-display; 3.Missing segments/line; 4.Glass crack; 5.Current IDD is twice higher than initial value.
Low Temperature Operating	-20°C, 96HR	
High Temperature Storage	80°C, 96HR	
Low Temperature Storage	-30°C, 96HR	
High Temperature & High Humidity Operating	+60°C, 90% RH ,96 hours.	
Thermal Shock (Non-operation)	-10°C,30 min ↔ +60°C,30 min, Change time:5min 20CYC.	
ESD test	C=150pF, R=330,5points/panel Air:±8KV, 5times; Contact:±6KV, 5 times; (Environment: 15°C~35°C, 30%~60%).	
Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total) (Package condition).	
Box Drop Test	1 Corner 3 Edges 6 faces,80cm(MEDIUM BOX)	

Remark:

- 1.The test samples should be applied to only one test item.
- 2.Sample size for each test item is 5~10pcs.
- 3.For Damp Proof Test, Pure water(Resistance > 10MΩ) should be used.
- 4.In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.
- 5.Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.
6. The color fading mura of polarizing filter should not care.



11. Cautions and Handling Precautions

11.1 Handling and Operating the Module

- (1) When the module is assembled, it should be attached to the system firmly.
Do not warp or twist the module during assembly work.
- (2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
- (3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
- (4) Do not allow drops of water or chemicals to remain on the display surface.
If you have the droplets for a long time, staining and discoloration may occur.
- (5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
- (6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.
Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static; it may cause damage to the CMOS ICs.
- (9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (10) Do not disassemble the module.
- (11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
- (12) Pins of I/F connector shall not be touched directly with bare hands.
- (13) Do not connect, disconnect the module in the "Power ON" condition.
- (14) Power supply should always be turned on/off by the item 6.1 Power On Sequence & 6.2 Power Off Sequence

11.2 Storage and Transportation.

- (1) Do not leave the panel in high temperature, and high humidity for a long time.
It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%
- (2) Do not store the TFT-LCD module in direct sunlight.
- (3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
- (4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.
In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
- (5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

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