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Production Custom designs Installation

Mechanical design



Project No. 项目编号	ET070WS06-TT
Customer 客户名称	
Module No. 客户型号	
Product type 产品内容	Standard LCD Module TFT: 600*RGBx1024Dots 6.95" TFT LCD+CTP

客户确认Customer Approval

项目负责人Project Manager	
品质主管Director of Quality	
采购工程师Purchasing Engineer	

PREPARED BY	CHECKED BY	APPROVED BY



1. Introduction

1.1 Scope of application

This specification applies to the LCD module that is supplied by YOURITECH Technology CO., LTD.

LCD specification: Dots 600xRGBx1024

As to basic specification of the driver IC, refer to the IC (JD9365DA-H3) specification and data book.

All material & processing of the LCD module should be Lead Free.

1.2 TFT features:

Structure: TFT PANNEL+IC +FPC+BL+CTP;

ALL Viewing Type LCD

600 dot-segment and 1024 dot-common outputs;

16.7M Color can be selected by software;

White LED back light;

4lane MIPI interface

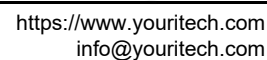
1.3 Applications:



2. LCM General specification

ITEM	Standard value	Unit
LCD Type	Normally Black	--
Drive element	TFT active matrix	--
Number of pixels	600*3RGB(H)X1024(V)	Dots
Pixel arrangement	RGB Vertical Stripe	--
Pixel Pitch (W*H)	0.1488(H) X 0.1488(V)	mm
Active area	89.28(H) x 152.37(V)	mm
Viewing direction	ALL O'CLOCK	--
TFT Driver IC	JD9365DA-H	--
TFT interface	4lane MIPI interface	--
Approx. Weight	TBD	g
LCM Size(W*H*T)	94.58(W) ×161.29(H) ×2.53(T)	mm
LCM+CTP Size(W*H*T)	104.36(W) ×178.67(H) ×5.28(T)	mm
Touch structure	G+G	--
Touch Driver IC	ST1633I	--
Touch Interface	I2C	--





3. Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
LCM Operating Temperature	T _{OPR}	-20	+70	°C
LCM Storage Temperature	T _{STG}	-30	+80	°C
TP Operating Temperature & Humidity (20% ~ 90%RH)	T _{OPR}	-20	+70	°C
TP SStorage Temperature & Humidity (20% ~ 90%RH)	T _{STG}	-30	+80	°C
Humidity	RH	--	90	%

4. Electrical Characteristics

4.1 TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage for I/O	VDDIO	1.65	1.8	3.3	V
Supply Voltage for(DC/DC)	VDD	2.6	3.3	3.6	V
Current Consumption	I _{DD}	--	--	--	mA
	I _{DD-SLEEP}	--	--	--	uA

4.2 Back-Light Unit Characeristics

The back-light system is an edge-lighting type with 18 white LEDs. The characteristics of the back-light are shown in the following tables.

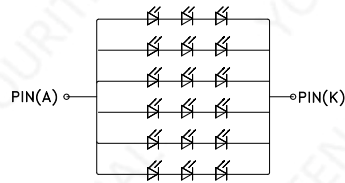
Characteristics	Symbol	Min.	Type	Max.	Unit	Notes
Forward Voltage	V _F	16.8	--	19.2	V	--
Forward current	I _F	--	120	--	mA	--
Luminance(With LCD+CTP)	L _v	--	800	--	cd/m ²	--
LED life time	N/A	--	20,000	--	Hr	Note 1

Note:

- (1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=20mA/LED. The LED life time could be decreased if operating I_L is larger than 25mA/LED.

Backlight circuit diagram shown in below:





5. Module Function Description

Pin No.	Symbol	LCM Functional	Notes
1	GND	Power Ground	
2	MIPI D0+	High speed interface data differential signal input/output pins	
3	MIPI D0-	High speed interface data differential signal input/output pins	
4	GND	Power Ground	
5	MIPI D1+	High speed interface data differential signal input/output pins	
6	MIPI D1-	High speed interface data differential signal input/output pins	
7	GND	Power Ground	
8	MIPI CLK+	High speed interface clock differential signal input/output pins	
9	MIPI CLK-	High speed interface clock differential signal input/output pins	
10	GND	Power Ground	
11	MIPI D2+	High speed interface data differential signal input/output pins	
12	MIPI D2-	High speed interface data differential signal input/output pins	
13	GND	Power Ground	
14	MIPI D3+	High speed interface data differential signal input/output pins	
15	MIPI D3-	High speed interface data differential signal input/output pins	
16~17	GND	Power Ground	
18~19	VCC 1.8V	power supply for the I/O circuit	
20~23	NC	NC	
24	RESET	Reset pin. Setting either pin low initializes the LSI	
25~26	NC	NC	
27	GND	Power Ground	
28~29	LEDK	Power supply for backlight cathode input terminal.	
30	GND	Power Ground	
31	NC	NC	
32~33	GND	Power Ground	
34	NC	NC	
35~36	LEDA	Power supply for backlight anode input terminal.	
37	GND	Power Ground	
38~39	VDD 3.3V	power supply for DC/DC circuit	
40	NC	NC	

CTP PIN Description:

Pin No.	Symbol	CTP Functional	Notes
1	CTP_VCC2.8V	Touch panel Power supply 2.8~3.3V	
2	CTP_INT 1.8V	Touch panel interrupt output	
3	CTP_RST 1.8V	Touch panel reset	
4	CTP_SCL 1.8V	Touch panel I2C clock	
5	CTP_SDA 1.8V	Touch panel I2C data	
6	GND	Power Ground	



6. Timing Characteristics

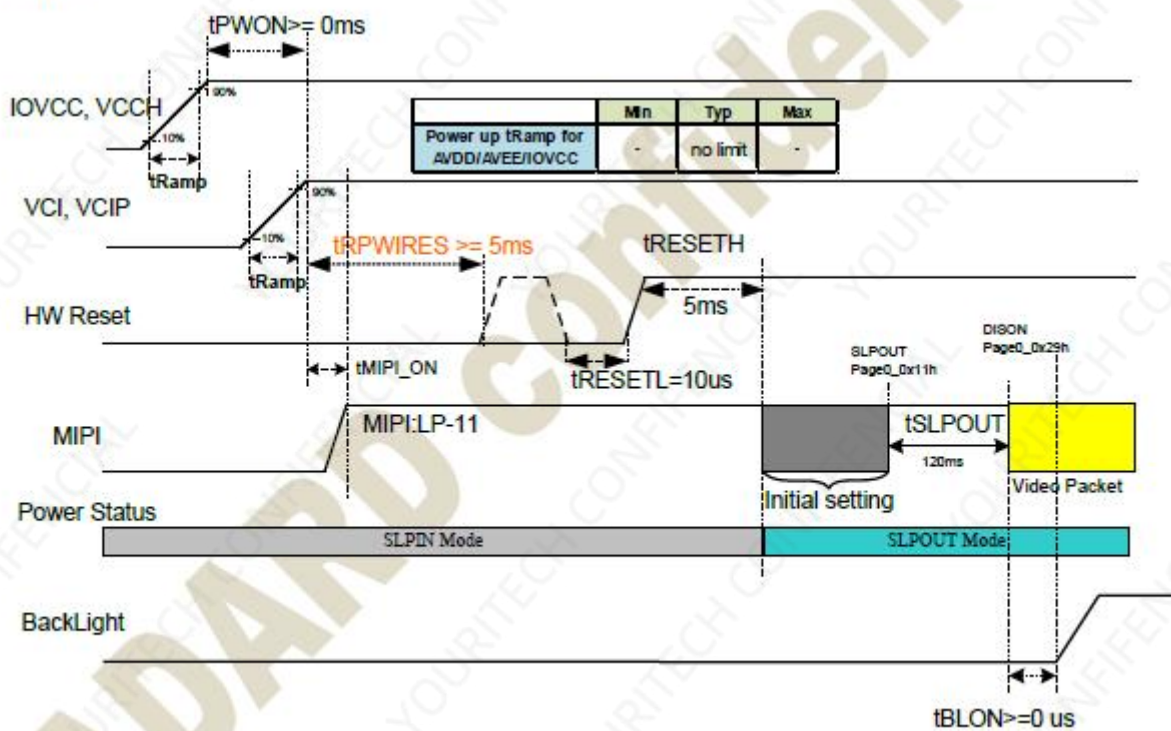
Power on sequence for differential power mode

Symbol	Min	Typ	Max	Unit	Remark
tRamp	-	no limit	-	us	
tPWON	0	-	-	ms	
tON1	0	-	-	ms	
tMIPI-ON	0	-	tRPWIRES	ms	
tRPWIRES	5	-	-	ms	
tRESETL	10	-	-	us	
tRESETH	5	-	-	ms	
tSLPOUT	120	-	-	ms	
tBLON	0	-	-	ms	

BOOSTM[1:0]=10 (Internal DC/DC power mode : Charge Pump, FP7721)

VCCD=IOVCC=VCCH=1.65V ~ 3.6V, VCI=VCIP=2.5V ~ 4.8V.

Power on:



Burst Mode Data Transmission

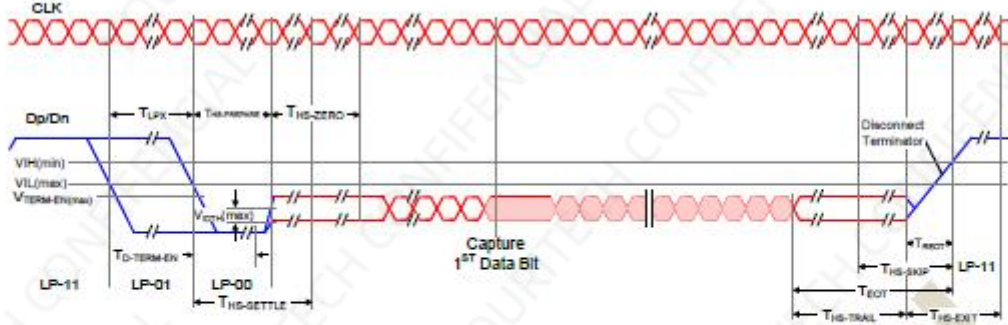


Figure 11.7: High-Speed Data Transmission in Bursts

Parameter	Description	Min	Typ	Max	UNIT
T_{LPX}	Transmitted length of any Low-Power state period	50	-	-	ns
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	$40 + 4 \cdot UI$	-	$85 + 6 \cdot UI$	ns
$T_{HS-PREPARE} + T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	$145 + 10 \cdot UI$	-	-	ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination.	-	-	$35 + 4 \cdot UI$	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions.	$85 + 6 \cdot UI$	-	$145 + 10 \cdot UI$	ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	$\max(n \cdot 8 \cdot UI, 60 + n \cdot 4 \cdot UI)$	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns



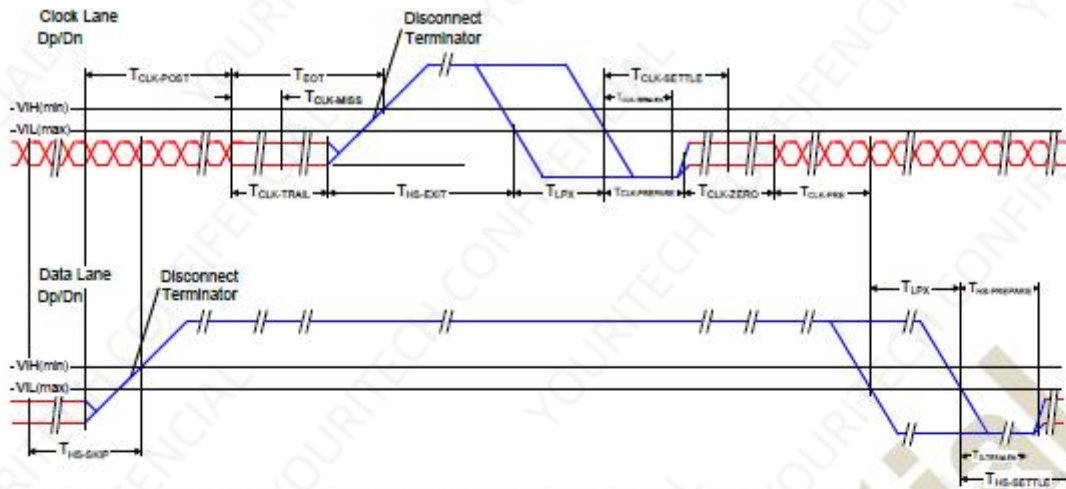


Figure 11.8: Switching the Clock Lane between Clock Transmission and Low-Power Mode

Parameter	Description	Min	Typ	Max	UNIT
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode.	$60 + 52 \cdot UI$	-	-	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	$8 \cdot UI$	-	-	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38	-	95	ns
$T_{CLK-PREPARE} + T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300	-	-	ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination.	-	-	38	ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns



Reset input timings

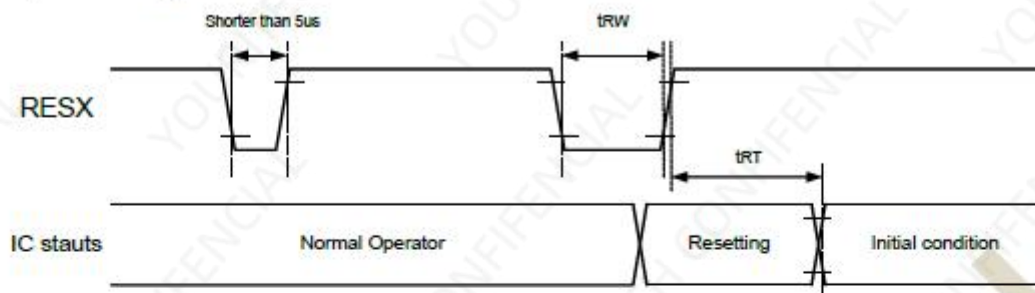


Figure 11.1: Reset input timings

Symbol	Parameter	Related pins	Min.	Max.	Unit
t_{RW}	Reset pulse width ⁽²⁾	RESX	10	-	μ s
t_{RT}	Reset complete time ⁽³⁾	-	-	5 (Note 5)	ms
		-	-	120 (Note 6, 7)	ms

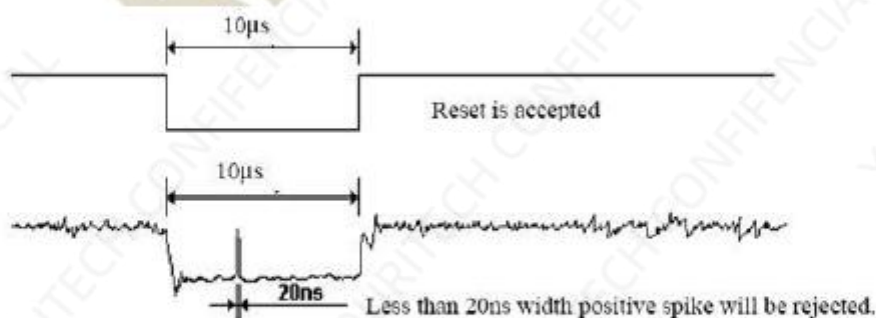
Note: (1) The reset complete time also required time for loading ID bytes from OTP to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

(2) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5 μ s	Reset Rejected
Longer than 10 μ s	Reset
Between 5 μ s and 10 μ s	Reset Start

(3) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for H/W reset.

(4) Spike Rejection also applies during a valid reset pulse as shown below:



(5) When Reset is applied during Sleep In Mode.

(6) When Reset is applied during Sleep Out Mode.

(7) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

(8) After Sleep Out Command, it is necessary to wait 120msec then send RESX.

Table 11.3: Reset timings



7. Optical Characteristics

Item		Specification	Unit	Note
Screen Size		6.95	inch	-
Shipping size		Cut : 1109.92 (H) x 644.72 (V) x 0.4(D)	mm	
Cell Outline Dimension		93.28(H)x 159.82(V)x 0.4(D)	mm	
Active Area		89.28 (H)x 152.3712(V)	mm	
Driver Element		a-Si TFT active matrix	-	-
Cell Transmittance		5.0%(Typ) 4.5%(Min)	-	Center point at C-Light
Pixel Number		600(RGB) x 1024	pixel	-
Pixel Pitch		148.8(H) x 148.8(V)	um	-
Pixel Arrangement		RGB stripe	-	-
Display Mode		Normally Black	-	-
Response Time		30 (Typ.) 35(Max.)	ms	
Contrast Ratio		1000:1(Typ);800:1(Min)		
View Angle		L/R/U/D:85/85/85/85(Typ.)		
Driver IC		ICNL9707	-	
		FL7703NI/JD9365DA/HX8394F /IL19881C/ ER88577B		Compatibility
Operation Temperature		-20~70	°C	
Storage Temperature		-30~80	°C	
Chromaticity	NTSC Ratio	50% (Typ.) 45% (Min.)		Only CF Under C-light
	White	(0.302±0.03,0.342±0.03)		
	R			
	G			
	B			
Weight		1369.9 _1/8 Cut	g	Q panel

1. The color chromaticity coordinates specified shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

2. Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression,

$$\text{Contrast Ratio (CR): } CR = \frac{CR_w}{CR_D}$$

CR_w : Luminance of LCD module with full screen white pattern (255,255, 255) at center point.



CR_D : Luminance of LCD module with full screen Dark pattern (0, 0, 0) at center point.

Where the measure point of to the Contrast Ratio is the center of the panel.

1. Definition of Response time (T_g):

Measured response time is determined by 10% to 90% brightness difference of rising (T_R) and falling (T_F) time.

2. The test backlight spectrum is as follows

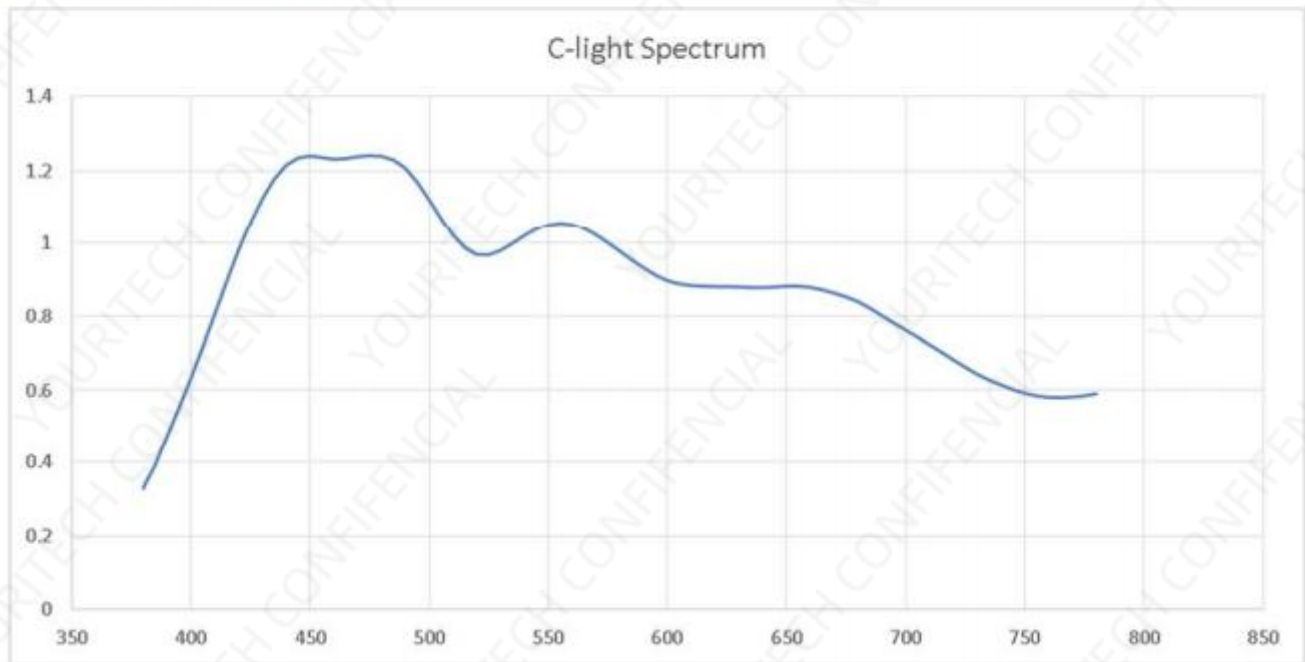


Figure 1: C light spectrum

8. Reliability Test Item

No.	Test Item	Test Condition	Notes
1	High Temp. Storage	+80°C / 96H	1. Functional test is OK. Missing Segment, short, unclear segment non-display, display abnormally and liquid crystal leakage un-allowed. 2. No low temperature bubbles, end seal loose and fall, frame rainbow.
2	Low Temp. Storage	-30°C / 96H	
3	High Temp. Operating	+70°C / 96H	
4	Low Temp. Operating	-20°C / 96H	
5	High Temperature / Humidity storage	50°C x 90%RH / 96H	
6	Thermal and cold shock	Static state, -20°C (30min) ~60°C (30min), 10 cycles	

9. Packing Method----TBD

- END -

