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Project No. 项目编号	ET070WU01-TT
Customer 客户名称	
Module No. 客户型号	
Product type 产品内容	**Standard LCD Module** **TFT：1200*RGBx1920Dots** **7.02”TFT LCD + CTP**

客户确认Customer Approval	
项目负责人Project Manager	
品质主管Director of Quality	
采购工程师Purchasing Engineer	

PREPARED BY	CHECKED BY	APPROVED BY

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1. Introduction

1.1 Scope of application

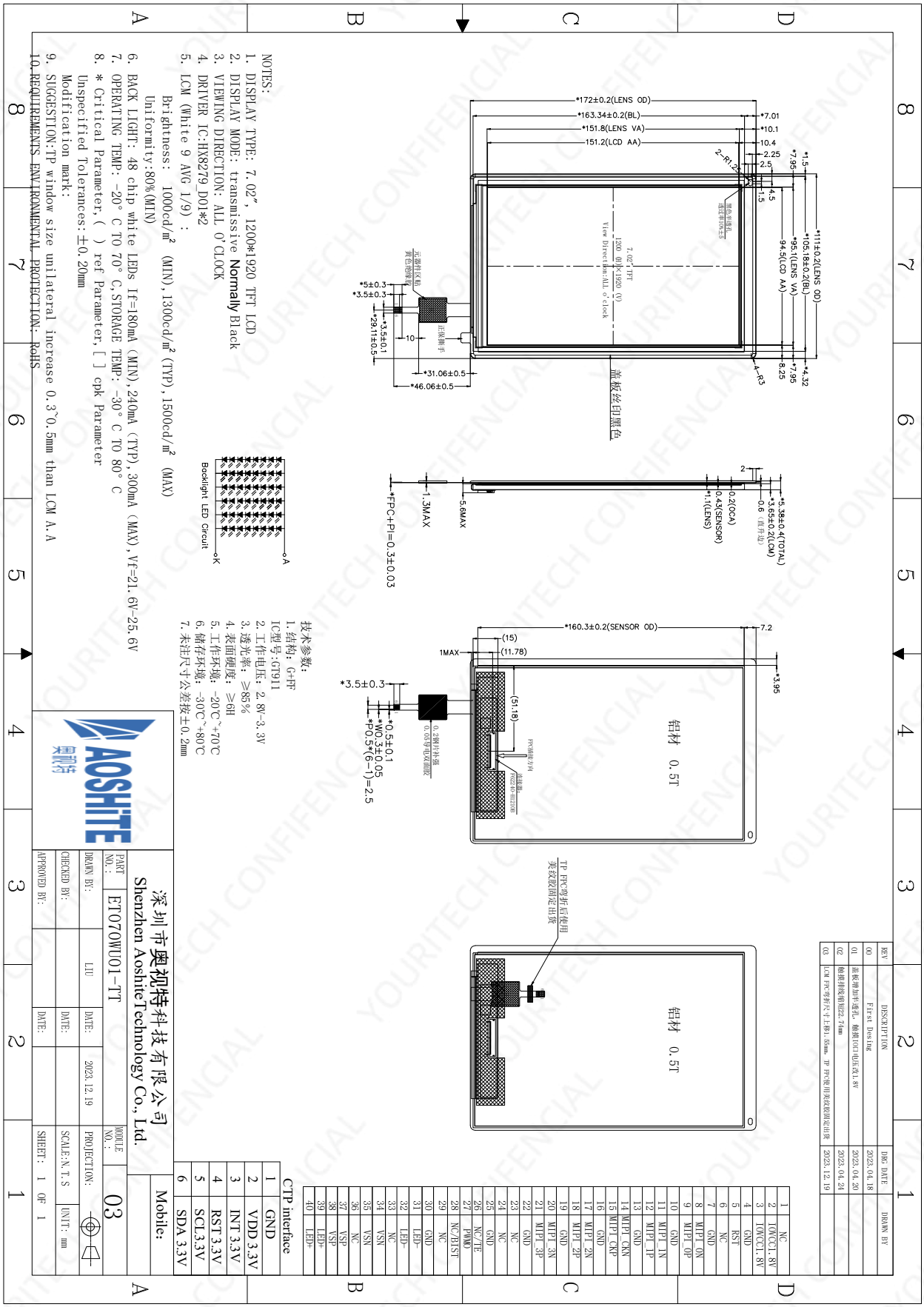
This specification applies to the LCD module that is supplied by Aoshite Technology CO., LTD.
LCD specification: Dots 1200xRGBx1920
As to basic specification of the driver IC, refer to the IC (HX8279-D01x2) specification and data book.
All material & processing of the LCD module should be Lead Free.

1.2 TFT features:

Structure: TFT PANNEL+IC +FPC+BL+CTP;
ALL Viewing Type LCD
1200 dot-segment and 1920 dot-common outputs;
16.7M Color can be selected by software;
White LED back light;
4lane MIPI interface

2. LCM General specification

ITEM	Sandard value	Unit
LCD Type	Normally Black	--
Drive element	TFT active matrix	--
Number of pixels	1200*3RGB(H)X1920(V)	Dots
Pixel arrangement	RGB Vertical Stripe	--
Pixel Pitch (W*H)	0.07875(H) X 0.07875(V)	mm
Active area	94.50(H) x 151.20(V)	mm
Viewing direction	ALL O'CLOCK	--
TFT Driver IC	HX8279-D01x2	--
TFT interface	4lane MIPI interface	--
Approx. Weight	TBD	g
LCM Size(W*H*T)	105.18(W) ×163.34(H) ×3.65(T)	mm
LCM+CTP Size(W*H*T)	111.00(W) ×172.00(H) ×5.38(T)	mm
Touch structure	G+FF	--
Touch Driver IC	GT911	--
Touch Interface	I2C	--



NOTES:
1. DISPLAY TYPE: 7.02", 1200*1920 TFT LCD
2. DISPLAY MODE: transmissive Normally Black
3. VIEWING DIRECTION: ALL O'CLOCK
4. DRIVER IC:HX8279_D01*2
5. LCM (White 9 AVG 1/9) :
   Brightness: 1000cd/m² (MIN),1300cd/m² (TYP),1500cd/m² (MAX)
   Uniformity:80%(MIN)
6. BACK LIGHT: 48 chip white LEDs If=180mA (MIN),240mA (TYP),300mA (MAX),Vf=21.6V~25.6V
7. OPERATING TEMP: -20° C TO 70° C,STORAGE TEMP: -30° C TO 80° C
8. * Critical Parameter,( ) ref Parameter,[ ] cpk Parameter
   Unspecified Tolerances:±0.20mm
   Modification mark:
9. SUGGESTION:TP window size unilateral increase 0.3~0.5mm than LCM A.A
10. REQUIREMENTS ENVIRONMENTAL PROTECTION: RoHS

技术参数:
1. 结构: G+FF
IC型号:GT911
2. 工作电压: 2.8V~3.3V
3. 透光率: ≥85%
4. 表面硬度: ≥6H
5. 工作环境: -20℃~+70℃
6. 储存环境: -30℃~+80℃
7. 未注尺寸公差按±0.2mm

REV	DESCRIPTION	DRG DATE	DRAWN BY
00	First Design	2023.04.18	
01	盖板增加异形孔、触摸IC由5V改1.8V	2023.04.20	
02	触摸排线铜箔22.7mm	2023.04.24	
03	LCM FPC弯折尺寸上移1.55mm，TP FPC使用美纹胶固定出货	2023.12.19	

NO.	CTP interface
1	GND
2	VDD 3.3V
3	INT 3.3V
4	RST 3.3V
5	SCL3.3V
6	SDA 3.3V

NO.		NO.	
1	NC	21	MIPI_3P
2	10V/CCL_8V	22	GND
3	10V/CCL_8V	23	NC
4	GND	24	NC
5	RST	25	GND
6	NC	26	NC/TE
7	GND	27	PWM
8	MIPI_ON	28	NC/BIST
9	MIPI_OP	29	NC
10	GND	30	GND
11	MIPI_1N	31	LED-
12	MIPI_1P	32	LED-
13	GND	33	NC
14	MIPI_CKN	34	VSN
15	MIPI_CKP	35	VSN
16	GND	36	NC
17	MIPI_2N	37	VSP
18	MIPI_2P	38	VSP
19	GND	39	LED+
20	MIPI_3N	40	LED+

深圳市奥视特科技有限公司
Shenzhen Aoshite Technology Co., Ltd.

PART NO.:	ET070WU01-TT	MODULE NO.:	03
DRAWN BY:	LIU	DATE:	2023.12.19
CHECKED BY:		DATE:	
APPROVED BY:		DATE:	
PROJECTION:		SCALE:N.T.S	
UNIT: mm		SHEET: 1 OF 1	

Mobile:

3.Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
LCM Operating Temperature	T_{OPR}	-20	+70	°C
LCM Storage Temperature	T_{STG}	-30	+80	°C
TP Operating Temperature & Humidity(20% ~ 90%RH)	T_{OPR}	-20	+70	°C
TP SStorage Temperature & Humidity(20% ~ 90%RH)	T_{STG}	-30	+80	°C
Humidity	RH	--	90	%

4.Electrical Characteristics

4.1 TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage for I/O	VDDIO	1.7	1.8	2.0	V
Supply Voltage for VSP	VSP	4.5	5.5	6	V
Supply Voltage for VSN	VSN	-6	-5.5	-4.5	V

4.2 Back-Light Unit Characeristics

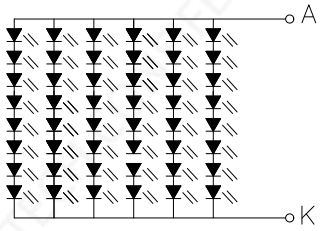
The back-light system is an edge-lighting type with 48 white LEDs. The characteristics of the back-light are shown in the following tables.

Characteristics	Symbol	Min.	Type	Max.	Unit	Notes
Forward Voltage	V_F	21.6	--	25.6	V	--
Forward current	I_F	180	240	300	mA	--
Luminance(With LCD+CTP)	Lv	1000	1300	1500	cd/m^2	--
LED life time	N/A	--	20,000	--	Hr	Note 1

Note:

(1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=40mA/LED. The LED life time could be decreased if operating I_L is larger than 45mA/LED.

Backlight circuit diagram shown in below:



5. Module Function Description

5. Module Function Description

Pin No.	Symbol	Functional	Notes
1	NC	No Connection.	
2	IOVCC 1.8V	Power Supply For I/O.	
3	IOVCC 1.8V	Power Supply For I/O.	
4	GND	Power Ground	
5	RST	Reset Signal input pin.	
6	NC	No Connection.	
7	GND	Power Ground	
8	MIPI_0N	High speed interface data differential signal input/output pins	
9	MIPI_0P	High speed interface data differential signal input/output pins	
10	GND	Power Ground	
11	MIPI_1N	High speed interface data differential signal input/output pins	
12	MIPI_1P	High speed interface data differential signal input/output pins	
13	GND	Power Ground	
14	CLKN	High speed interface clock differential signal input/output pins	
15	CLKP	High speed interface clock differential signal input/output pins	
16	GND	Power Ground	
17	MIPI_2N	High speed interface data differential signal input/output pins	
18	MIPI_2P	High speed interface data differential signal input/output pins	
19	GND	Power Ground	
20	MIPI_3N	High speed interface data differential signal input/output pins	
21	MIPI_3P	High speed interface data differential signal input/output pins	
22	GND	Power Ground	
23	NC	No Connection.	
24	NC	No Connection.	
25	GND	Power Ground	
26	NC/TE	No Connection.	
27	PWMO	PWM (Pulse Width Modulation) Signal Of LED Driving.	
28	NC/BIST	No Connection.	
29	NC	No Connection.	
30	GND	Power Ground	
31	LEDK	Power supply for backlight cathode input terminal.	
32	LEDK	Power supply for backlight cathode input terminal.	

33	NC	No Connection.	
34	VSN	External input voltage（-4.5V~ -6V）	
35	VSN	External input voltage（-4.5V~ -6V）	
36	NC	No Connection.	
37	VSP	External input voltage（4.5V~ 6V）	
38	VSP	External input voltage（4.5V~ 6V）	
39	LEDA	Power Supply For LED Backlight Anode Input.	
40	LEDA	Power Supply For LED Backlight Anode Input.	

CTP PIN Description:

Pin No.	Symbol	CTP Functional	Notes
1	GND	Power Ground	
2	CTP_VCC 3.3V	Touch panel Power supply	
3	CTP_INT 3.3V	Touch panel interrupt output	
4	CTP_RST 3.3V	Touch panel reset	
5	CTP_SCL 3.3V	Touch panel I2C clock	
6	CTP_SDA 3.3V	Touch panel I2C data	

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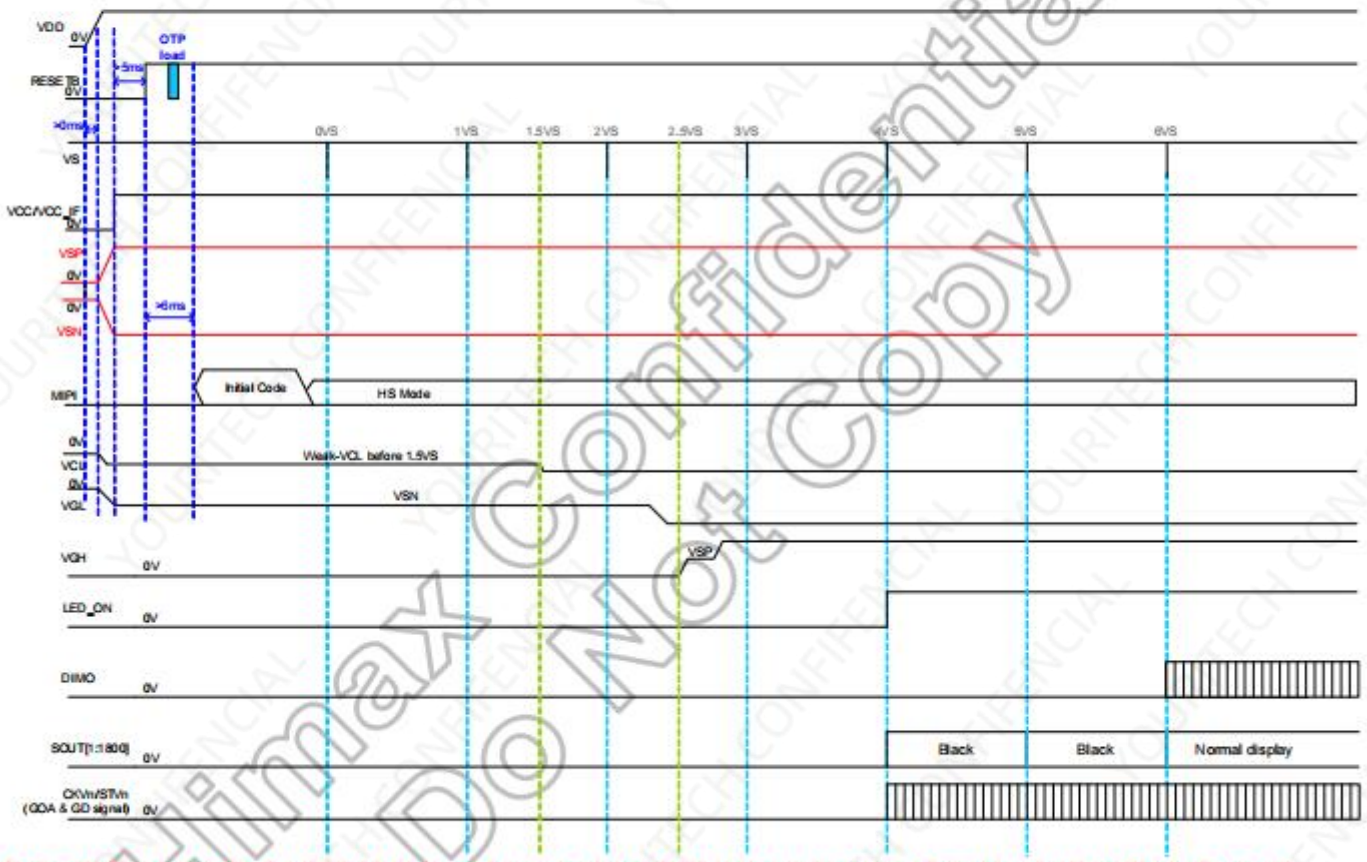
6. Timing Characteristics

Power on sequence PWRMD=0 ➔ max. Power on time=7VS

After reset state or exit STB mode, the power on sequence will start.

To prevent the device from damage due to latch up, The VGL will be earlier than VGH. At 2.25VS the VGL negative high voltage will be generated via the external charge pump circuit. Then at 2.5VS the VGH positive high voltage can be generated via the external charge pump circuit. One SCHOTTKY diode is necessary between VGL and GND when VDD and VSP start at the same time.



Note: (1) Finish to write the GOA MUX (page1 registers) and GOA timing setting (page3 registers) within 50ms after reset pulls to high.

Figure 5.5: Power on sequence with PWRMD=0 and repair OP disable

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Power off sequence PWRMD=0 ➔ max. Power off time=5VS

When enter STB mode, the STBYB signal will be set to low. The power off sequence will start.

Power-off sequence
External VSP/VSN. Internal VGH/VGL.

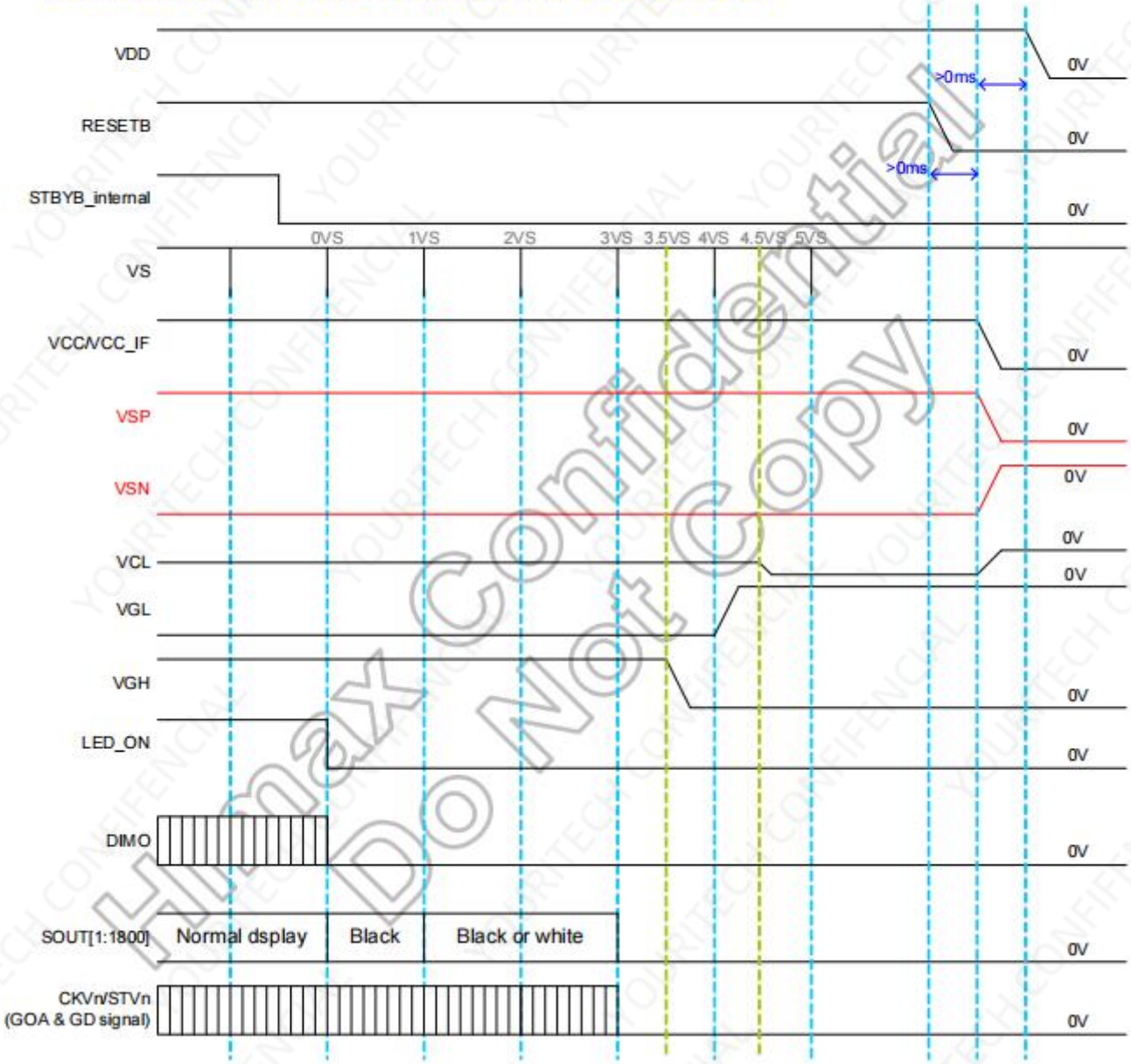

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Figure 5.6: Power off sequence with PWRMD=0

MIPI AC characteristics

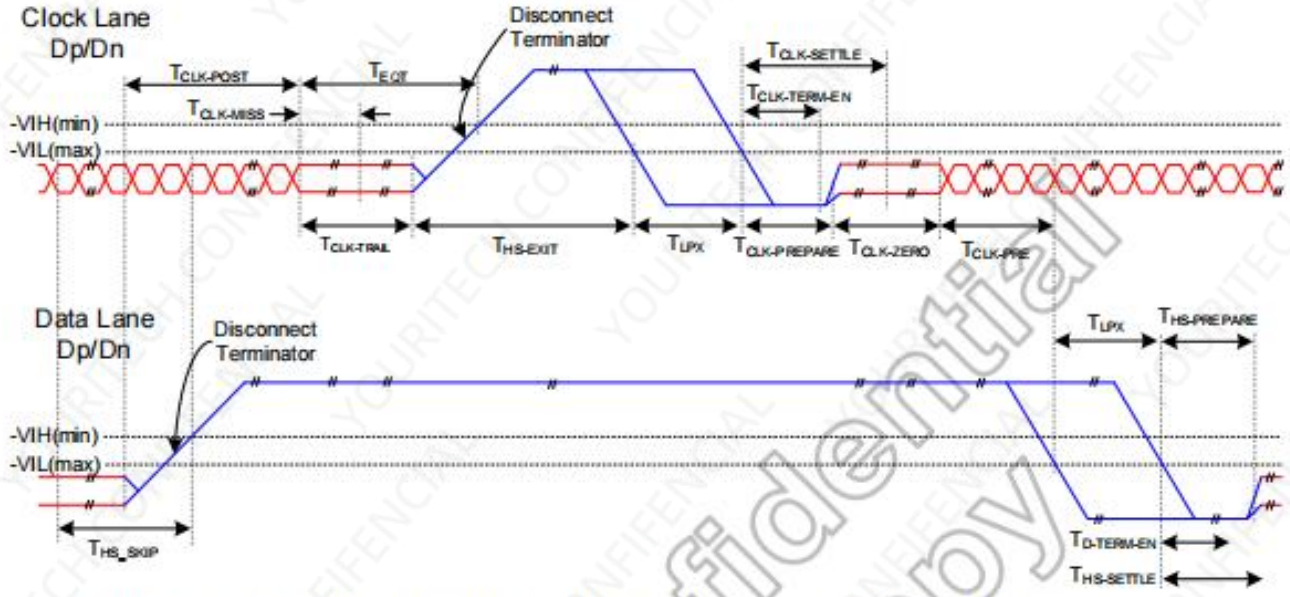

Figure 13.1: Switching the clock lane between clock transmission and low-power mode

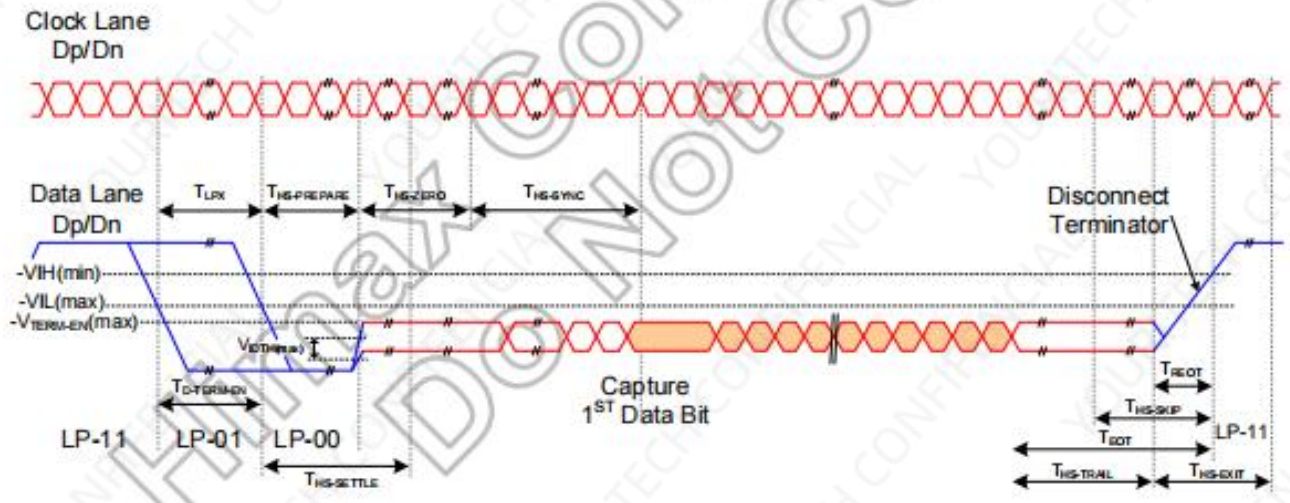

Figure 13.2: Timing of high-speed data transmission in bursts

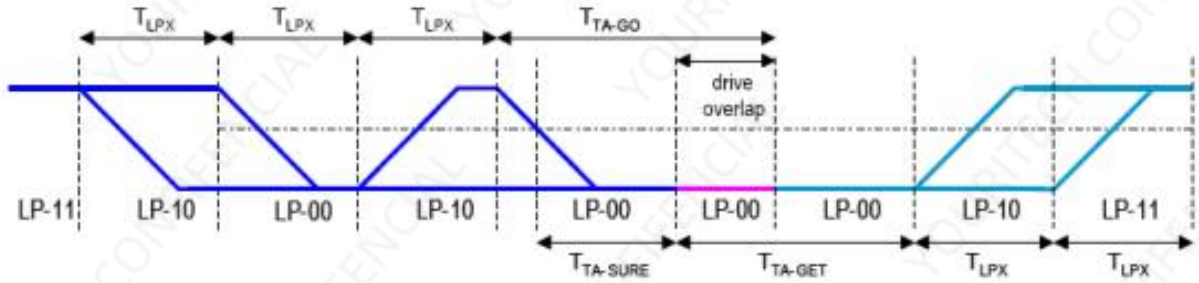

Figure 13.3: Turnaround Procedure

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MIPI AC Characteristics

Parameter	Description	Spec.			Unit
		Min.	Typ.	Max.	
T_{REOT}	30%-85% rise time and fall time	-	-	35	ns
$T_{CLK-MISS}$	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.	-	-	60	ns
$T_{CLK-POST}$*1	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of $T_{CLK-TRAIL}$.	60 ns + 52*UI **(For DCS)**	-	-	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8	-	-	ns
$T_{CLK-SETTLE}$	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of $T_{CLK-PRE}$.	95	-	300	ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$	-	38	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $T_{HSPREPARE}$.	85 ns + 6*UI		145 ns + 10*UI	ns
T_{EOT}	Time from start of $T_{HS-TRAIL}$ or $T_{CLK-TRAIL}$ period to start of LP-11 state	-	-	105ns+48*UI	-
$T_{HS-EXIT}$ (1)	time to drive LP-11 after HS burst	100	-	-	ns
$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40ns + 4*UI	-	85ns+6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + Time to drive HS-0 before the Sync sequence	145ns + 10*UI	-	-	ns
$T_{HS-SKIP}$	Time-out at RX to ignore transition period of EoT	40	-	55ns+4*UI	ns
$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60 + 4*UI	-	-	ns
T_{LPX}	Length of any Low-Power state period	50	-	-	ns
Ratio T_{LPX}	Ratio of $T_{LPX(MASTER)}$/$T_{LPS(SLAVE)}$ between Master and Slave side	2/3	-	3/2	-
T_{TA-GET}	Time to drive LP-00 by new TX	$5*T_{LPX}$			ns
T_{TA-GO}	Time to drive LP-00 after Turnaround Request	$4*T_{LPX}$			ns
$T_{TA-SURE}$	Time-out before new TX side starts driving	T_{LPX}	-	$2*T_{LPX}$	ns

Note: (1) For image transmission:
$T_{CLK-POST}$ min value =164 when MIPI max frequency per lane = 0.53Gbps.
$T_{CLK-POST}$ min value =112 when MIPI max frequency per lane = 1Gbps

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MIPI data-clock timing specification

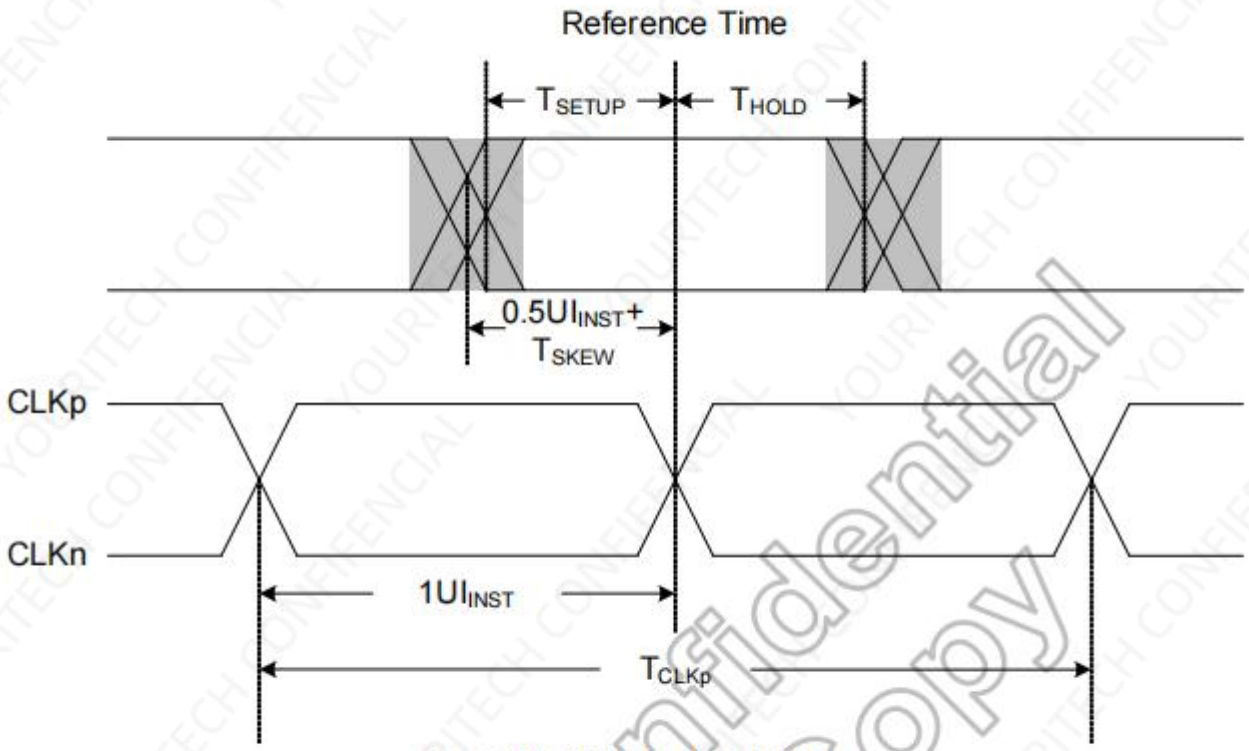

Figure 13.4: Data to clock timing

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
UI instantaneous	UI_{INST}	1.0	-	12.5(1)	ns
Data to clock setup time	T_{SETUP}	0.3	-	-	UI_{INST}
Data to clock hold time	T_{HOLD}	0.3	-	-	UI_{INST}

Note: (1) This value corresponds to a minimum 80 Mbps data rate.

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Timing requirements for RESETB

When RESETB of the reset pin equals to Low, it will be in the condition of reset. When it is in the condition of reset, it will make the device recover the initial set.

However, in order to avoid the reset noise cause reset, there is a mechanism to judge about whether the reset is needed or not.

The closed interval of low can be shown as the following.

(VDD=1.7V~2.0V, VSS=0V, T_A=-20℃~+85℃)

Parameter	Symbol	Conditions	Spec. Min.	Spec. Typ.	Spec. Max.	Unit
Reset low pulse width	Trst	-	20	-	-	μs

Table 13.5: Reset timing

Figure 13.6: Reset timing

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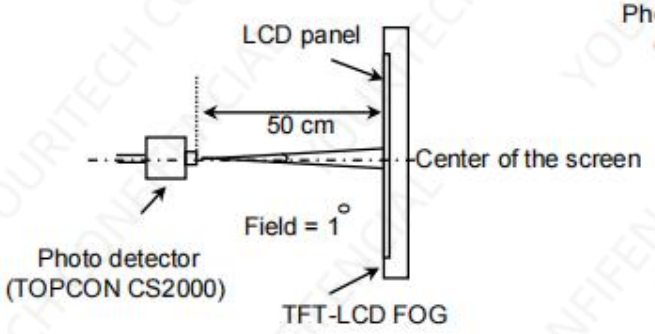
7. Optical Characteristics

Optical Specification

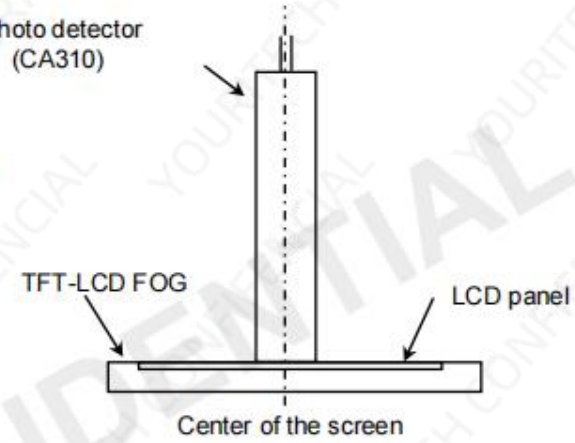
Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle Range	Horizontal	Θ_3	CR > 10	75	80	-	Deg.	Note 6.1
		Θ_9		75	80	-	Deg.	
	Vertical	Θ_{12}		75	80	-	Deg.	
		Θ_6		75	80	-	Deg.	
Contrast Ratio		CR	Θ = 0°	1000	1200	-		HC+APF @silicate BLU Note 6.2/6.3
Cell Transmittance		Tr		3.05	3.6	-	%	
Reproduction of color		Rx	Θ = 0°					CF @C Light Note 6.4
		Ry						
		Gx						
		Gy						
		Bx						
		By						
		Wx		0.265	0.285	0.305		
		Wy		0.299	0.319	0.339		
Color Gamut			Θ = 0°	75	80	-	%	
Response Time		Tr+Tf	Ta= 25°C Θ = 0°	-	30	40	ms	Note 6.5

Note 1: Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see Figure 6).

<Figure 6. Viewing Angle Range Is Defined As Follows>



View angel range, uniformity, etc. measurement setup



Flicker, measurement setup

Note 2: Contrast measurements shall be made at viewing angle of Θ=0° and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

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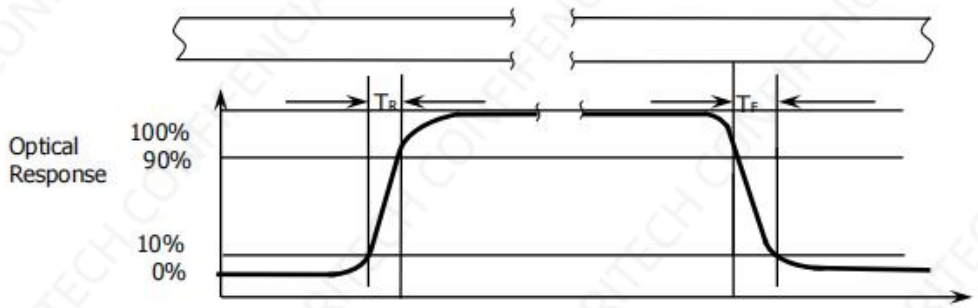
Note 3 : The color chromaticity coordinates specified in Table 5 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

Note 6.5: The electro-optical response time measurements shall be made as Figure 7 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Tf.

<Figure 7. Response Time Testing>



8. Reliability Test Item

No.	Test Item	Test Condition	Notes
1	High Temp. Storage	+80°C / 96H	1. Functional test isOK. Missing Segment,short, unclear segment non-display,display abnormally and liquid crystal leakare un-allowed. 2. No low temperature bubbles,end seal loose andfall, frame rainbow.
2	Low Temp. Storage	-30°C / 96H	
3	High Tempe. Operating	+70°C / 96H	
4	Low Tempe. Operating	-20°C / 96H	
5	High Temperature /Humidity storage	60°C x 90%RH /96H	
6	Thermal and cold shock	Static state， -20℃（30min）~70℃（30min），10 cycles	

9. Packing Method----TBD