

INDUSTRIAL STRENGTH... Start Your Application From YOURITECH

Integration support

Obsolescence Management

PCAP

Embedded Systems

Human Machine Interface

Touch Solutions

Software

Quality Management

Open Frame Monitors

LCD Controller

Research & Development

Firmware

EMC tests

on-site service

Optical Bonding

In-house Manufacturing

Cover glass

System solutions

OEM Solutions

Custom Display

Production Custom designs Installation

Mechanical design



MODEL NO : ET078HD03-T

MODEL VERSION: 01

SPEC VERSION : 1.0

ISSUED DATE: 2021-09-09

☐ Preliminary Specification

☒ Final Product Specification

Customer : _____

Approved by	Notes

Youri Confirmation

Prepared by	Reviewed by	Approved by
John	Johnny	Wang

1. Introduction

1.1 Scope of application

LCD specification: Dots 400xRGBx1280

As to basic specification of the driver IC, refer to the IC (NV3051F1) specification and data book.

All material & processing of the LCD module should be Lead Free.

1.2 TFT features:

Structure: TFT PANNEL+IC +FPC+BL;

ALL Viewing Type LCD

400 dot-segment and 1280 dot-common outputs;

16.7M Color can be selected by software;

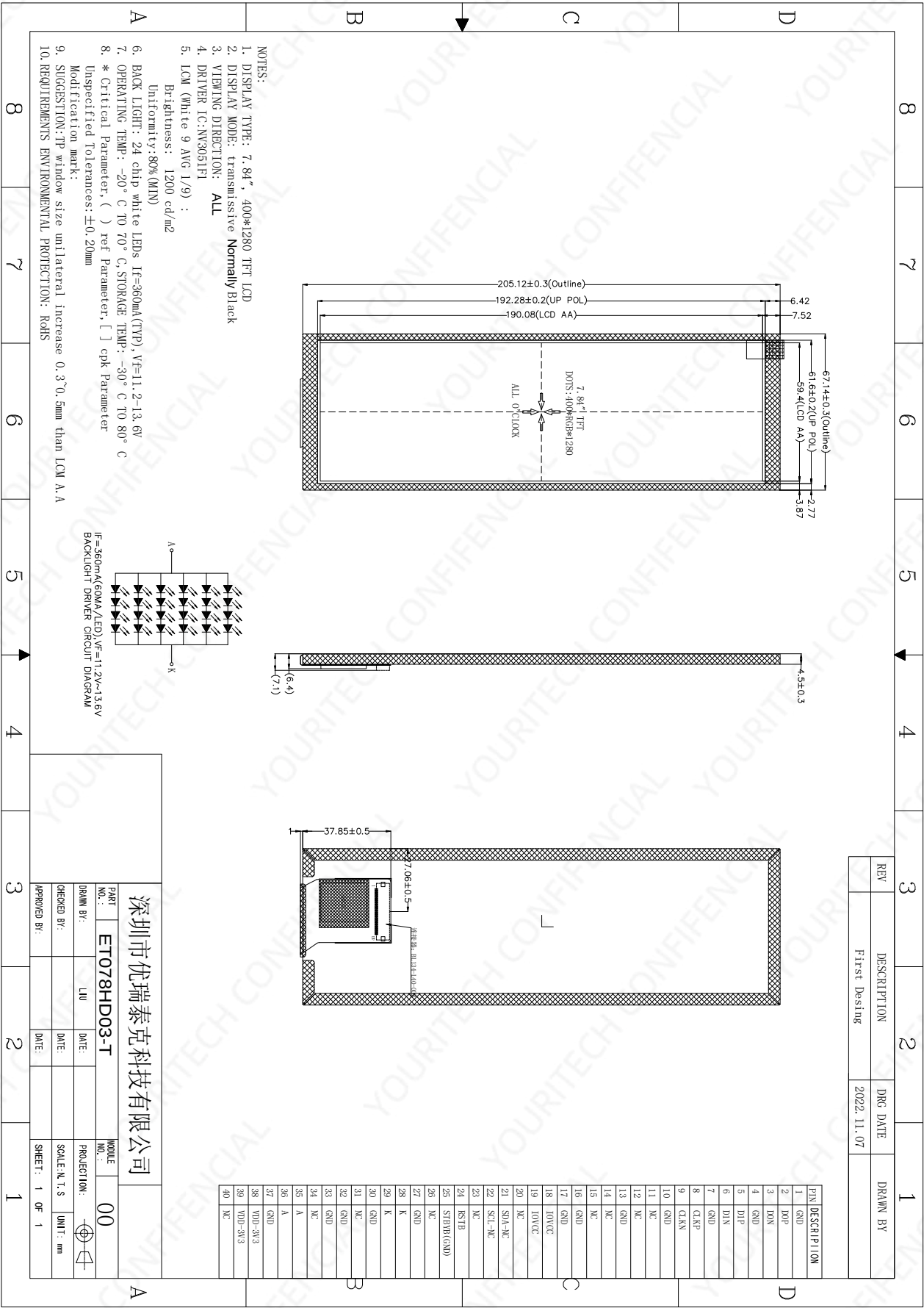
White LED back light;

2lane MIPI interface

1.3 Applications:

2. LCM General specification

ITEM	Standard value	Unit
LCD Type	Normally Black	--
Drive element	TFT active matrix	--
Number of pixels	400*3RGB(H)X1280(V)	Dots
Pixel arrangement	RGB Vertical Stripe	--
Pixel Pitch (W*H)	0.1485(H) X 0.1485(V)	mm
Active area	59.40(H) x 190.08(V)	mm
Viewing direction	ALL O'CLOCK	--
TFT Driver IC	NV3051F1	--
TFT interface	2lane MIPI interface	--
Approx. Weight	TBD	g
LCM Size(W*H*T)	67.14(W) ×205.12(H) ×4.50(T)	mm
Touch structure	--	--
Touch Driver IC	--	--
Touch Interface	--	--



3.Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
LCM Operating Temperature	T _{OPR}	-20	+70	°C
LCM Storage Temperature	T _{STG}	-30	+80	°C
Humidity	RH	--	90	%

4.Electrical Characteristics

4.1 TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage for I/O	VDDIO	1.65	1.8	3.3	V
Supply Voltage for(DC/DC)	VDD	2.7	3.3	3.6	V
Current Consumption	I _{DD}	--	160	--	mA
	I _{DD-SLEEP}	--	100	--	uA

4.2 Back-Light Unit Characteristics

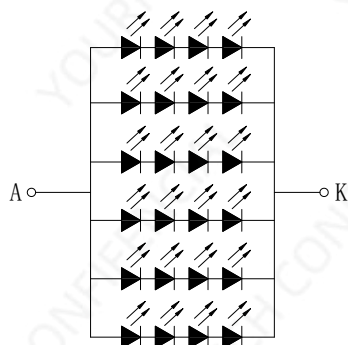
The back-light system is an edge-lighting type with 24 white LEDs. The characteristics of the back-light are shown in the following tables.

Characteristics	Symbol	Min.	Type	Max.	Unit	Notes
Forward Voltage	V _F	11.2	--	13.6	V	--
Forward current	I _F	--	360	--	mA	--
Luminance(With LCD)	L _v	--	1200	--	cd/m ²	--
LED life time	N/A	--	20,000	--	Hr	Note 1

Note:

- (1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=60mA/LED. The LED life time could be decreased if operating I_L is larger than 90mA/LED.

Backlight circuit diagram shown in below:



5. Module Function Description

Pin No.	Symbol	LCM Functional	Notes
1	GND	Power Ground	
2	D0P	MIPI-DSI Data differential signal input pins	
3	D0N	MIPI-DSI Data differential signal input pins	
4	GND	Power Ground	
5	D1P	MIPI-DSI Data differential signal input pins	
6	D1N	MIPI-DSI Data differential signal input pins	
7	GND	Power Ground	
8	CLKP	MIPI-DSI CLOCK differential signal input pins	
9	CLKN	MIPI-DSI CLOCK differential signal input pins	
10	GND	Power Ground	
14-15	NC	NC	
16-17	GND	Power Ground	
18-19	IOVCC	power supply for the I/O circuit (1.65~3.3V)	
20	NC	NC	
21	SDA/NC	NC	
22	SCL/NC	NC	
23	NC	NC	
24	RESET	Reset pin. Setting either pin low initializes the LSI	
25	STBYB(GND)	Power Ground	
26	NC	NC	
27	GND	Power Ground	
28	LEDK	Power supply for backlight cathode input terminal.	

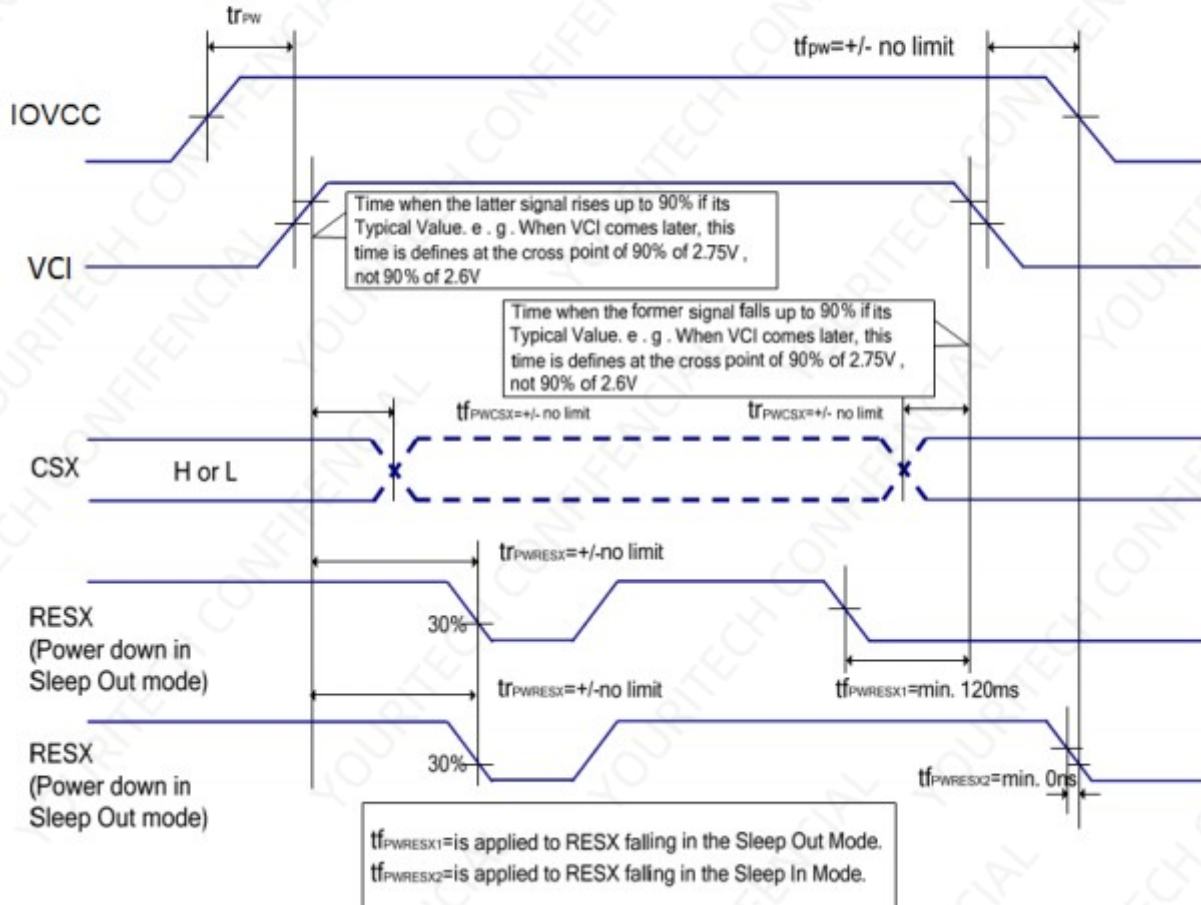
29	LEDK	Power supply for backlight cathode input terminal.	
30	GND	Power Ground	
31	NC	NC	
32	GND	Power Ground	
33	GND	Power Ground	
34	NC	NC	
35	LEDA	Power supply for backlight anode input terminal.	
36	LEDA	Power supply for backlight anode input terminal.	
37	GND	Power Ground	
38	VDD3.3V	power supply for DC/DC circuit(2.7~3.6V)	
39	VDD3.3V	power supply for DC/DC circuit(2.7~3.6V)	
40	NC	NC	

6. Timing Characteristics

Power On/Off Sequence

Case 1 – RESX line is held high or unstable by host at power on

If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and IOVCC have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



High speed mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed Mode						
DSI-CLK+/-	2Xui _{inst}	Double UI instantaneous	2.22	-	25	ns
DSI-CLK+/-	UI _{INSTA} , UI _{INSTB}	UI instantaneous Half's	1.11	-	12.5	ns
DSI-Dn+/-	T _{ds}	Data to clock setup time	0.15	-	-	UI
DSI-Dn+/-	T _{dh}	Data to clock hold time	0.15	-	-	UI
DSI-CLK+/-	T _{drclk}	Differential rise time for clock	150	-	0.3UI	ps
DSI-Dn+/-	T _{drdata}	Differential rise time for data	150	-	0.3UI	ps
DSI-CLK+/-	T _{dfclk}	Differential fall time for clock	150	-	0.3UI	ps
DSI-Dn+/-	T _{dfdata}	Differential fall time for data	150	-	0.3UI	ps

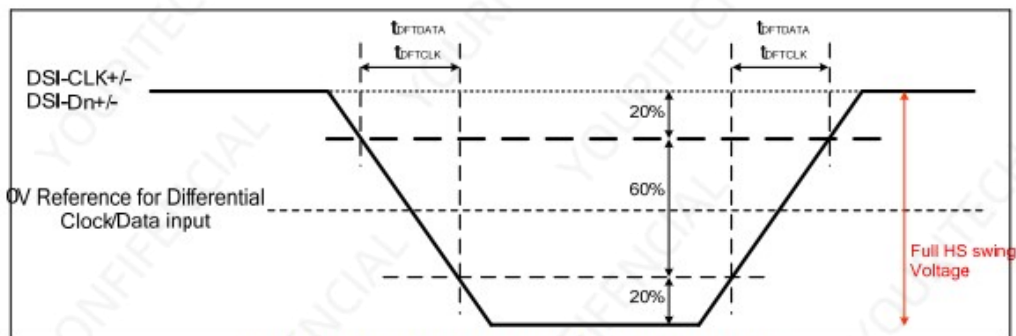
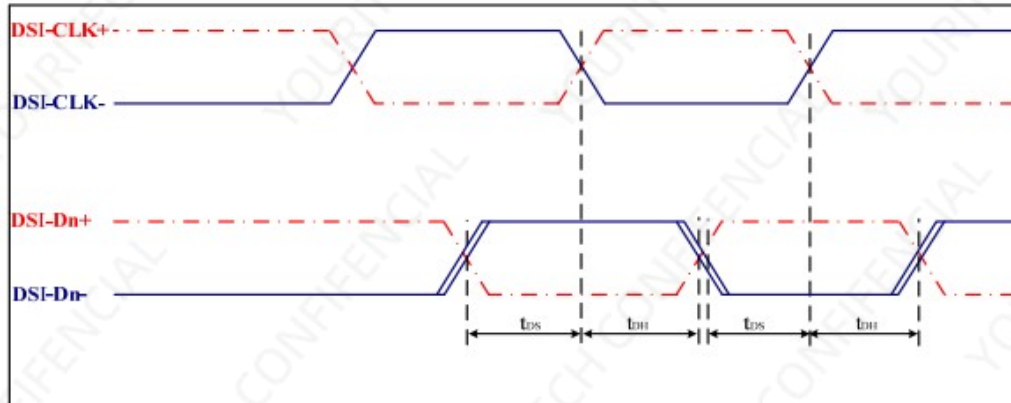
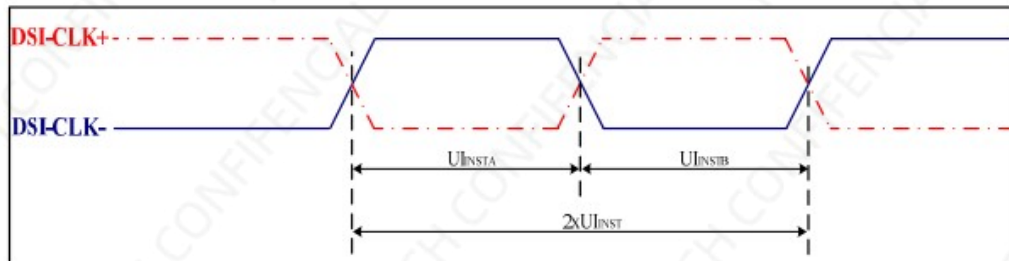


Figure: AC characteristics for MIPI-DSI High speed mode

Low power mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Low Power Mode						
DSI-D0+/-	TLPXM	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU Display Module	50	-	-	ns
DSI- D0+/-	TLPXD	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Modulen MPU	58	-	-	ns
DSI- D0+/-	TTA-SURED	Time-out before the MPU start driving	TLPXD	-	2XTLPXD	ns
DSI- D0+/-	TTA-GETD	Time to drive LP-00 by display module	5XTLPXD	-	-	ns
DSI- D0+/-	TTA-GOD	Time to drive LP-00 after turnaround request – MPU	4XTLPXD	-	-	ns
DSI- D0+/-	Ratio TLPX	Ratio of TLPXM / TLPXD between MCU and display module	2/3	-	3/2	

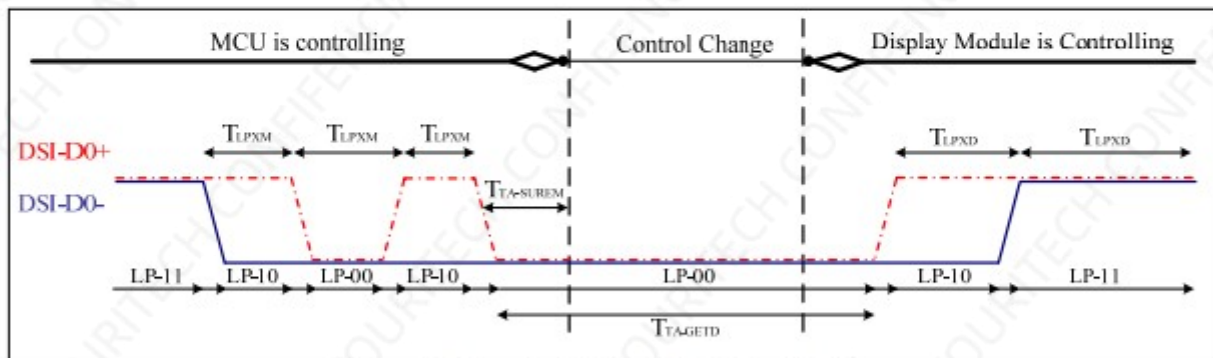


Figure: BTA from the MCU to the Display Module

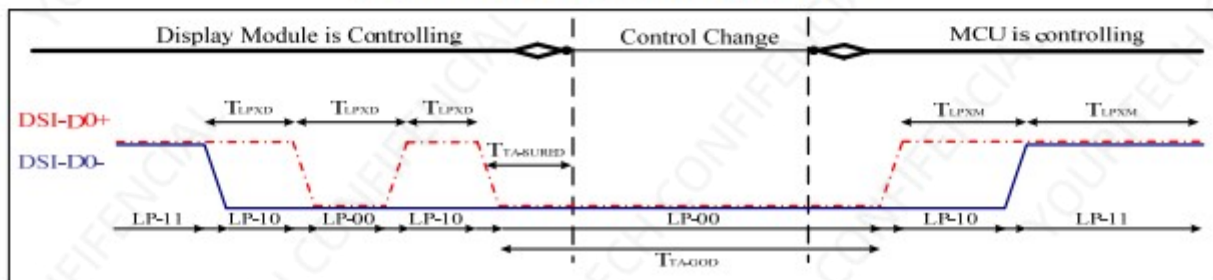


Figure: BTA from the Display Module to the MCU

Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed Data Transmission Bursts						
DSI-Dn+/-	TLPX	Length of any low-power state period	50	-	-	ns
DSI- Dn+/-	THS- PREPARE	Time to drive LP-00 to prepare for HS transmission	40ns+4UI	-	85ns+6UI	ns
DSI- Dn+/-	THS- PREPARE+THS- ZERO	THS-PREPARE+time to drive HS-0 before the sync sequence	145ns+10UI	-	-	ns
DSI- Dn+/-	TD-TERM- EN	Time to enable Data Lane receiver line termination measured from when Dn crosses VIL(max)	Time for Dn to reach VTERM-EN	-	35ns+4UI	ns
DSI- Dn+/-	THS-SKIP	Time-out at RX to ignore transition period of EoT	40	-	55ns+4UI	ns
DSI- Dn+/-	THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	max (8UI, 60ns+4UI)	-	-	ns
DSI- Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	-	ns
DSI- Dn+/-	TeoT	Time from start of THS-TRAIL period to start of LP-11 state	-	-	105ns+12UI	ns

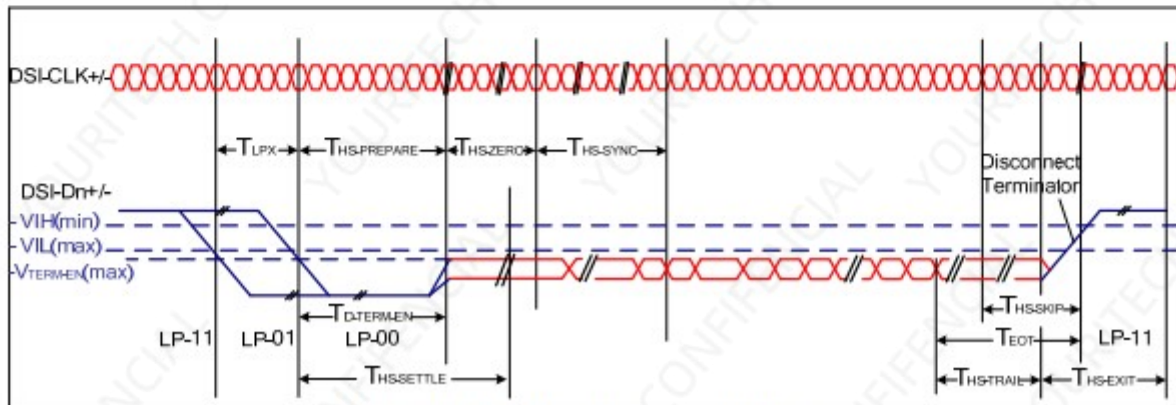


Figure: High Speed Data Transmission Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Switching the clock Lane between clock Transmission and Low Power Mode						
DSI-CLK+/-	TCLK-POST	Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	60ns+52UI	-	-	ns
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8	-	-	UI
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS clock transmission	38	-	95	ns
DSI-CLK+/-	TCLK-TERM- EN	Time to enable Clock Lane receiver line termination measured from when Dn crosses $V_{IL(max)}$	Time for Dn to reach VTERM-EN	-	38	ns
DSI- CLK+/-	TCLK-PREPARE +TCLK-ZERO	TCLK-PREPARE + time for lead HS-0 drive period before starting Clock	300	-	-	ns
DSI- CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns
DSI-CLK+/-	TeoT	Time from start of TCLK-TRAIL period to start of LP-11 state	-	-	105ns+12UI	ns

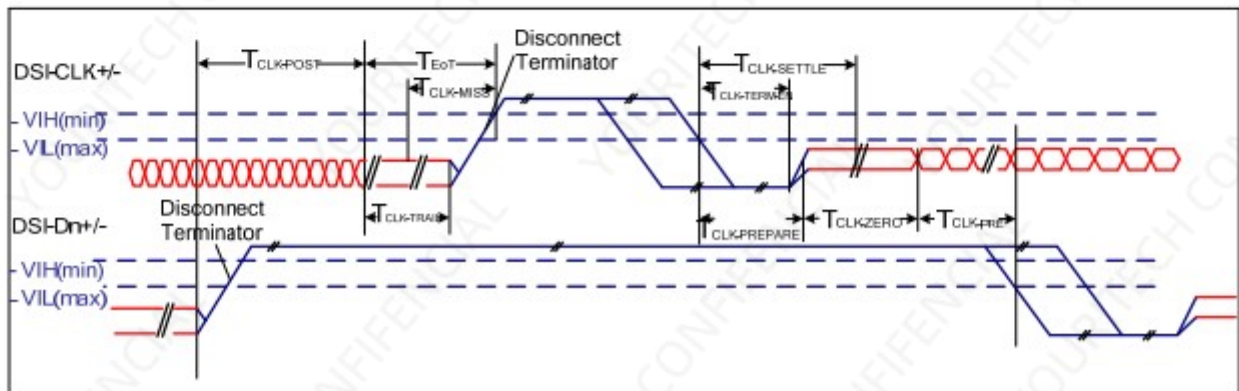
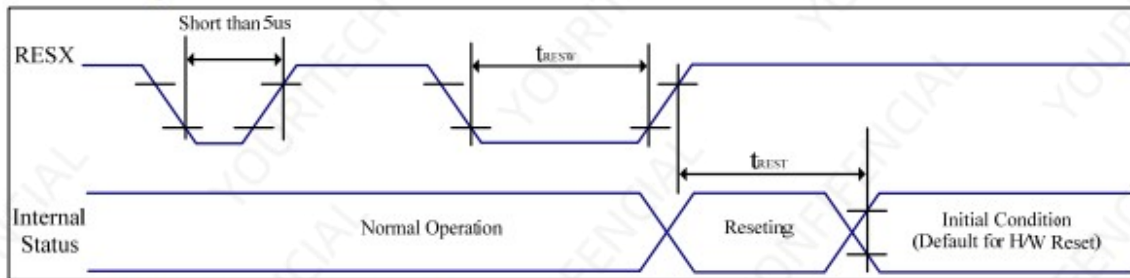


Figure: Switching the clock Lane between clock Transmission and Low Power Mode

Reset timing characteristics



VSS=0V, IOVCC=1.65V to 3.6V, VCI=2.5V to 6.0V, Ta = -30°C to 70°C

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
T_{resw}	*1) Reset low pulse width	RESX	10	-	-	-	us
T_{rest}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-	-	-	120	When reset applied during Sleep out mode	ms

Table: Reset input timing

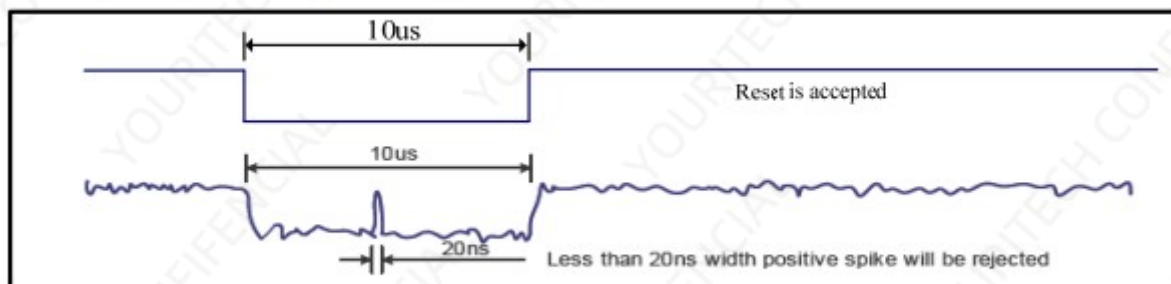
Note 1: Due to an electrostatic discharge on RESX line, spike does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts (It depends on voltage and temperature condition.)

Note 2: During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120ms, when Reset Starts in Sleep Out mode. The display remains the blank state in Sleep In mode), then return to default condition for H/W reset.

Note 3: During Reset Complete Time, ID1/ID2/ID3 and VCOM value in OTP will be latched to internal register. After a rising edge of RESX, there is a H/W reset complete time (T_{rest}) which lasted 5ms. The loading operation will be done every time during this reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



Note 5: It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120 msec.

7. Optical Characteristics

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle range	Horizontal	Θ_3	CR > 10	70	80	-	Deg.	Note 1
		Θ_9		70	80	-	Deg.	
	Vertical	Θ_{12}		70	80	-	Deg.	
		Θ_6		70	80	-	Deg.	
Contrast ratio		CR	$\Theta = 0^\circ$	700	900	-	-	Note 2
Transmittance		Tr		3.7	4.3	-	%	Note 3
Color Gamut	NTSC	CIE1931	$\Theta = 0^\circ$	65	70	-	%	Note 4
Reproduction of color	White	Wx	$\Theta = 0^\circ$	Typ -0.03	0.300	Typ +0.03	-	
		Wy			0.329		-	
Response Time		Tr+Td	Ta= 25° C $\Theta = 0^\circ$	-	30	40	ms	Note 5

Notes : 1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see FIGURE 1).

2. Contrast measurements shall be made at viewing angle of $\Theta = 0$ and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state . (see FIGURE 1)
- 1) Luminance Contrast Ratio (CR) is defined mathematically.

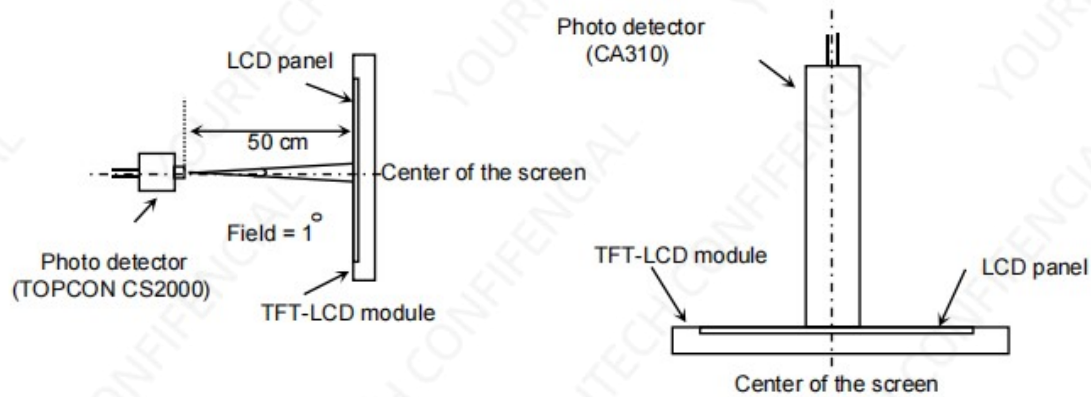
$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Transmittance is the Value without APF and without CG.

4. The color chromaticity coordinates specified in Table 5. shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel and based on C Light.

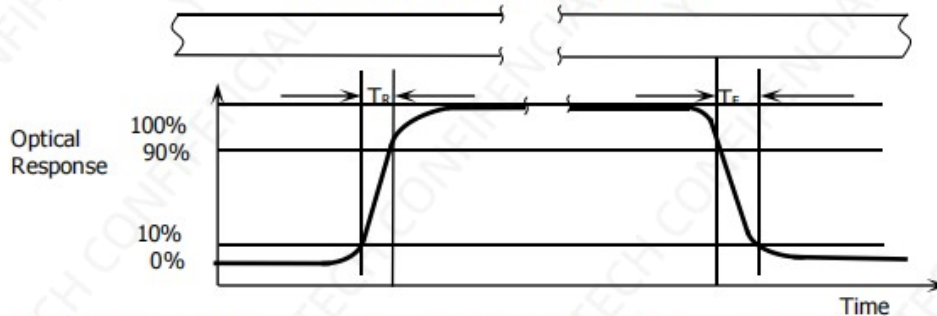
5. The electro-optical response time measurements shall be made as FIGURE 2. The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Tf.

Figure 1. Measurement Set Up



View angel range, uniformity, etc. measurement setup Flicker, measurement setup

Figure 2. Response Time Testing



The electro-optical response time measurements shall be made as shown in FIGURE 3. The times needed for the luminance to change from 10% to 90% is T_r and 90% to 10% is T_f .

8. Reliability Test Item

No.	Test Item	Test Condition	Notes
1	High Temp. Storage	+80°C / 96H	1. Functional test is OK. Missing Segment, short, unclear segment non-display, display abnormally and liquid crystal leakage are un-allowed. 2. No low temperature bubbles, end seal loose and fall, frame rainbow.
2	Low Temp. Storage	-30°C / 96H	
3	High Temperature Operating	+70°C / 96H	
4	Low Temperature Operating	-20°C / 96H	
5	High Temperature / Humidity storage	50°C x 90%RH / 96H	
6	Thermal and cold shock	Static state, -20°C (30min) ~ 70°C (30min), 50 cycles	

9. Packing Method----TBD

- END -