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MODEL NO : ET080WX01-T

MODEL VERSION: 01

SPEC VERSION : 1.0

ISSUED DATE: 2021-08-23

□Preliminary Specification

■Final Product Specification

Customer :

Approved by	Notes

Youri Confirmation

Prepared by	Reviewed by	Approved by
John	Johnny	Wang

1. Introduction

1.1 Scope of application

LCD specification: Dots 800xRGBx1280
As to basic specification of the driver IC, refer to the IC (JD9365DA-H3) specification and data book.
All material & processing of the LCD module should be Lead Free.

1.2 TFT features:

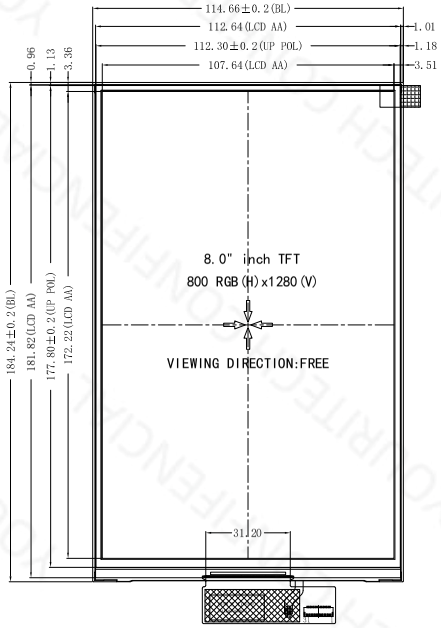
Structure: TFT PANNEL+IC +FPC+BL;
ALL Viewing Type LCD
800 dot-segment and 1280 dot-common outputs;
16.7M Color can be selected by software;
White LED back light;
4lane MIPI interface

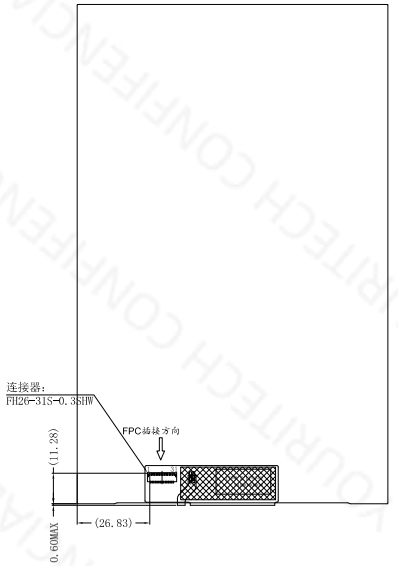
1.3 Applications:

2. LCM General specification

ITEM	Sandard value	Unit
LCD Type	Normally Black	--
Drive element	TFT active matrix	--
Number of pixels	800*3RGB(H)X1280(V)	Dots
Pixel arrangement	RGB Vertical Stripe	--
Pixel Pitch (W*H)	0.13455(H) X 0.13455(V)	mm
Active area	107.64(H) x 172.224(V)	mm
Viewing direction	ALL O'CLOCK	-
TFT Driver IC	JD9365DA-H	
TFT interface	4lane MIPI interface	-
Approx. Weight	TBD	g
LCM Size(W*H*T)	114.66(W) ×184.24(H) ×2.41(T)	mm
Touch structure	--	
Touch Driver IC	--	-
Touch Interface	--	

REV	DESCRIPTION	DRG DATE	DRAWN BY
	First Desing	2021.08.03	

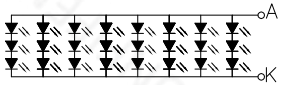




PIN DESCRIPTION

1	LEDA
2	LEDA
3	LEDA
4	NC
5	LEDK
6	LEDK
7	LEDK
8	LEDK
9	GND
10	GND
11	MIPI_D2+
12	MIPI_D2-
13	GND
14	MIPI_D1+
15	MIPI_D1-
16	GND
17	MIPI_CLK+
18	MIPI_CLK-
19	GND
20	MIPI_D0+
21	MIPI_D0-
22	GND
23	MIPI_D3+
24	MIPI_D3-
25	GND
26	TE
27	RESET
28	ID(NC)
29	VDDIO/1.8V
30	VDD/3.3V
31	VDD/3.3V

NOTES:
1. DISPLAY TYPE: 8.0", TFT LCD
2. DISPLAY MODE: transmissive Normally Black
3. VIEWING DIRECTION: 80/80/80/80(TYP)
4. DRIVER IC:JD9365DA-H3
5. LCM (White 9 AVG 1/6) :
   Brightness: 350cd/m2 (TYP)
   Uniformity:70%(MIN)
6. BACK LIGHT: 24 chip white LEDs If=160mA, Vf=8.4V~9.6V
7. OPERATING TEMP: -10° C TO 60° C, STORAGE TEMP: -20° C TO 70° C
8. * Critical Parameter, ( ) ref Parameter, [ ] cpk Parameter
   Unspecified Tolerances:±0.20mm
   Modification mark:
9. SUGGESTION:TP window size unilateral increase 0.3~0.5mm than LCM A.A
10. REQUIREMENTS ENVIRONMENTAL PROTECTION: RoHS



Backlight LED Circuit

深圳市优瑞泰克科技有限公司

PART NO.:	ET080WX01-T			MODULE NO.:	00
DRAWN BY:	LIU	DATE:		PROJECTION:	
CHECKED BY:		DATE:		SCALE:N.T.S	UNIT: mm
APPROVED BY:		DATE:		SHEET: 1 OF 1	

3.Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
LCM Operating Temperature	T_{OPR}	-10	+60	°C
LCM Storage Temperature	T_{STG}	-20	+70	°C
Humidity	RH	-	90	%

4.Electrical Characteristics

4.1 TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage for I/O	VDDIO	1.65	1.8	3.6	V
Supply Voltage for(DC/DC)	VDD	2.7	3.3	3.6	V
Current Consumption	I_{DD}	--	150	--	mA
	$I_{DD-SLEEP}$	--	80	160	uA

4.2 Back-Light Unit Characeristics

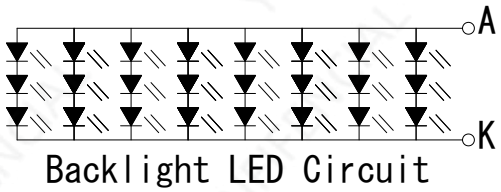
The back-light system is an edge-lighting type with 24 white LEDs. The characteristics of the back-light are shown in the following tables.

Characteristics	Symbol	Min.	Type	Max.	Unit	Notes
Forward Voltage	V_F	8.4		9.6	V	-
Forward current	I_F	--	160	-	mA	-
Luminance(With LCD)	Lv		350	--	cd/m^2	-
LED life time	N/A	----	30,000	--	Hr	Note 1

Note:

(1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=20mA/LED. The LED life time could be decreased if operating I_L is larger than 25mA/LED.

Backlight circuit diagram shown in below:



Backlight LED Circuit

5. Module Function Description

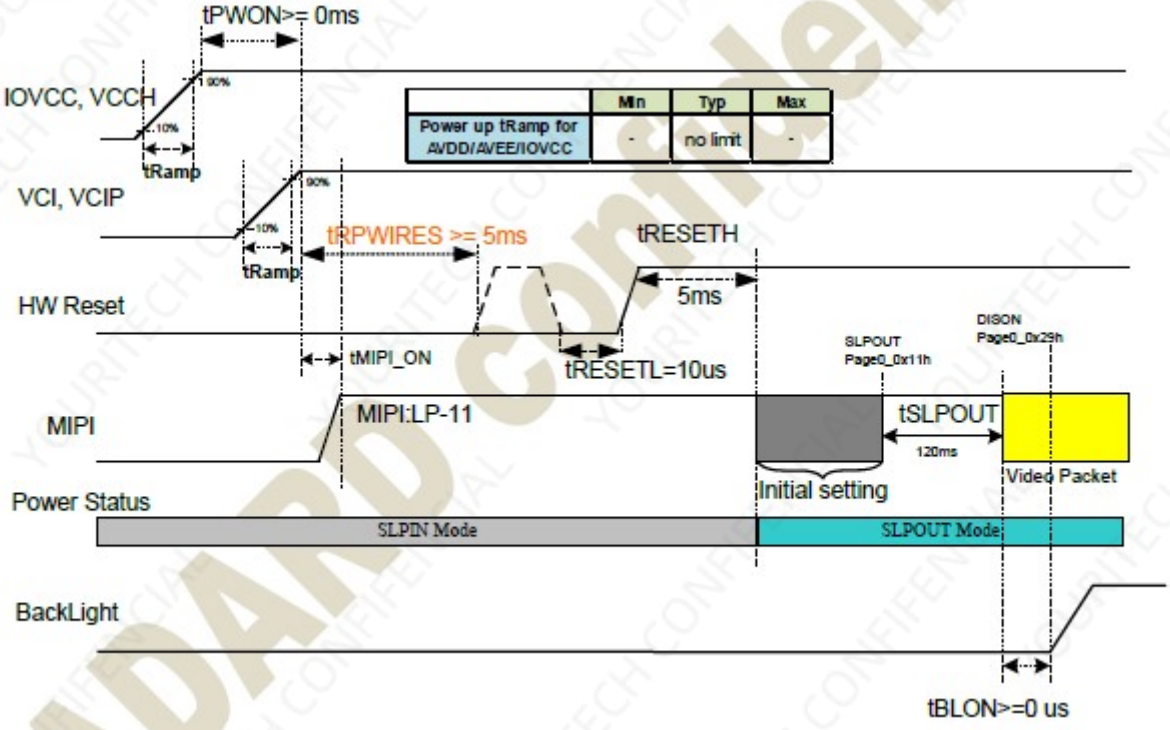
Pin No.	Symbol	LCM Functional	Notes
1	LEDA	Power supply for backlight anode input terminal.	
2	LEDA	Power supply for backlight anode input terminal.	
3	LEDA	Power supply for backlight anode input terminal.	
4	NC	NC	
5	LEDK	Power supply for backlight cathode input terminal.	
6	LEDK	Power supply for backlight cathode input terminal.	
7	LEDK	Power supply for backlight cathode input terminal.	
8	LEDK	Power supply for backlight cathode input terminal.	
9	GND	Power Ground	
10	GND	Power Ground	
11	MIPI_D2+	MIPI-DSI Data differential signal input pins	
12	MIPI_D2-	MIPI-DSI Data differential signal input pins	
13	GND	Power Ground	
14	MIPI_D1+	MIPI-DSI Data differential signal input pins	
15	MIPI_D1-	MIPI-DSI Data differential signal input pins	
16	GND	Power Ground	
17	MIPI_CLK+	MIPI-DSI CLOCK differential signal input pins	
18	MIPI_CLK-	MIPI-DSI CLOCK differential signal input pins	
19	GND	Power Ground	
20	MIPI_D0+	MIPI-DSI Data differential signal input pins	
21	MIPI_D0-	MIPI-DSI Data differential signal input pins	
22	GND	Power Ground	
23	MIPI_D3+	MIPI-DSI Data differential signal input pins	
24	MIPI_D3-	MIPI-DSI Data differential signal input pins	
25	GND	Power Ground	
26	TE	Serves TE (Tearing Effect) pin on MPU interface	
27	RESET	Reset pin. Setting either pin low initializes the LSI	
28	ID	NC	
29	VDDIO/1.8V	power supply for the I/O circuit	
30	VDD/3.3V	power supply for DC/DC circuit	
31	VDD/3.3V	power supply for DC/DC circuit	

6. Timing Characteristics

Power on sequence for differential power mode

Symbol	Min	Typ	Max	Unit	Remark
tRamp	-	no limit	-	us	
tPWON	0	-	-	ms	
tON1	0	-	-	ms	
tMIPI-ON	0	-	tRPWIRES	ms	
tRPWIRES	5	-	-	ms	
tRESETL	10	-	-	us	
tRESETH	5	-	-	ms	
tSLPOUT	120	-	-	ms	
tBLON	0	-	-	ms	

BOOSTM[1:0]=10 (Internal DC/DC power mode : Charge Pump, FP7721)
VCCD=IOVCC=VCCH=1.65V ~ 3.6V, VCI=VCIP=2.5V ~ 4.8V.
Power on:



Burst Mode Data Transmission

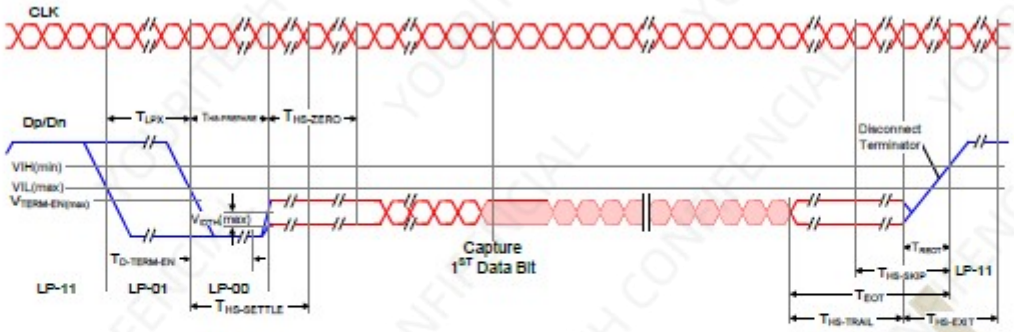


Figure 11.7: High-Speed Data Transmission in Bursts

Parameter	Description	Min	Typ	Max	UNIT
T_{LPX}	Transmitted length of any Low-Power state period	50	-	-	ns
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40 + 4*UI	-	85 + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 + 10*UI	-	-	ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination.	-	-	35 + 4*UI	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions.	85 + 6*UI	-	145 + 10*UI	ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	max(n*8*UI, 60 + n*4*UI)	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

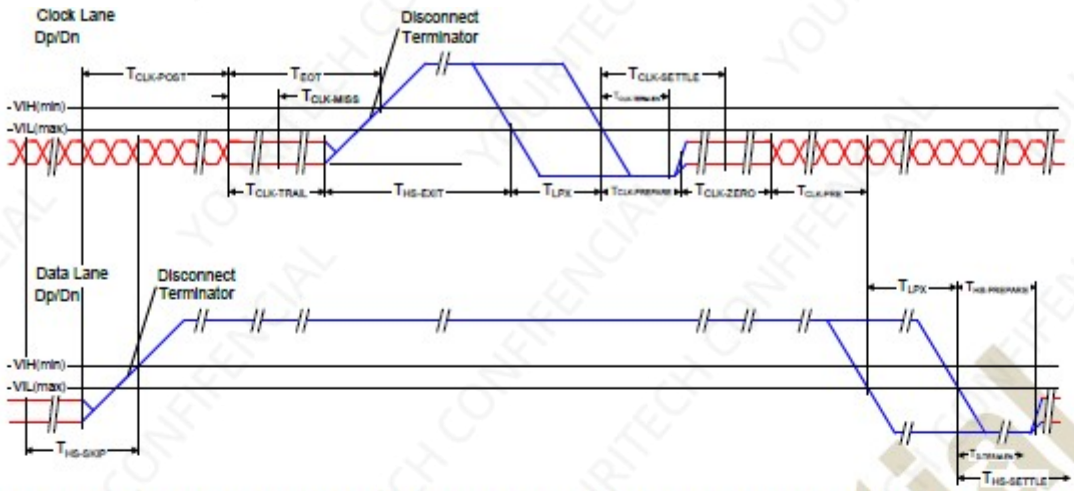


Figure 11.8: Switching the Clock Lane between Clock Transmission and Low-Power Mode

Parameter	Description	Min	Typ	Max	UNIT
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode.	60 + 52*UI	-	-	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8*UI	-	-	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38	-	95	ns
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300	-	-	ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination.	-	-	38	ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

Reset input timings

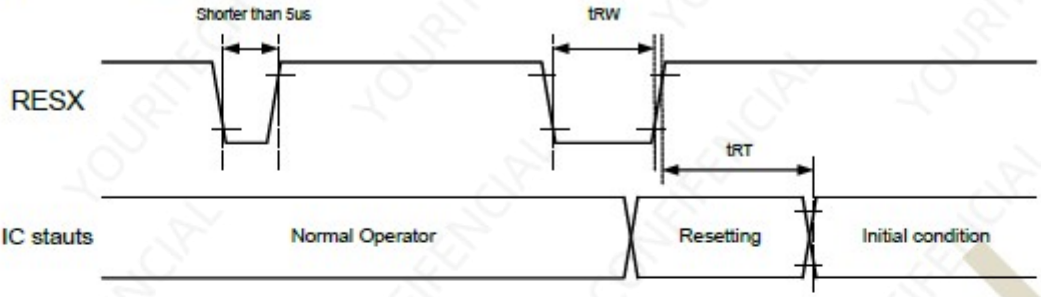


Figure 11.1: Reset input timings

Symbol	Parameter	Related pins	Min.	Max.	Unit
t_{RW}	Reset pulse width(2)	RESX	10	-	µs
t_{RT}	Reset complete time(3)	-	-	5 (Note 5)	ms
		-	-	120 (Note 6, 7)	ms

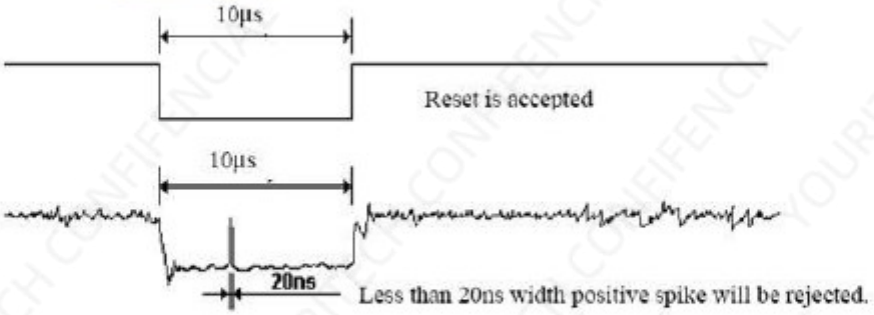
Note: (1) The reset complete time also required time for loading ID bytes from OTP to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

(2) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5 µs	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

(3) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for H/W reset.

(4) Spike Rejection also applies during a valid reset pulse as shown below:



(5) When Reset is applied during Sleep In Mode.

(6) When Reset is applied during Sleep Out Mode.

(7) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

(8) After Sleep Out Command, it is necessary to wait 120msec then send RESX.

Table 11.3: Reset timings

7. Optical Characteristics

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle range	Horizontal	Θ_3	CR > 10	-	80	-	Deg.	WV-Pol Note 1
		Θ_9		-	80	-	Deg.	
	Vertical	Θ_{12}		-	80	-	Deg.	
		Θ_6		-	80	-	Deg.	
Luminance Contrast ratio		CR	Θ = 0°	900	1200	-		Note 2
Cell Transmittance		Tr		-	4.8	-	%	W/O APF
White Chromaticity		x_w		TYP. - 0.03	0.306	TYP. + 0.03		Note 3 Base on C Light
		y_w			0.360			
Reproduction of color (C light)	Red	R_x			0.646			
		R_y			0.339			
	Green	G_x			0.271			
		G_y			0.581			
	Blue	B_x			0.138			
		B_y			0.158			
Color Gamut (C light)				-	60%	-	%	NTSC
Response Time (Rising + Falling)		T_{RT}	Ta= 25° C Θ = 0°	-	-	35	ms	Note 4

Note :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface .

2. Contrast measurements shall be made at viewing angle of Θ= 0 and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state . Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Transmittance is the Value with Polarizer.

4. The color chromaticity coordinates specified in Table 6 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Calculation is based on C light.

5. The electro-optical response time measurements shall be made as FIGURE 6 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Td.

8. Reliability Test Item

No.	Test Item	Test Condition	Notes
1	High Temp. Storage	+70°C / 96H	1. Functional test isOK. Missing Segment,short, unclear segment non-display,display abnormally and liquid crystal leakare un-allowed. 2. No low temperature bubbles,end seal loose andfall, frame rainbow.
2	Low Temp. Storage	-20°C / 96H	
3	High Tempe. Operating	+60°C / 96H	
4	Low Tempe. Operating	-10°C / 96H	
5	High Temperature /Humidity storage	50°C x 90%RH /96H	
6	Thermal and cold shock	Static state， -20℃（30min） ~60℃（30min），50 cycles	

9. Packing Method----TBD

- END -