YOURITech
AN EUROTECH COMPANY

INDUSTRIAL STRENGTH...
Start Your Application From YOURITECH

Integration support
Obsolescence Management
PCAP
Embedded Systems
Human Machine Interface
Touch Solutions
Production
Custom designs
Installation
Software
Mechanical design
Quality Management
Open Frame Monitors
LCD Controller
Research & Development
Firmware
EMC tests
on-site service
In-house Manufacturing
Optical Bonding
Cover glass
System solutions
OEM Solutions
Custom Display

Erotech YOURITech AN EUROTECH COMPANY AOSHITE 奥视特 Your Reliable Display Panel and Smart Touch Embedded Solution Partner

For more information about comprehensive display panels and touch embedded solutions, welcome contact us at:

https://www.youritech.com
info@youritech.com

Project No. 项目编号	ET088WF01-TT
Customer 客户名称	
Module No. 客户型号	
Product type 产品内容	**Standard LCD Module** **TFT：480*RGBx1920Dots** **8.8”TFT LCD+CTP**

客户确认Customer Approval	
项目负责人Project Manager	
品质主管Director of Quality	
采购工程师Purchasing Engineer	

1. Introduction

1.1 Scope of application

This specification applies to the LCD module that is supplied by YOURITECH Technology CO., LTD.
LCD specification: Dots 480xRGBx1920
As to basic specification of the driver IC, refer to the IC (OTA7290B) specification and data book.
All material & processing of the LCD module should be Lead Free.

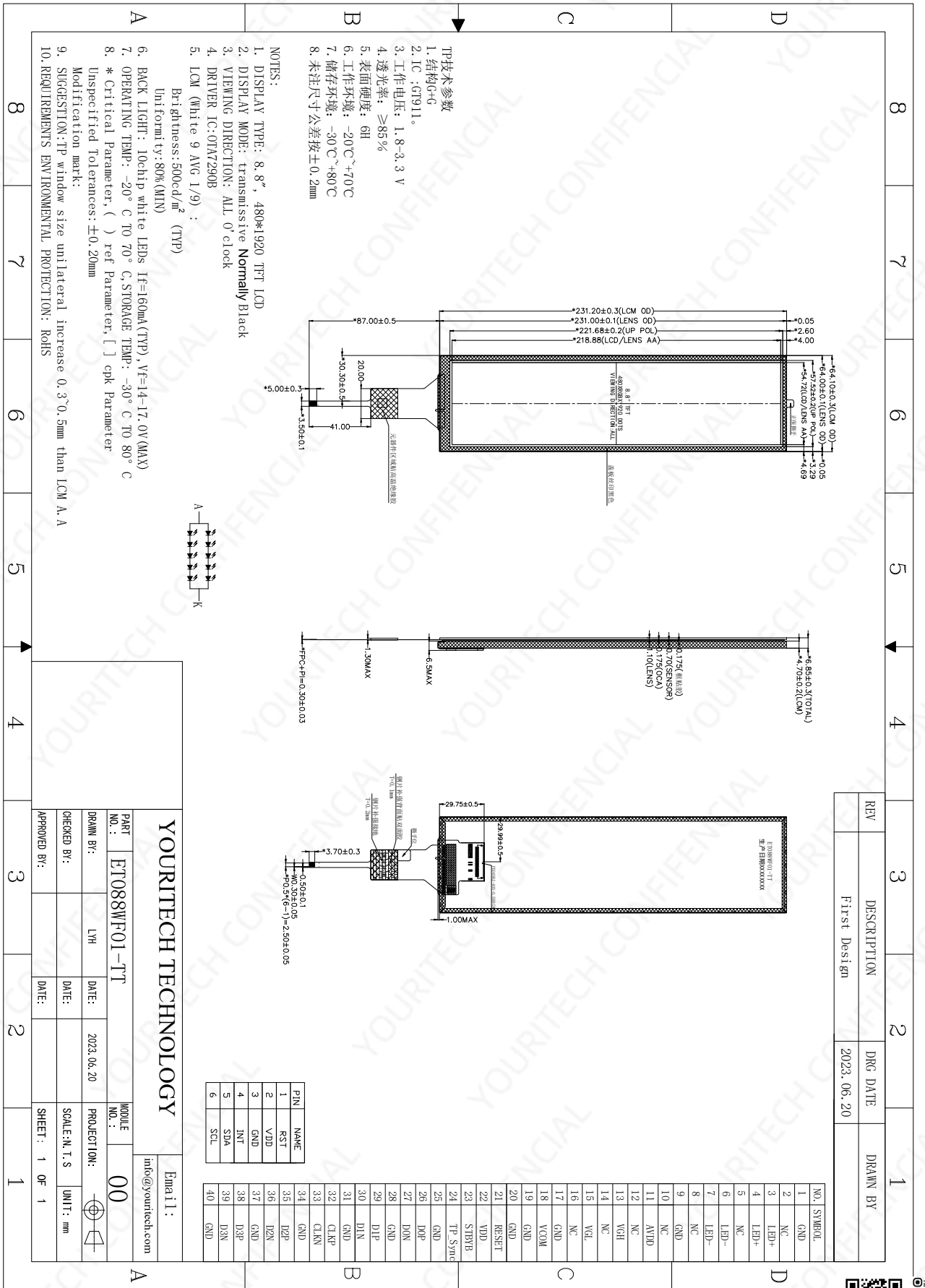
1.2 TFT features:

Structure: TFT PANNEL+IC +FPC+BL+CTP;
ALL Viewing Type LCD
480 dot-segment and 1920 dot-common outputs;
16.7M Color can be selected by software;
White LED back light;
4lane MIPI interface

1.3 Applications:

2. LCM General specification

ITEM	Sandard value	Unit
LCD Type	Normally Black	--
Drive element	TFT active matrix	--
Number of pixels	480*3RGB(H)X1920(V)	Dots
Pixel arrangement	RGB Vertical Stripe	--
Pixel Pitch (W*H)	0.114(H) X 0.114(V)	mm
Active area	54.72(H) x 218.88(V)	mm
Viewing direction	ALL O'CLOCK	--
TFT Driver IC	OTA7290B	--
TFT interface	4lane MIPI interface	--
Approx. Weight	TBD	g
LCM Size(W*H*T)	64.10(W) ×231.20(H) ×4.70(T)	mm
LCM+CTP Size(W*H*T)	64.00(W) ×231.00(H) ×6.85(T)	mm
Touch structure	G+G	--
Touch Driver IC	GT911	--
Touch Interface	I2C	--


TP技术参数
1. 结构G+G
2. IC ：GT911。
3. 工作电压：1.8~3.3 V
4. 透光率：≥85%
5. 表面硬度：6H
6. 工作环境：-20℃~+70℃
7. 储存环境：-30℃~+80℃
8. 未注尺寸公差按±0.2mm
NOTES:
1. DISPLAY TYPE: 8.8", 480*1920 TFT LCD
2. DISPLAY MODE: transmissive Normally Black
3. VIEWING DIRECTION: ALL O'clock
4. DRIVER IC:OTA7290B
5. LCM (White 9 AVG 1/9) :
Brightness:500cd/m² (TYP)
Uniformity:80%(MIN)
6. BACK LIGHT: 10chip white LEDs If=160mA(TYP),Vf=14-17.0V(MAX)
7. OPERATING TEMP: -20° C TO 70° C,STORAGE TEMP: -30° C TO 80° C
8. * Critical Parameter,( ) ref Parameter,[ ] cpk Parameter
Unspecified Tolerances:±0.20mm
Modification mark:
9. SUGGESTION:TP window size unilateral increase 0.3~0.5mm than LCM A.A
10. REQUIREMENTS ENVIRONMENTAL PROTECTION: RoHS
*231.20±0.3(LCM OD)
*231.00±0.1(LENS OD)
*221.68±0.2(UP POL)
*218.88(LCD/LENS AA)
*87.00±0.5
*64.10±0.3(LCM OD)
*54.72(LCD/LENS AA)
*30.30±0.5
20.00
*5.00±0.3
*3.50±0.1
41.00
*0.05
*2.60
*4.00
*3.29
*4.69
*6.85±0.3(TOTAL)
*4.70±0.2(LCM)
*1.30MAX
*6.5MAX
*FPC+PI=0.30±0.03
*0.175(粘贴胶)
*0.70(SENSOR)
*0.175(OCA)
*1.10(LENS)
*29.75±0.5
*29.99±0.5
*3.70±0.3
*1.00MAX
*0.50±0.1
*W0.30±0.05
P0.5(6-1)=2.50±0.05
A
K
REV
DESCRIPTION
DRG DATE
DRAWN BY
First Desig
2023.06.20
NO. SYMBOL
1 GND
2 NC
3 LED+
4 LED+
5 NC
6 LED-
7 LED-
8 NC
9 GND
10 NC
11 AVDD
12 NC
13 VGH
14 NC
15 VGL
16 NC
17 GND
18 VCOM
19 GND
20 GND
21 RESET
22 VDD
23 STBYB
24 TP Sync
25 GND
26 DOP
27 DON
28 GND
29 D1P
30 D1N
31 GND
32 CLKP
33 CLKN
34 GND
35 D2P
36 D2N
37 GND
38 D3P
39 D3N
40 GND
PIN NAME
1 RST
2 VDD
3 GND
4 INT
5 SDA
6 SCL
YOURITECH TECHNOLOGY
Email: info@youritech.com
PART NO.: ET088WF01-TT
MODULE NO.: 00
DRAWN BY: LYH
DATE: 2023.06.20
PROJECTION:
CHECKED BY:
DATE:
SCALE:N.T.S
UNIT: mm
APPROVED BY:
DATE:
SHEET: 1 OF 1

3.Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
LCM Operating Temperature	T_{OPR}	-20	+70	°C
LCM Storage Temperature	T_{STG}	-30	+80	°C
TP Operating Temperature & Humidity (20% ~ 90%RH)	T_{OPR}	-20	+70	°C
TP SStorage Temperature & Humidity (20% ~ 90%RH)	T_{STG}	-30	+80	°C
Humidity	RH	--	90	%

4.Electrical Characteristics

4.1 TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
TFT OperationFrame rate	Hz	--	60	--	Hz	--
Supply Voltage for(DC/DC)	VDD	2.7	2.8	3.6	V	--
TFT Gate ON Voltage	VGH	--	18	--	V	--
TFT Gate OFF Voltage	VGL	--	-10	--	V	--
TFT Common Voltage	Vcom	4.5	4.88	5.2	V	--
AVDD	Avdd	--	9.6	--	V	--

4.2 Back-Light Unit Characeristics

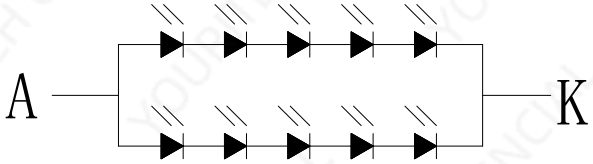
The back-light system is an edge-lighting type with 10 white LEDs. The characteristics of the back-light are shown in the following tables.

Characteristics	Symbol	Min.	Type	Max.	Unit	Notes
Forward Voltage	V_F	14	--	17	V	--
Forward current	I_F	--	160	--	mA	--
Luminance(With LCD+CTP)	Lv	--	500	--	cd/m^2	--
LED life time	N/A	--	20,000	--	Hr	Note 1

Note:

(1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=40mA/LED. The LED life time could be decreased if operating I_L is larger than 50mA/LED.

Backlight circuit diagram shown in below:



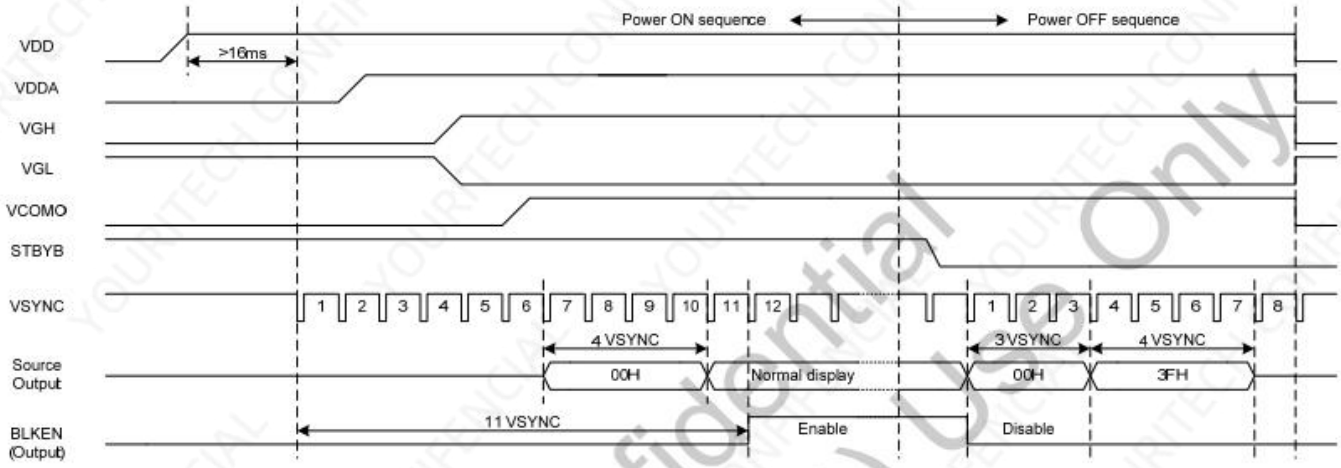
5. Module Function Description

Pin No.	Symbol	LCM Functional	Notes
1	GND	Power Ground	
2	NC	No Connection.	
3	LEDA	Power supply for backlight anode input terminal.	
4	LEDA	Power supply for backlight anode input terminal.	
5	NC	No Connection.	
6	LEDK	Power supply for backlight cathode input terminal.	
7	LEDK	Power supply for backlight cathode input terminal.	
8	NC	No Connection.	
9	GND	Power Ground	
10	NC	No Connection.	
11	AVDD	Power supply for Analog Circuit	
12	NC	No Connection.	
13	VGH	Power supply for Positive Power for TFT	
14	NC	No Connection.	
15	VGL	Power supply for Negative Power for TFT	
16	NC	No Connection.	
17	GND	Power Ground	
18	VCOM	Power supply for Common voltage.	
19	GND	Power Ground	
20	GND	Power Ground	
21	RESET	Reset pin. Setting either pin low initializes the LSI	
22	VCI	power supply for DC/DC circuit(2.7~3.6V)	
23	STBYB	Standby mode	
24	TP_SYNC	Sync signal for touch panel	
25	GND	Power Ground	
26	D0P	High speed interface data differential signal input/output pins	
27	D0N	High speed interface data differential signal input/output pins	
28	GND	Power Ground	
29	D1P	High speed interface data differential signal input/output pins	
30	D1N	High speed interface data differential signal input/output pins	
31	GND	Power Ground	
32	CLKP	High speed interface clock differential signal input/output pins	

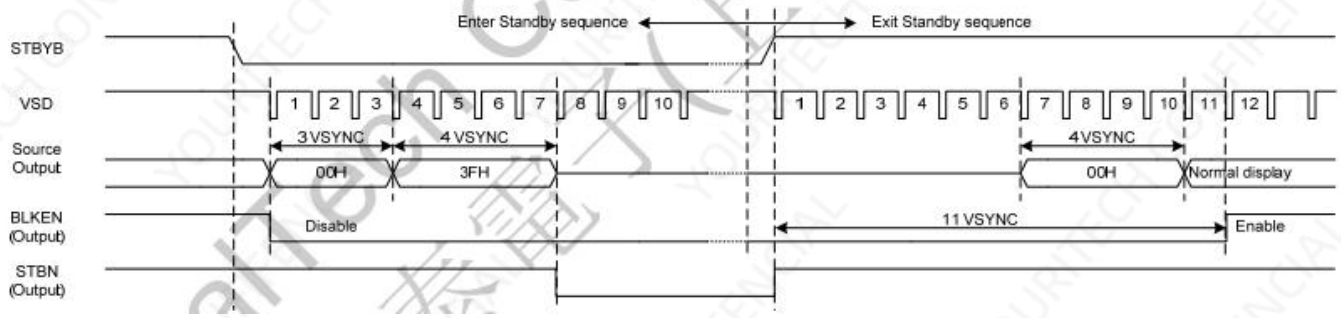
33	CLKN	High speed interface clock differential signal input/output pins	
34	GND	Power Ground	
35	D2P	High speed interface data differential signal input/output pins	
36	D2N	High speed interface data differential signal input/output pins	
37	GND	Power Ground	
38	D3P	High speed interface data differential signal input/output pins	
39	D3N	High speed interface data differential signal input/output pins	
40	GND	Power Ground	

6. Timing Characteristics

Power-On/Off Timing Sequence:



Enter and Exit Standby Mode Sequence:



HS Receiver AC Timing Characteristics

Parameter	Symbol	Rating			Unit	Note
		Min	Typ	Max		
Bandwidth per lane	-	-	-	1000	Mbps	Bandwidth selected by register 'speedup' Speedup=0 → Max=550Mbps Speedup=1→ Max=1000Mbps
Operation frequency	-	-	-	500	MHz	
UI instantaneous	UI_{INST}	1	-	12.5	ns	1
Data to Clock Skew	Tskew	-0.15	-	0.15	UI_{INST}	
Inter-lane static skew	Tskew-lane	-	-	UI_{INST}/50	UI_{INST}	
Data to Clock Setup Time	T_{SETUP}	0.25	-	-	UI_{INST}	2
Data to Clock Hold Time	T_{HOLD}	0.25	-	-	UI_{INST}	
Common-mode interference beyond 450MHz	$\Delta V_{CMRX(HF)}$	-	-	100	mV	4
Common-mode interference 50MHz- 450MHz	$\Delta V_{CMRX(LF)}$	-50	-	50	mV	3,6
Common-mode termination	C_{CM}	-	-	60	pF	5

Note:

(1) Total silicon and package delay budget of 0.3*UINST

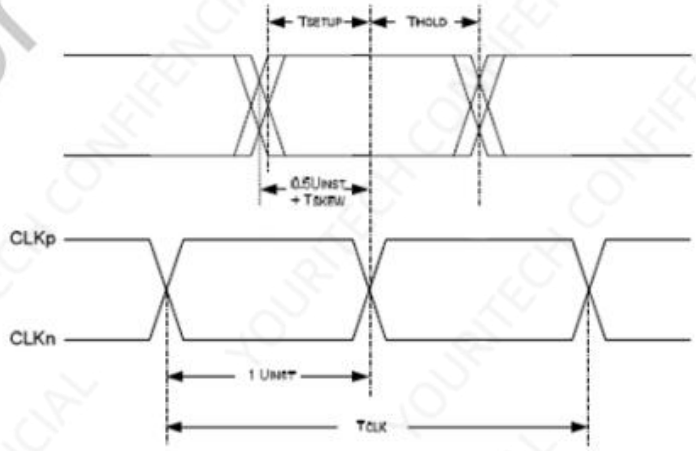
(2) Total setup and hold window for receiver of 0.3*UINST

(3) Excluding 'static' ground shift of 50mV

(4) =VCMRX (HF) is the peak amplitude of a sine wave superimposed on the receiver input

(5) For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

(6) Voltage difference compared to the DC average common-mode potential.



LP Receiver AC Timing Characteristics

Parameter	Symbol	Rating			Unit	Note
		Min	Typ	Max		
Input pulse rejection	e_{SPIKE}	-	-	300	V·ps	1,2,3
Minimum pulse width response	T_{MIN-RX}	20	-	-	ns	
Peak interference amplitude	V_{INT}	-	-	200	mV	
Interference frequency	f_{INT}	450	-	-	MHz	
Logic 1 input voltage	V_{IH}	880	-	-	mV	
Logic 0 input voltage, not in ULP State	V_{IL}	-	-	550	mV	
Logic 0 input voltage, ULP State	$V_{IL-ULPS}$	-	-	300	mV	
Input Hysteresis	V_{HYST}	25	-	-	mV	
Logic 1 contention threshold	V_{IHCD}	450	-	-	mV	
Logic 0 contention threshold	V_{ILCD}	-	-	200	mV	

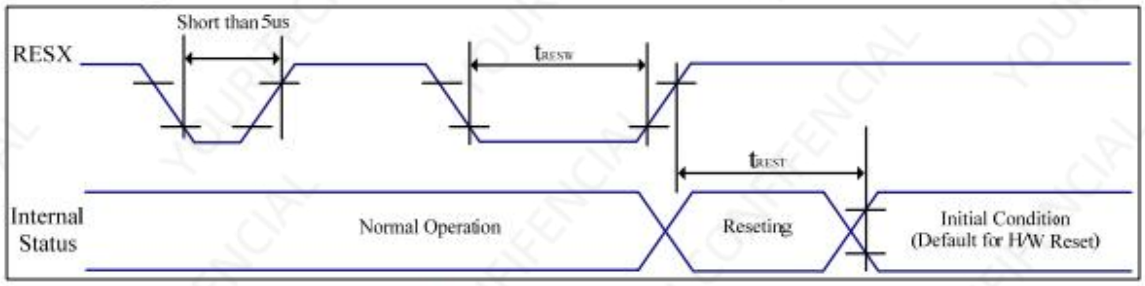
Note:

(1) Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1state.

(2) An impulse less than this will not change the receiver state.

(3) In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.

Reset timing characteristics



VSS=0V, IOVCC=1.65V to 3.6V, VCI=2.5V to 6.0V,Ta = -30℃ to 70℃

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
T_{resw}	*1) Reset low pulse width	RESX	10	-	-	-	us
T_{rest}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-	-	-	120	When reset applied during Sleep out mode	ms

Table: Reset input timing

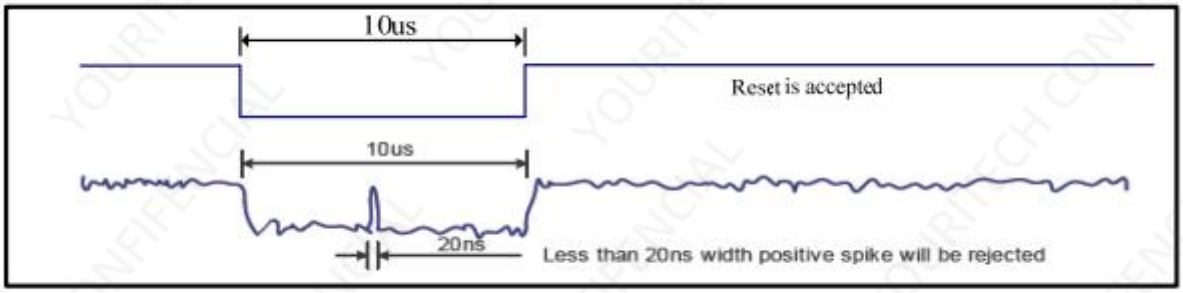
Note 1: Due to an electrostatic discharge on RESX line,spike does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts (It depends on voltage and temperature condition.)

Note 2: During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120ms, when Reset Starts in Sleep Out mode. The display remains the blank state in Sleep In mode) , then return to default condition for H/W reset.

Note 3: During Reset Complete Time, ID1/ID2/ID3 and VCOM value in OTP will be latched to internal register. After a rising edge of RESX, there is a H/W reset complete time (Trest) which lasted 5ms.The loading operation will be done every time during this reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120 msec.

7. Optical Characteristics

7.1 Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Transmittance (with Polarizer)		T (%)	Θ=0 Normal viewing angle	—	4.2	—	%	Measuring with Polarizer, Reference Only
Transmittance (without Polarizer)		T (%)		—	14.2	—	%	
Contrast		CR		640	800	—	—	(1)(2)
Response time	Rising	$Tr+T_F$		—	40	—	msec	(1)(3)
Color gamut	(%)			—	50	—	%	C-light
Color chromaticity (CIE1931)	White	W_x		0.246	0.296	0.346	—	(1)(4) CF glass
		W_y		0.274	0.324	0.374		
	Red	R_x					—	
		R_Y					—	
	Green	G_x					—	
		G_Y						
	Blue	B_x					—	
		B_Y						
Viewing angle	Hor.	Θ_L	CR>10	—	80	—	—	(1)(4) Measuring with Polarizer, Reference Only
		Θ_R		—	80	—		
	Ver.	Θ_U		—	80	—		
		Θ_D		—	80	—		
Optima View Direction		Free						(5)

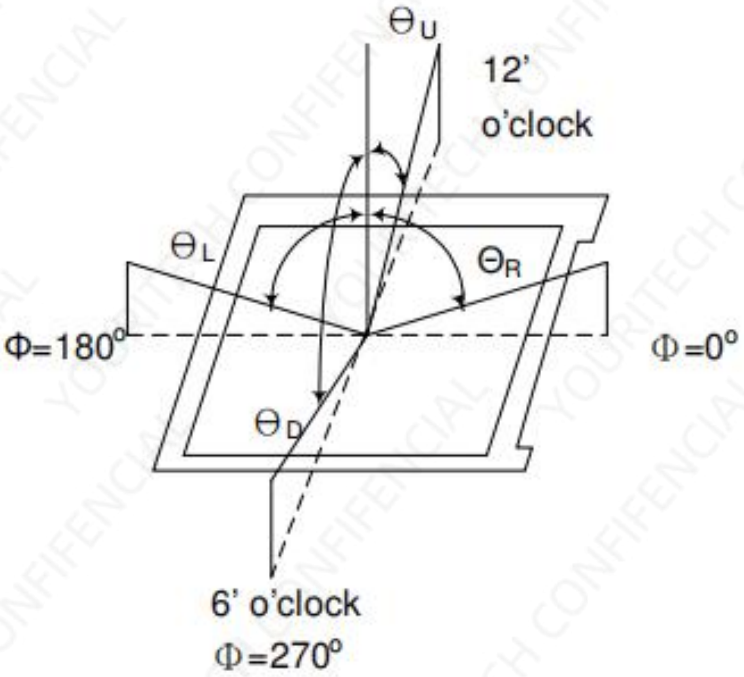
7.2 Measuring Condition

- Measuring surrounding：dark room
- Ambient temperature：25±2°C
- 15min. warm-up time.

7.3 Measuring Equipment

- FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

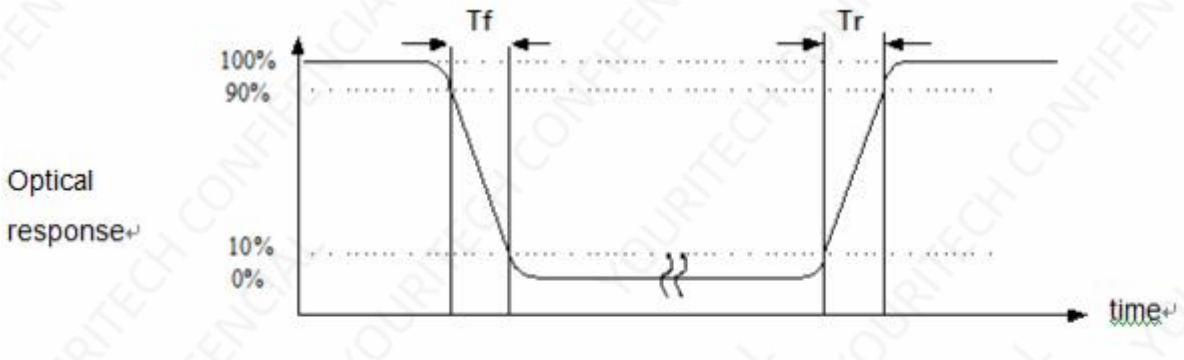
Note (1) Definition of Viewing Angle:



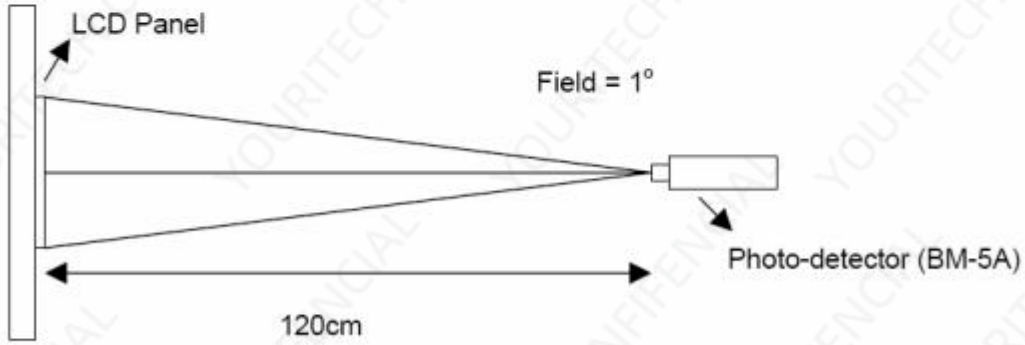
Note (2) Definition of Contrast Ratio (CR) :
measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note (3) Definition of Response Time : Sum of T_R and T_F



Note (4) Definition of optical measurement setup



Note (5) Rubbing Direction (The different Rubbing Direction will cause the different optima view direction.)

8. Reliability Test Item

No.	Test Item	Test Condition	Notes
1	High Temp. Storage	+80°C / 96H	1. Functional test isOK. Missing Segment,short, unclear segment non-display,display abnormally and liquid crystal leakare un-allowed. 2. No low temperature bubbles,end seal loose andfall, frame rainbow.
2	Low Temp. Storage	-30°C / 96H	
3	High Tempe. Operating	+70°C / 96H	
4	Low Tempe. Operating	-20°C / 96H	
5	High Temperature /Humidity storage	50°C x 90%RH /96H	
6	Thermal and cold shock	Static state，-20℃（30min）~70℃（30min），10 cycles	

9. Packing Method----TBD

- END -