YOURITech
AN EUROTECH COMPANY

INDUSTRIAL STRENGTH...
Start Your Application From YOURITECH

Integration support
Obsolescence Management
PCAP
Embedded Systems
Human Machine Interface
Touch Solutions
Production
Custom designs
Installation
Software
Mechanical design
Quality Management
Open Frame Monitors
LCD Controller
Research & Development
Firmware
EMC tests
on-site service
In-house Manufacturing
Optical Bonding
Cover glass
System solutions
OEM Solutions
Custom Display

Erotech YOURITech AN EUROTECH COMPANY AOSHITE 奥视特 Your Reliable Display Panel and Smart Touch Embedded Solution Partner

For more information about comprehensive display panels and touch embedded solutions, welcome contact us at:

https://www.youritech.com
info@youritech.com

Product Specifications

Customer	Standard
Description	ePaper Display
Model Name	ET100EP01-J
Date	2026/01/20
Revision	1.0

	Design Engineering		
	Approval	Check	Design

Content

1. Overview

ET100EP01-J is a reflective electrophoretic Spectra 6 technology displaymodule based on active matrix TFT substrate. It has 10 ” active area with 1200 x 1600 pixels and3 ： 4 aspect ratios. The display is capable to display images at Black/White/Red/Yellow/Blue/Green depending on the display controller and the associated waveform file it used.

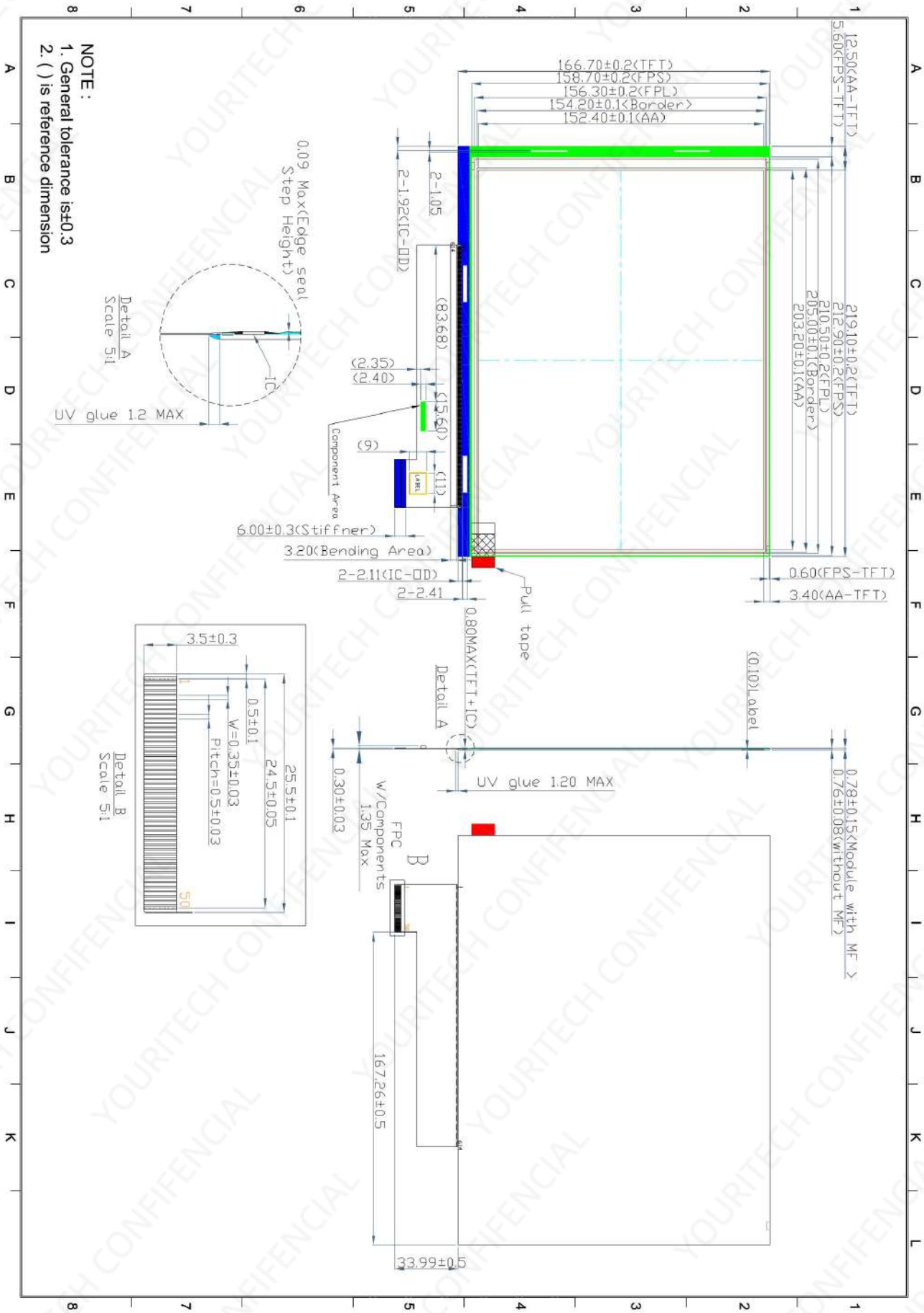
2. Features

- Display Black/White/Red/Yellow/Blue/Green colors
- High contrast electrophoreticimaging film
- Ultra-wide viewing angle
- Ultra-low power consumption
- Pure reflective mode
- Bi-stableimage
- Landscape mode
- Operation temperature range: 0℃ ~50℃

3. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	10	Inch	200ppi
Display Resolution	1600(H)×1200(V)	Pixel	4:3
Active Area	203.2 (H) ×152.4(V)	mm	
Pixel Pitch	0.127 (H) x 0.127 (V)	mm	
Pixel Configuration	Square		
Outline Dimension	219.1 (H) x 166.7 (V) x 0.78(D)	mm	Without masking film
Module Weight	31 ± 6	g	
Display operating mode	Reflective mode		
Surface treatment	Anti-glare treatment for protective sheet		
Operating Temp. Range	0 ~ 50	℃	
Storage Temp. Range	-25 ~ 60	℃	

4. Mechanical Drawing of EPD module



5. Input /Output Interface

5.1 Pin Assignment

Pin Assignment			
Pin #	**Single**	**Single**	**Description**
1	VGL	P	Negative Gate driving voltage.
2	NC	--	No Connection.
3	VGH	P	Positive Gate driving voltage.
4	NC	--	No Connection
5	VDD	P	Digital power for source and gate driver (Typ 3.3V).
6	OEV	I	Output enable for gate driver. When OEV=H, output is enabled and it is normal single pulse based on CKV. When OEH=L, all channel output forced to VGL.
7	CKV	I	Shift Clock for gate driver. The shift register data inside is shifted synchronously with each rising edge of CKV. And high and Low period of CKV is related to turn on and off time for TFT element of backplane.
8	SPV	I	Start pulse for gate driver. The default state should be at H level and active at L level.
9	GND	P	Ground.
10	VCOM	P	Common voltage.
11	CKH	I	Clock for source driver. Sensing SPH input at rising edge and then makes the internal shift register enabled. Also, at the rising edge, it would catch the data bits and stored in the latch circuit. CKH can't be toggled at OEH=L.
12	GND	P	Ground.
13	NC	--	No Connection.
14	D0	I	Image TTL Data for source driver.
15	D1	I	Image TTL Data for source driver.
16	D2	I	Image TTL Data for source driver.
17	D3	I	Image TTL Data for source driver.
18	D4	I	Image TTL Data for source driver.
19	D5	I	Image TTL Data for source driver.
20	D6	I	Image TTL Data for source driver.

21	D7	I	Image TTL Data for source driver.
22	GND	P	Ground.
23	D8	I	Image TTL Data for source driver.
24	D9	I	Image TTL Data for source driver.
25	D10	I	Image TTL Data for source driver.
26	D11	I	Image TTL Data for source driver.
27	D12	I	Image TTL Data for source driver.
28	D13	I	Image TTL Data for source driver.
29	D14	I	Image TTL Data for source driver.
30	D15	I	Image TTL Data for source driver.
31	SPH	I	Start pulse for source driver. The default state should be at H level and active at L level.
32	LEH	I	Latch enable for source driver. While LEH=H, the data stored in shift-register block is loaded into latch circuitry and then output starts to change according to the data in the latch block.
33	OEH	I	Output enable for source driver. When OEH=H, output is enabled and voltage level depends on input data. When OEH=L, all source channel output forced to GND.
34	NC	--	No Connection.
35	NC	--	No Connection.
36	VPOS3	P	Highest positive power supply source driver.
37	NC	--	No Connection.
38	VNEG3	P	Highest Negative power supply of source driver.
39	NC	--	No Connection.
40	BORDER	I	EPD border driving pin. To identify the Active Area of display.
41	XON	I	Control pin of all gate output switched to VGH. The default state should be at H level and active at L level.
42	VPOS2	P	Middle positive power supply source driver.
43	VPOS1	P	Lowest positive power supply source driver.
44	VNEG2	P	Middle Negative power supply of source driver.
45	VNEG1	P	Lowest Negative power supply of source driver.
46	GND	P	Ground.
47	GND	P	Ground.
48	GND	P	Ground.
49	GND	P	Ground.
50	GND	P	Ground.

6. Electrical Characteristics

6.1 Absolute Maximum Ratings:

Parameter	Symbol	Rating		Unit
		Min	Max	
Logic Supply Voltage	VDD	-0.3	+5	V
Positive Supply Voltage	VPOS1~VPOS3	-0.3	+27.5	V
Negative Supply Voltage	VNEG1~VNEG3	-27.5	+0.3	V
Max. Drive Voltage Range	VPOS3 – VNEG3	0	+55	V
Gate on Supply voltage	VGH	-0.3	+55	V
Gate off Supply voltage	VGL	-32	+0.3	V
Supply range	VGH - VGL	-0.3	+55	V
Operating Temp. Range	TOTR	TBD	TBD	°C
Storage Temperature	TSTG	TBD	TBD	°C

6.2 Display Module DC characteristics

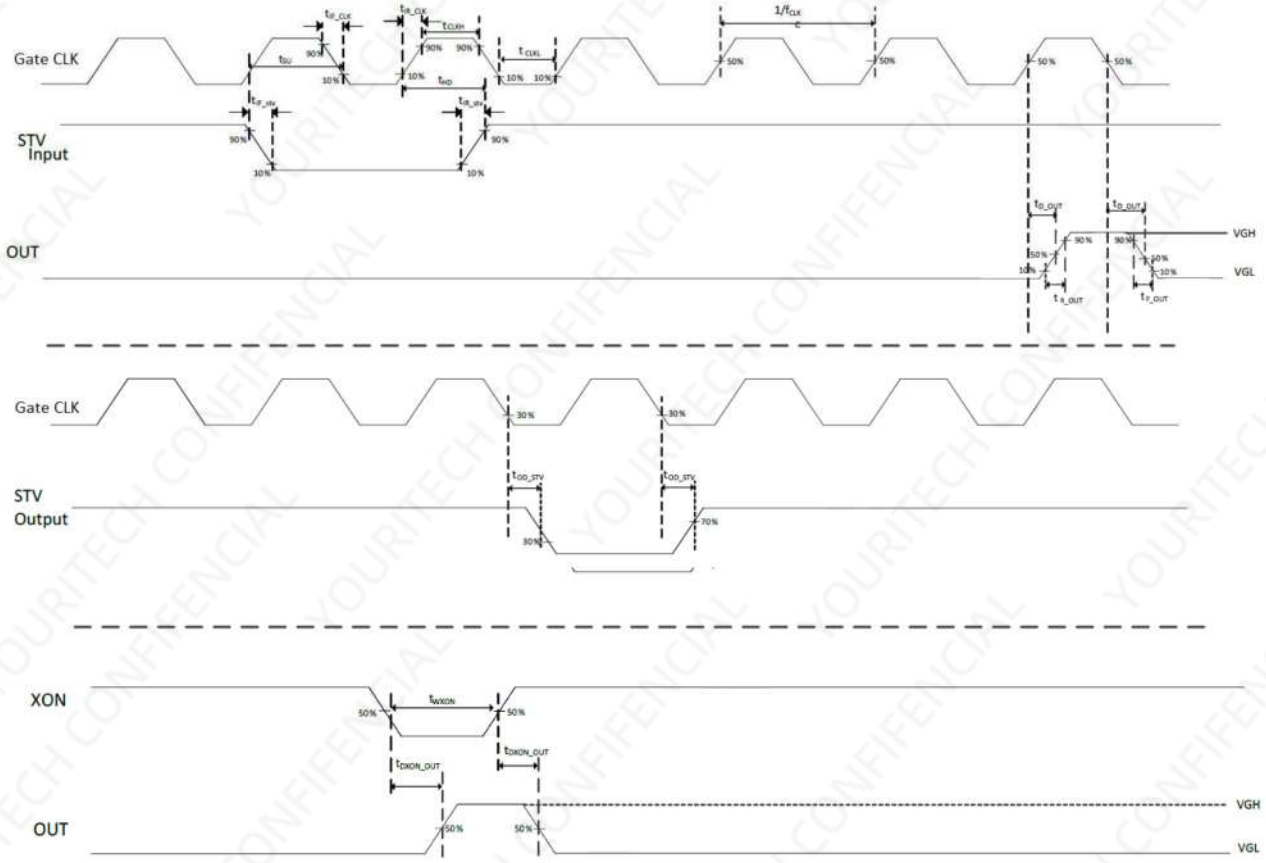
The following specifications apply for: VDD = 3.3V, TA = 25°C

Parameter	Symbol	Conditions 25°C	MIN.	TYP.	MAX.	Unit
Signal Ground	GND		--	0	--	V
Logic Voltage	VDD		TBD	TBD	TBD	V
Gate Negative Voltage	VGH		TBD	TBD	TBD	V
Gate Positive Voltage	VGL		TBD	TBD	TBD	V
Highest Source Negative Voltage	VNEG3		TBD	TBD	TBD	V
Highest Source Positive Voltage	VPOS3		TBD	TBD	TBD	V
Middle Source Negative Voltage	VNEG2		TBD	TBD	TBD	V
Middle Source Positive Voltage	VPOS2		TBD	TBD	TBD	V
Lowest Source Negative Voltage	VNEG1		TBD	TBD	TBD	V
Lowest Source Positive Voltage	VPOS1		TBD	TBD	TBD	V
Border Voltage	VBorder		TBD	TBD	TBD	V
Common Voltage	VCOM		TBD	TBD	TBD	V
Common Current	ICOM		--	TBD	TBD	V
Logic Current	IDD		--	TBD	TBD	mA
Gate Negative Current	IGL		--	TBD	TBD	mA
Gate Positive Current	IGH		--	TBD	TBD	mA
Highest Source Negative Current	INEG3		--	TBD	TBD	mA
Highest Source Positive Current	IPOS3		--	TBD	TBD	mA
Middle Source Negative Current	INEG2		--	TBD	TBD	mA
Middle Source Positive Current	IPOS2		--	TBD	TBD	mA
Lowest Source Negative Current	INEG1		--	TBD	TBD	mA
Lowest Source Positive Current	I_{POS1}		--	TBD	TBD	mA
Operating Max. Average Power (@ V_{NEG3}/ V_{POS3})	P		--	TBD	TBD	W
Standby power	PSTBY	25°C	--	--	TBD	V

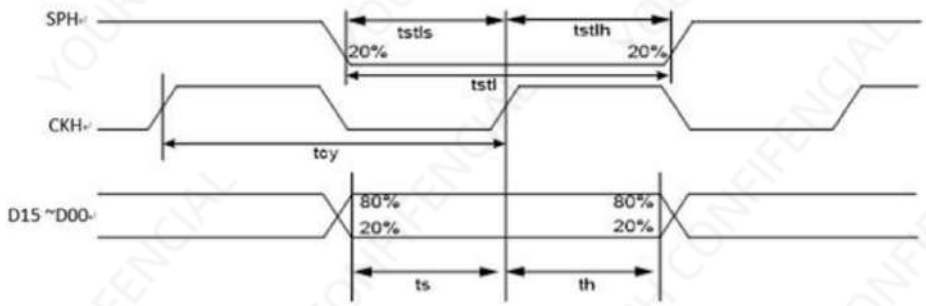
6.3 Panel AC Characteristics

Gate Parameter	Symbol	Condition	Min	Typ	Max	Unit
Gate clock frequency	f_{CLK}	In cascade connection	-	-	200	kHz
Gate clock pulse high period	t_{CLKH}		500	-	-	ns
Gate clock pulse low period	t_{CLKL}		500	-	-	ns
Gate clock rise time	t_{IR_CLK}		-	-	100	ns
Gate clock fall time	t_{IF_CLK}		-	-	100	ns
SPV setup time	t_{SU}		100	-	t_{CLKH}-100	ns
SPV hold time	t_{HD}		100	-	t_{CLKL}-100	ns
SPV rise time	t_{IR_STV}		-	-	100	ns
SPV fall time	t_{IF_STV}		-	-	100	ns
STV output delay from Gate CLK	t_{OD_STV}		-	-	500	ns
Gate output delay time from Gate CLK	t_{D_OUT}		-	-	2	us
Gate Output rise time, output pins	t_{R_OUT}		-	-	1	us
Gate Output fall time, output pins	t_{F_OUT}		-	-	1	us
XON pulse width	t_{WXON}		10	-	-	us
Output delay time from XON	t_{DXON_OUT}		-	-	20	us
Clock CKH cycle time	tcy	-	16.66			ns
D15…D0 setup time	ts	-	4			ns
D15...D0 hold time	th	-	4			ns
SPH setup time	tstls	-	6			ns
SPH hold time	tstlh	-	6			ns
SPH low-level pulse width	tstl		1		3	clk
LEH on delay time	tLEdly	-	44 x tcy			ns
LEH high-level pulse width	tLE	-	300			ns
LEH off delay time	tLEoff	-	14 x tcy			ns
VDD rise time	Ton	-	-	-	20	ms
VDD fall time	Toff	-	-	-	20	ms
VDD waiting time	Toff-on	-	700	-	-	ms

Gate Clock , SPV and Gate Output Timing



Source Clock and Date and SPH Timing



Source Output Latch Control Timing

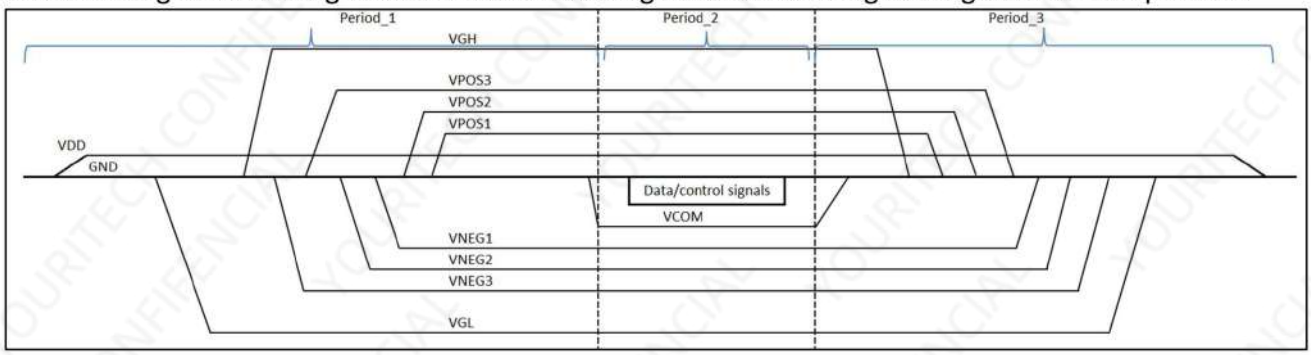
Refresh Rate

The module applied at a maximum refresh rate of TBD Hz.

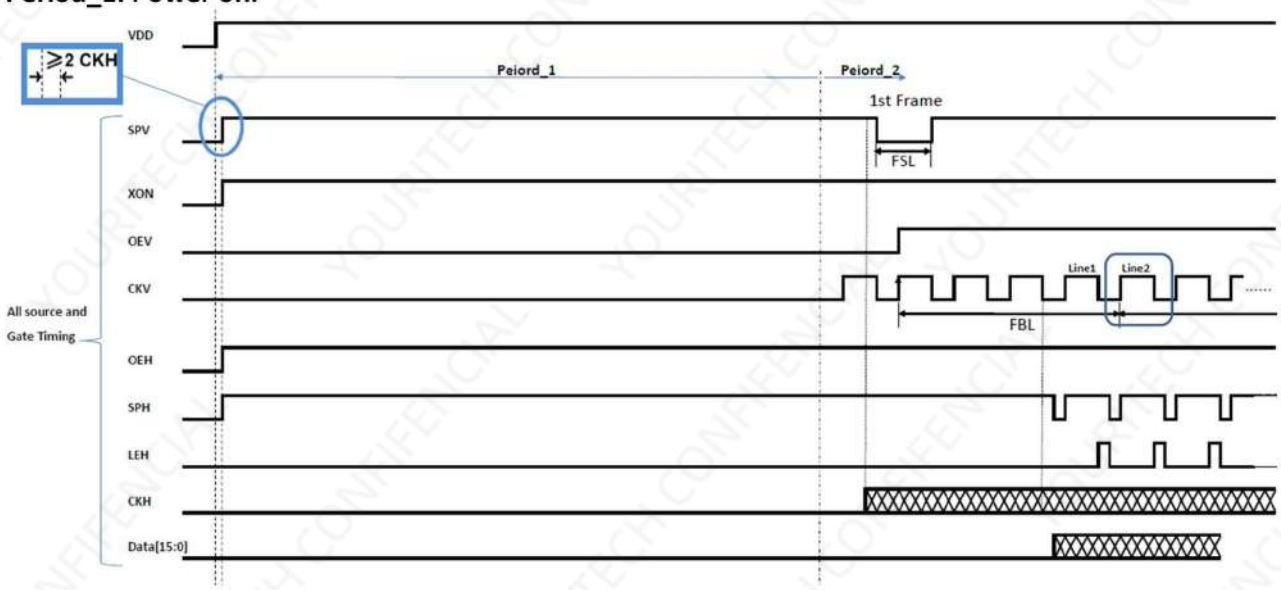
	Min	Max
Refresh Rate	-	TBD Hz

Controller Timing

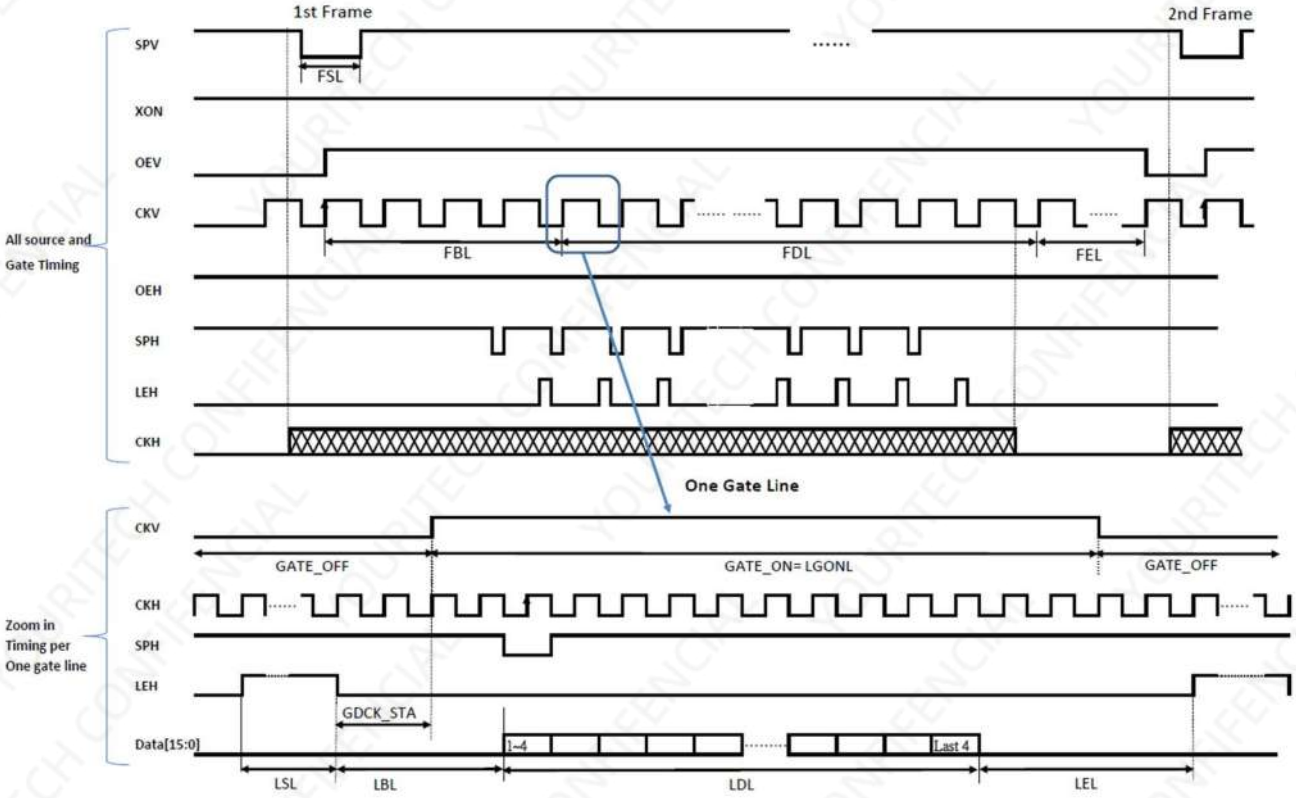
The following whole timing chart are included with gate and source signals together for this product.



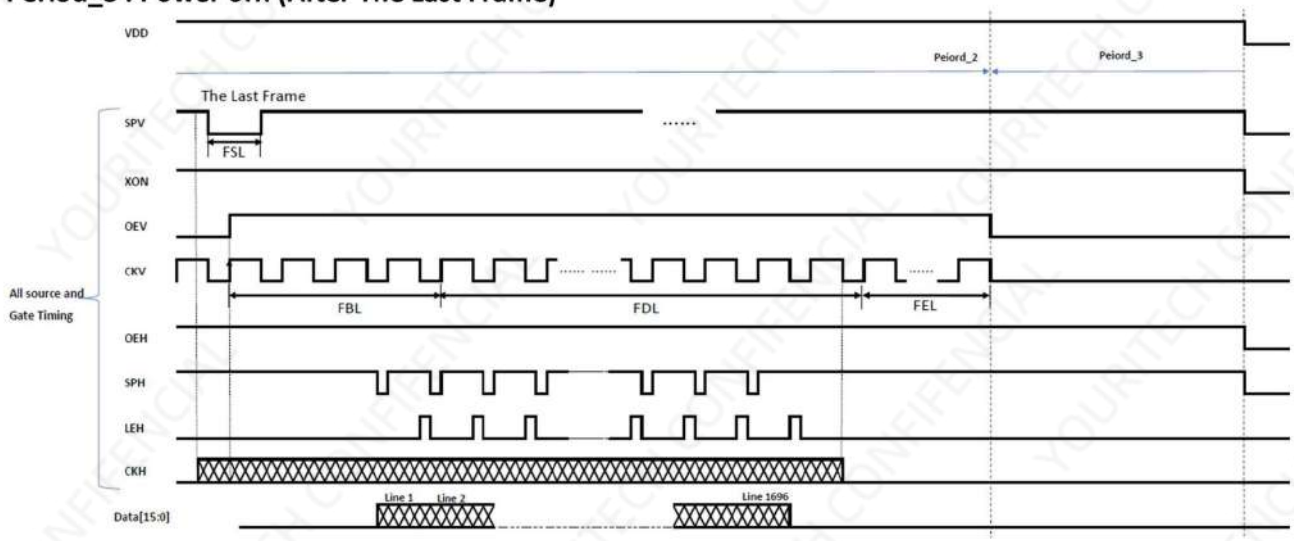
Period_1: Power on.



Period_2 : Display period.



Period_3 : Power off. (After The Last Frame)

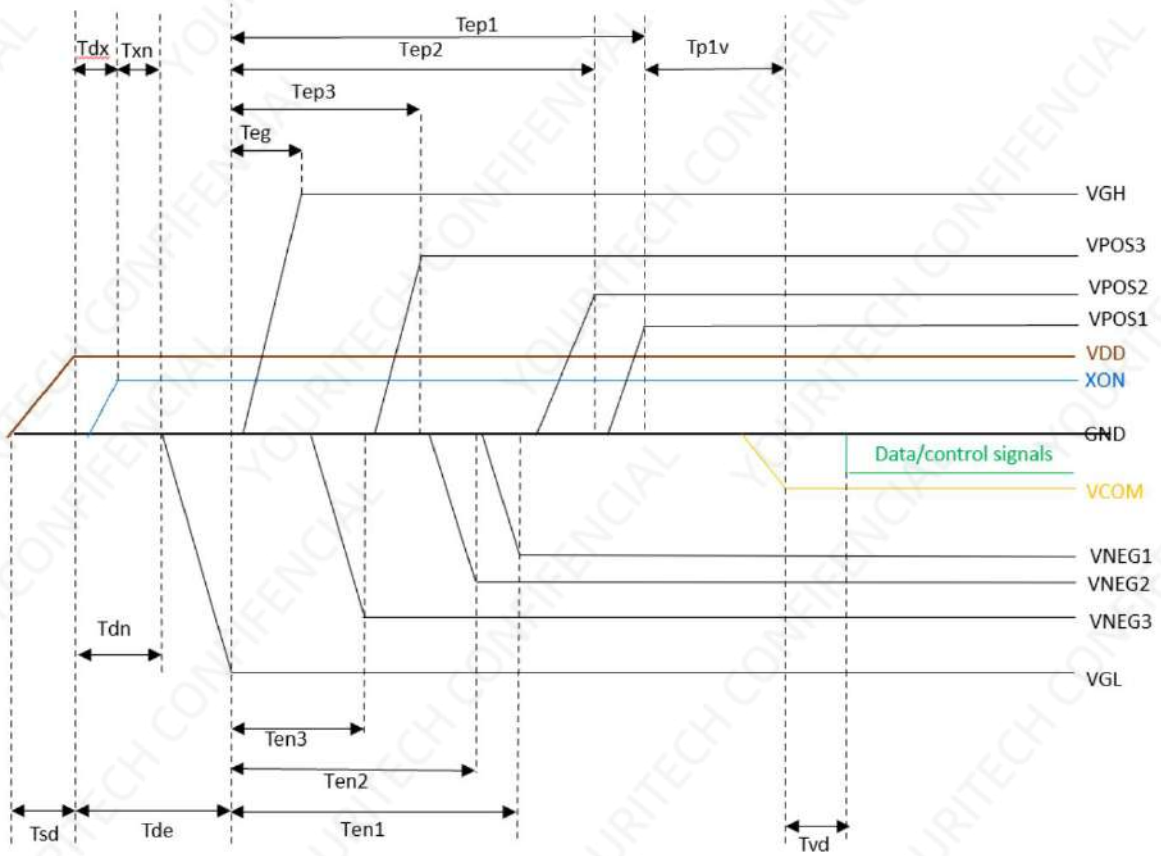


7. Power Sequence

POWER ON

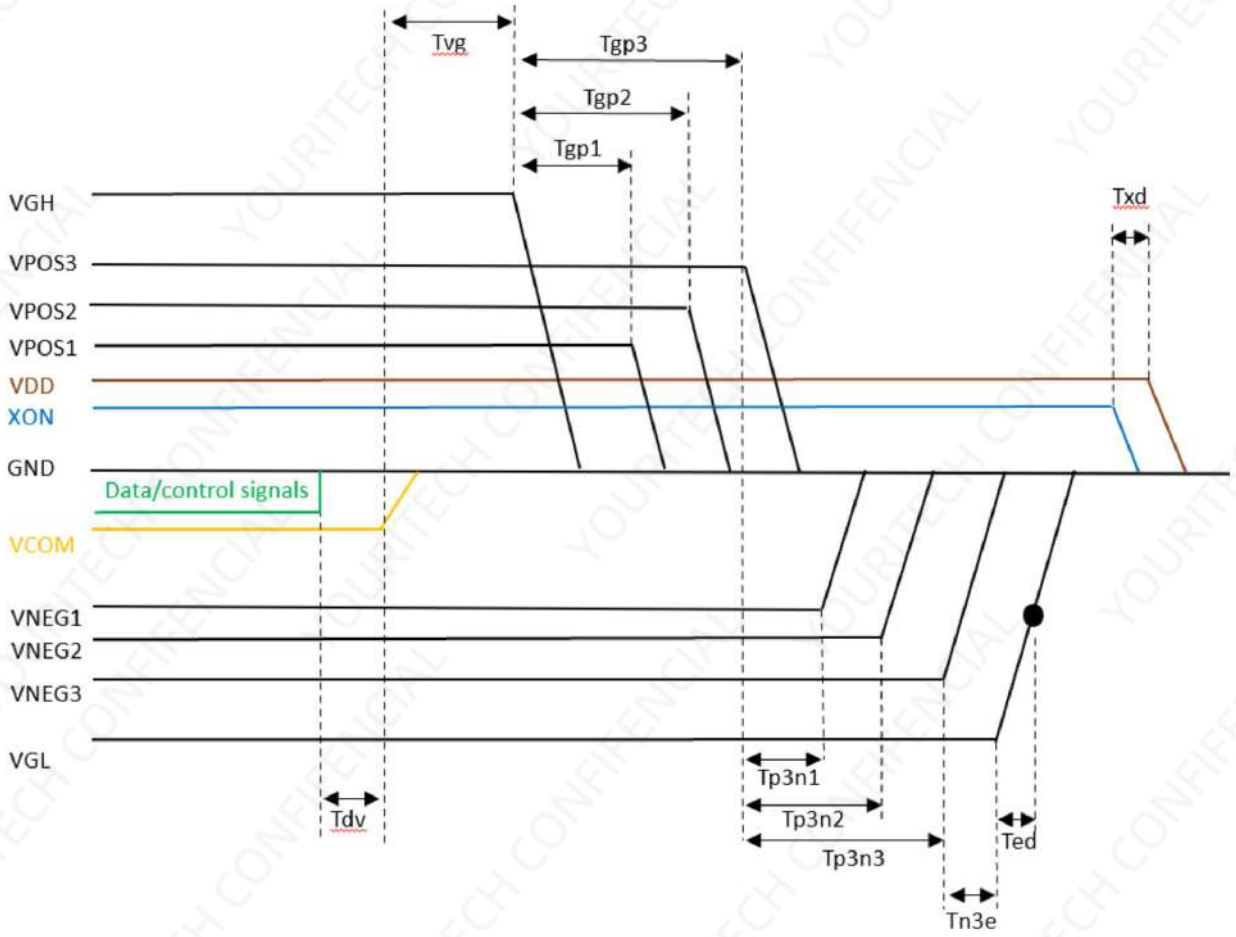
Power Rails must be sequencedin the following order：

GND → VDD → VGL → VGH → VNEG3 → VPOS3 → VNEG2 → VNEG1 → VPOS2 → VPOS1 → VCOM



NO		Description	Min	Max	Remark (Period time)
1	Tsd	VDD(3.3V)power on time	30us	18ms	GND – 100% VDD
2	Tdx	VDD to XON high	0us	-	100% VDD – 100% XON
3	Txn	XON high to VGL start	0us	-	100% XON – 0% VGL
4	Tdn	VDD to VGL start	0us	-	100% VDD – 0% VGL
5	Tde	VDD to VGL	1000us	-	100% VDD – 100% VGL
6	Teg	VGL to VGH	1000us	-	100% VGL – 100% VGH
7	Ten3	VGL to VNEG3	2000us	-	100% VGL – 100% VNEG3
8	Ten2	VGL to VNEG2	4000us	-	100% VGL – 100% VNEG2
9	Ten1	VGL to VNEG1	5000us	-	100% VGL – 100% VNEG1
10	Tep3	VGL to VPOS3	3000us	-	100% VGL – 100% VPOS3
11	Tep2	VGL to VPOS2	6000us	-	100% VGL – 100% VPOS2
12	Tep1	VGL to VPOS1	7000us	-	100% VGL – 100% VPOS1
13	Tp1v	VPOS1 to VCOM	0us	-	100% VPOS1 – 100% VCOM
14	Tvd	VCOM to SPH high	100us	-	100% VCOM – 10%/90% Data

Day Mode POWER OFF



NO		Description	Min	Max	Remark
1	Tdv	SPH off to VCOM off	100µs	-	10%/90% Data -- 100% VCOM
2	Tvg	VCOM off to VGH off	0µs	-	100% VCOM – 100% VGH
3	Tgp1	VGH off to VPOS1 off	0µs	-	100% VGH – 100% VPOS1
4	Tgp2	VGH off to VPOS2 off	100µs	-	100% VGH – 100% VPOS2
5	Tgp3	VGH off to VPOS3 off	200µs	-	100% VGH – 100% VPOS3
6	Tp3n1	VPOS3 off to VNEG1 off	0µs	-	100% VPOS3 – 100% VNEG1
7	Tp3n2	VPOS3 off to VNEG2 off	100µs	-	100% VPOS3 – 100% VNEG2
8	Tp3n3	VPOS3 off to VNEG3 off	200µs	-	100% VPOS3 – 100% VNEG3
9	Tn3e	VNEG3 off to VGL off	0µs	-	100% VNEG3 – 100% VGL
10	Ted	VGL off to -7.4V	0.5s	-	VGL-Discharged point @ -7.4 Volt
11	Txd	XON off to VDD off	0µs	-	100% XON – 100% VDD

8. Optical Characteristic

8.1 Specification

Symbol	Parameter	Conditions	Temperature	Min	Typ.	Max	Unit	Note
R	Reflectance	White	25°C	30	34	-	%	Note 8-1
CR	Contrast Ratio	-	25°C	15	22	-	-	-
T_{update}	Update time	-	25°C	-	12	-	sec	-

Symbol	Parameter	Conditions	Temperature	L* Typ.	a* Typ.	b* Typ.	△E2000 Max.	Note
WS	White State L*/a*/b* value	White	25°C	66.5	-4	0	6	Note 8-1
DS	Dark State L*/a*/b* value	Dark	25°C	12	7	-11	6	Note 8-1
RS	Red State L*/a*/b* value	Red	25°C	26.5	41	30	6	Note 8-1
YS	Yellow State L*/a*/b* value	Yellow	25°C	62	-11	65	6	Note 8-1
BS	Blue State L*/a*/b* value	Blue	25°C	34	3.5	-37	6	Note 8-1
GS	Green State L*/a*/b* value	Green	25°C	35	-22	15	8	Note 8-1

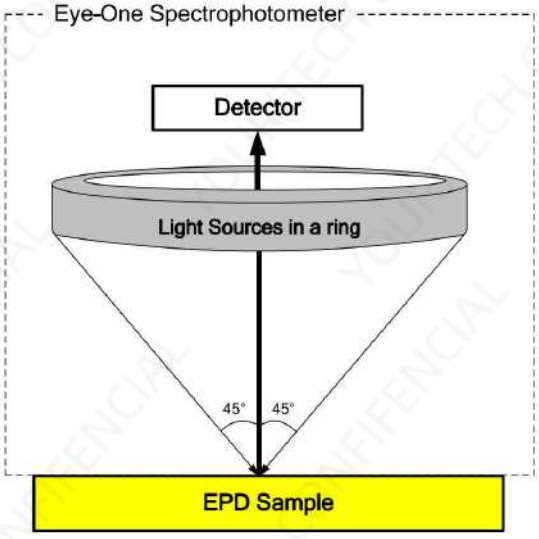
WS: White state,DS: Dark state,RS: Red state,YS: Yellow state,BS: Blue state,GS: Green state

Note 8-1:Luminance meter: Eye-One Pro3 plus Spectrophotometer

8.2 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (Rl) and the reflectance in a dark area (Rd) :

CR = Rl/Rd



8.3 Reflection Ratio

The reflection ratio is expressed as：

$R = \text{Reflectance Factor}_{\text{white board}} \times (L_{\text{center}} / L_{\text{white board}})$

L_{center} is the luminance measured at center in a white area (R=G=B=1). $L_{\text{white board}}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.

9. Reliability Test

	TEST	CONDITION	REMARK
1	High Temperature Storage	T = 60℃35% RH, 240Hrs Test in White pattern	IEC 60 068-2-2Bb
2	Low Temperature Storage	T = -25℃, 240Hrs Test in White pattern	IEC 60 068-2-1Ab
3	High Temperature Operation	T = 50℃30% RH, 240Hrs 150s interval between updates	IEC 60 068-2-2Be
4	Low Temperature Operation	T = 0℃, 240Hrs 150s interval between updates	IEC 60 068-2-1Ae
5	High-Temperature, High-Humidity Operation	T = +40℃, RH = 90%, 240Hrs 150s interval between updates	IEC 60 068-2-78
6	High Temperature, High-Humidity Storage	T = 60℃ 80% RH, 240Hrs Test in White pattern	IEC 60 068-2-78
7	Heat Shock	-25℃(30 min) ~60℃(30 min) 50 cycle, 1Hr/cycle Test in White pattern	IEC 068-2-14Nb
8	Electrostatic Discharge	(Machine model) +/- 200V ; 0Ω, 200pF	IEC 62180 Non-operation

Actual EMC level to be measured on customer application.

Note：

1. The protective film must be removed before temperature test.
2. For operation test, image update interval time 150s.

< Criteria >

In the standard conditions, there is not display function NG issue occurred.

All the cosmetic specification is judged before the reliability stress.

10. Matched Development Kit

Our Development Kit designed for SPI E-paper Display aims to help users to learn how to use E-paper Display more easily. It can refresh black-white E-paper Display, three-color (black, white and red/Yellow) E-paper Display and four-color(black, white, red and yellow) YOURITECH's E-paper Display. And it is also added the functions of USB serial port, FLASH chip, font chip, current detection ect.
Development Kit consists of the development board and the pinboard.

Supported development platforms include STM32, ESP32, ESP8266, Arduino UNO, etc.

11. Handling, Safety and Environmental Requirements

WARNING
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

Data sheet status	
Product specification	The data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and dose not form part of the specification.	

Product Environmental certification
RoHS

12. Precautions

(1) Do not apply pressure to the EPD panel in order to prevent damaging it.

(2) Do not connect or disconnect the interface connector while the EPD panel is in operation.

(3) Do not touch IC bonding area. It may scratch TFT lead or damage IC function.

(4) Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.

(5) If the EPD Panel / Module is not refreshed every 24 hours, a phenomena known as "Ghosting" or "Image Sticking" may occur. It is recommended to refreshed the ESL / EPD Tag every 24 hours in use case. It is recommended that customer ships or stores the ESL / EPD Tag with a completely white image to avoid this issue

(6) High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel's performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time.