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Cover glass

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Custom Display

Production Custom designs Installation

Mechanical design



Project No. 项目编号	ET101WU13-TT
Customer 客户名称	
Module No. 客户型号	
Product type 产品内容	Standard LCD Module TFT: 1200*RGBx1920Dots 10.1" TFT LCD+CTP

客户确认Customer Approval

项目负责人Project Manager	
品质主管Director of Quality	
采购工程师Purchasing Engineer	

PREPARED BY	CHECKED BY	APPROVED BY



1. Introduction

1.1 Scope of application

This specification applies to the LCD module that is supplied by YOURITECH Technology CO., LTD.

LCD specification: Dots 1200xRGBx1920

As to basic specification of the driver IC, refer to the IC (HX8279D) specification and data book.

All material & processing of the LCD module should be Lead Free.

1.2 TFT features:

Structure: TFT PANNEL+IC +FPC+BL+CTP

ALL Viewing Type LCD

1200 dot-segment and 1920 dot-common outputs;

16.7M Color can be selected by software;

White LED back light;

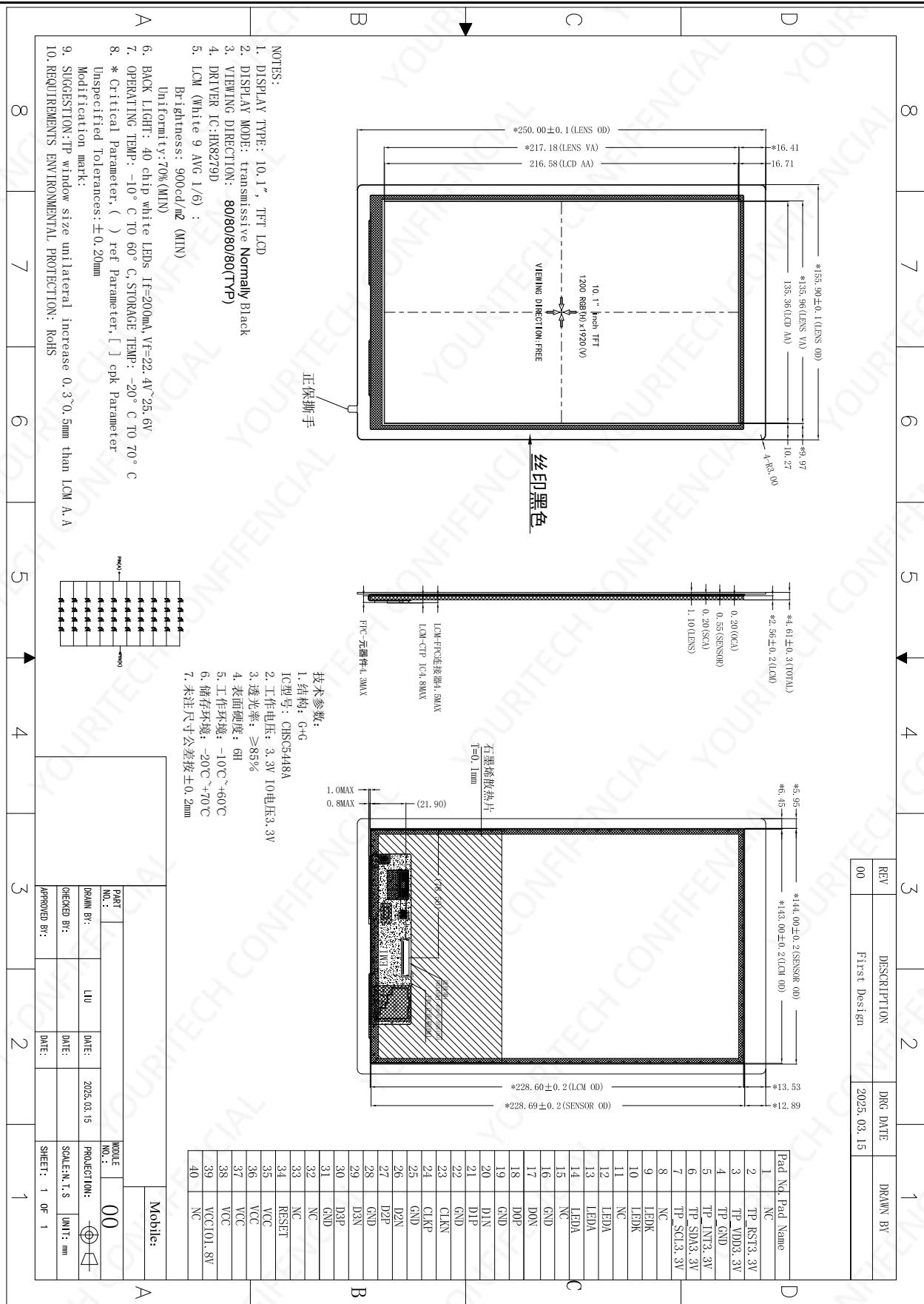
4lane MIPI interface



2. LCM General specification

ITEM	Standard value	Unit
LCD Type	Normally Black	--
Drive element	TFT active matrix	--
Number of pixels	1200*3RGB(H)X1920(V)	Dots
Pixel arrangement	RGB Vertical Stripe	--
Pixel Pitch (W*H)	0.1128(H)×0.1128(V)	mm
Active area	135.36(H)x216.58(V)	mm
Viewing direction	ALL O'CLOCK	--
TFT Driver IC	HX8279D	--
TFT interface	4lane MIPI interface	--
Approx. Weight	TBD	g
LCM Size(W*H*T)	143.00(W) ×228.60(H) ×2.56(T)	mm
LCM+CTP Size(W*H*T)	155.90(W)x 250.00(H) x 4.61(T)	mm
Touch structure	G+G	--
Touch Driver IC	CHSC5448A	--
Touch Interface	I2C	--





3. Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
LCM Operating Temperature	T _{OPR}	-10	+60	°C
LCM Storage Temperature	T _{STG}	-20	+70	°C
TP Operating Temperature & Humidity(20% ~ 90%RH)	T _{OPR}	-10	+60	°C
TP SStorage Temperature & Humidity(20% ~ 90%RH)	T _{STG}	-20	+70	°C
Humidity	RH	--	90	%

4. Electrical Characteristics

4.1 TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage for I/O	VDDIO	--	1.8	--	V
Supply Voltage for(DC/DC)	VDD	--	3.3	--	V

4.2 Back-Light Unit Characteristics

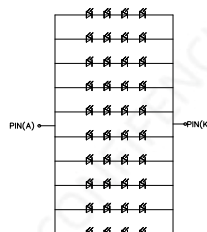
The back-light system is an edge-lighting type with 40 white LEDs. The characteristics of the back-light are shown in the following tables.

Characteristics	Symbol	Min.	Type	Max.	Unit	Notes
Forward Voltage	V _F	22.4	--	25.6	V	--
Forward current	I _F	--	200	--	mA	--
Luminance(With LCD+CTP)	L _v	900	--	--	cd/m ²	--
LED life time	N/A	--	30,000	--	Hr	Note 1

Note:

- (1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=20mA/LED. The LED life time could be decreased if operating I_L is larger than 25mA/LED.

Backlight circuit diagram shown in below:



5. Module Function Description

Pin No.	Symbol	LCM Functional	Notes
1	NC	No Connection.	
2	CTP_RESET 3.3V	CTP_Reset Signal input pin.	
3	CTP_VDD 3.3V	power supply for DC/DC circuit	
4	GND	Power Ground	
5	CTP_INT 3.3V	CTP_STOP Singnal	
6	CTP_SDA 3.3V	CTP_Data Singnal	
7	CTP_SCL 3.3V	CTP_Clock Singnal	
8	NC	No Connection.	
9	LEDK	Power supply for backlight cathode input terminal.	
10	LEDK	Power supply for backlight cathode input terminal.	
11	NC	No Connection.	
12	LEDA	Power supply for backlight anode input terminal.	
13	LEDA	Power supply for backlight anode input terminal.	
14	LEDA	Power supply for backlight anode input terminal.	
15	NC	No Connection.	
16	GND	Power Ground	
17	MIPI_D0N	High speed interface data differential signal input/output pins	
18	MIPI_D0P	High speed interface data differential signal input/output pins	
19	GND	Power Ground	
20	MIPI_D1N	High speed interface data differential signal input/output pins	
21	MIPI_D1P	High speed interface data differential signal input/output pins	
22	GND	Power Ground	
23	MIPI_CLKN	High speed interface clock differential signal input/output pins	
24	MIPI_CLKP	High speed interface clock differential signal input/output pins	
25	GND	Power Ground	
26	MIPI_D2N	High speed interface data differential signal input/output pins	
27	MIPI_D2P	High speed interface data differential signal input/output pins	
28	GND	Power Ground	
29	MIPI_D3N	High speed interface data differential signal input/output pins	
30	MIPI_D3P	High speed interface data differential signal input/output pins	
31	GND	Power Ground	
32	NC	No Connection.	
33	NC	No Connection.	
34	RESET 1.8V	Reset pin. Setting either pin low initializes the LSI	
35	VCC 3.3V	Booster circuit power supply	
36	VCC 3.3V	Booster circuit power supply	
37	VCC 3.3V	Booster circuit power supply	
38	VCC 3.3V	Booster circuit power supply	
39	IOVCC 1.8V	power supply for DC/DC circuit	
40	NC	No Connection.	

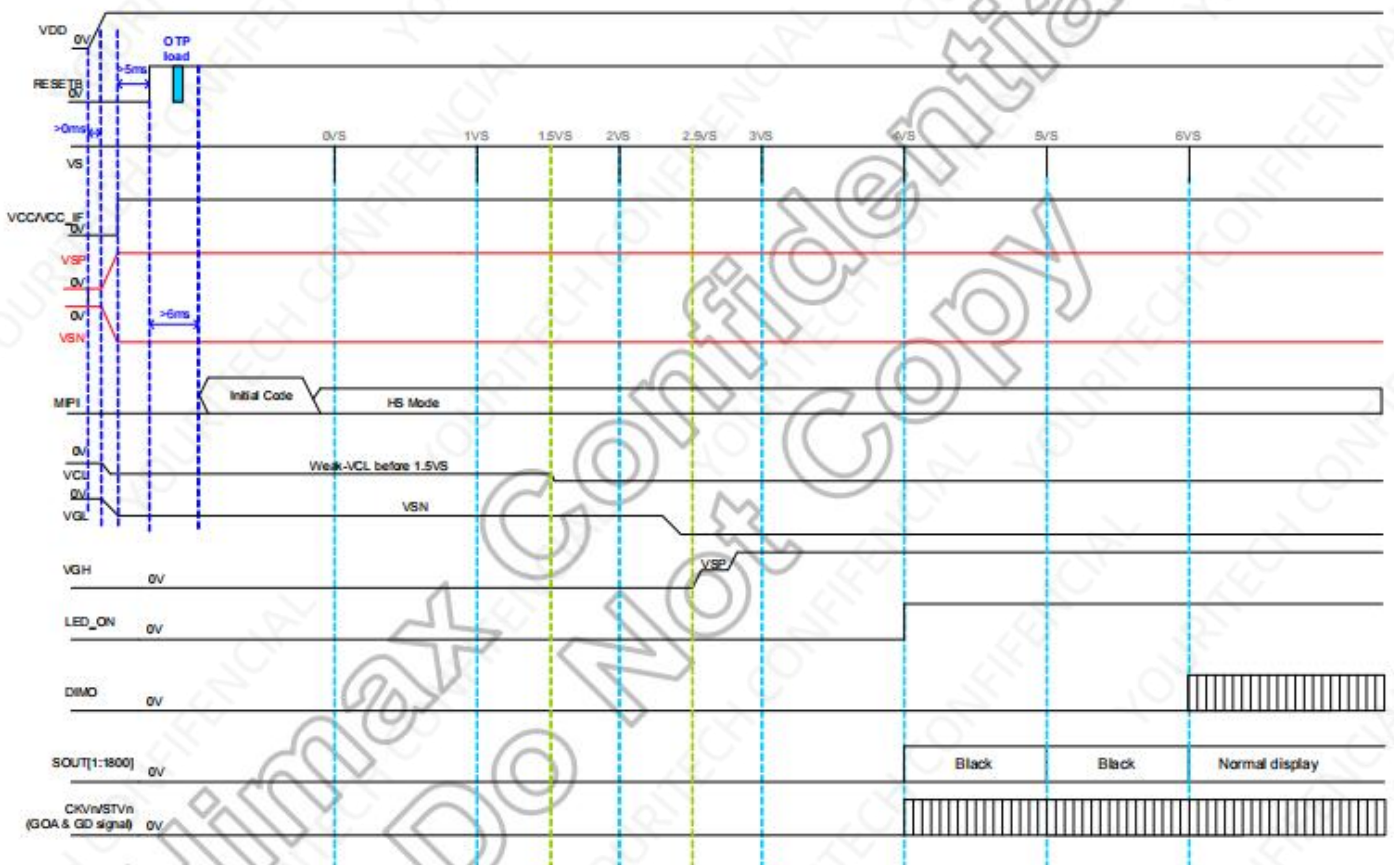


6. Timing Characteristics

Power on sequence PWRMD=0 → max. Power on time=7VS

After reset state or exit STB mode, the power on sequence will start.

To prevent the device from damage due to latch up, The VGL will be earlier than VGH. At 2.25VS the VGL negative high voltage will be generated via the external charge pump circuit. Then at 2.5VS the VGH positive high voltage can be generated via the external charge pump circuit. One SCHOTTKY diode is necessary between VGL and GND when VDD and VSP start at the same time.



Note: (1) Finish to write the GOA MUX (page1 registers) and GOA timing setting (page3 registers) within 50ms after reset pulls to high.

Figure 5.5: Power on sequence with PWRMD=0 and repair OP disable



Power off sequence PWRMD=0 → max. Power off time=5VS

When enter STB mode, the STBYB signal will be set to low. The power off sequence will start.

Power-off sequence

External VSP/VSN. Internal VGH/VGL.

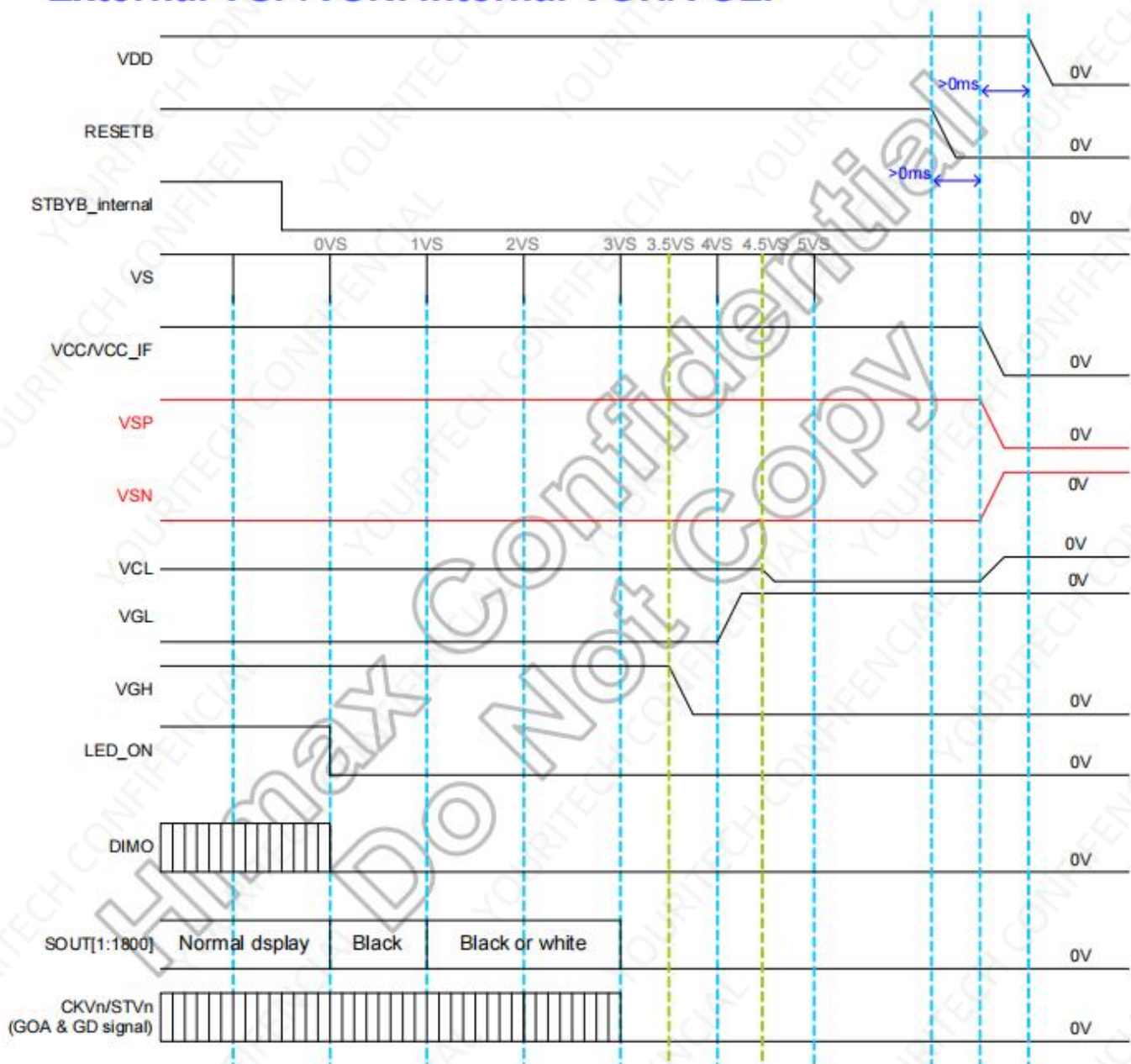
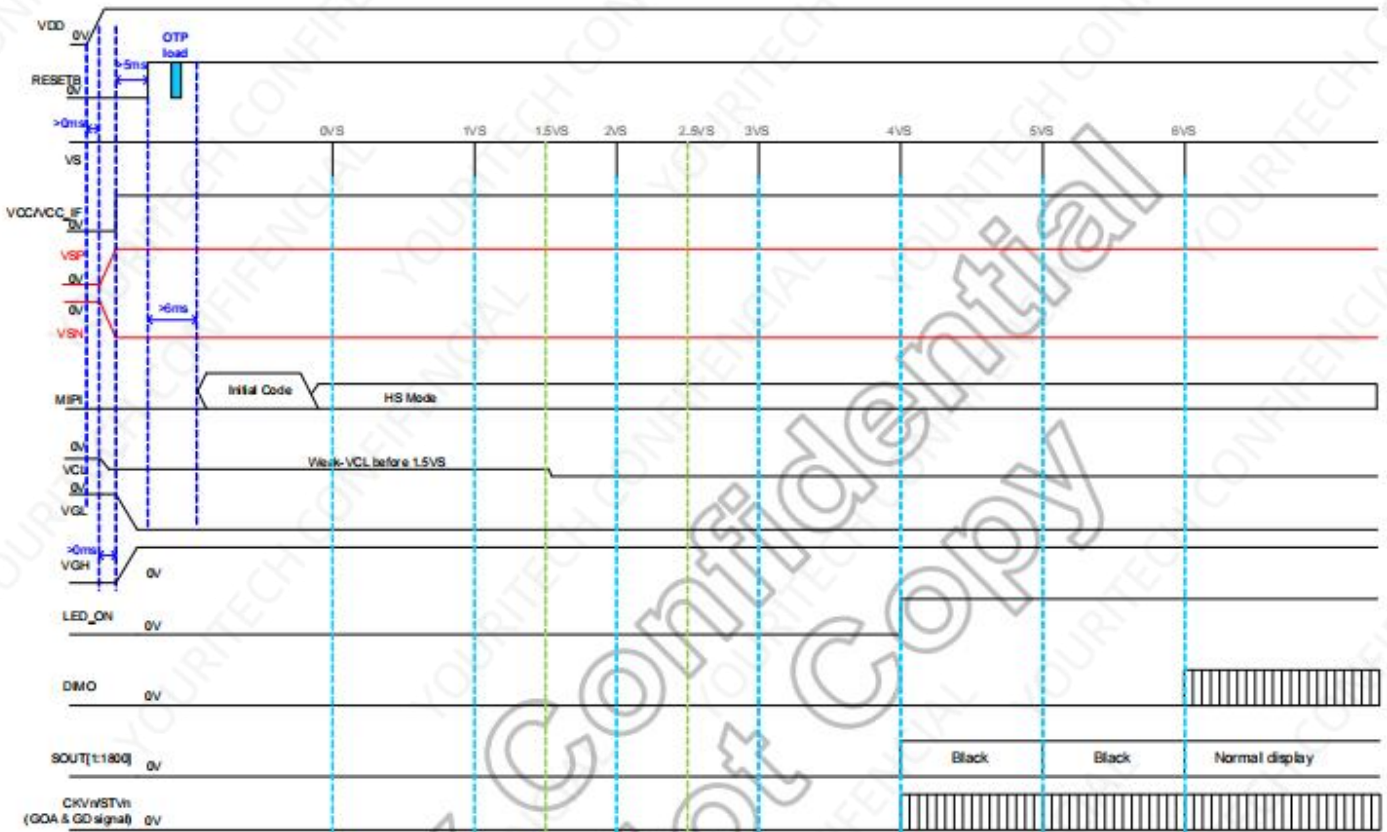


Figure 5.6: Power off sequence with PWRMD=0



Power on sequence PWRMD=1 → Max. Power on time=6VS

After reset state or exit STB mode, the power on sequence will start. One SCHOTTKY diode is necessary between VGL and GND when VDD and VSP start at the same time.



Note: (1) Finish to write the GOA MUX (page1 registers) and GOA timing setting (page3 registers) within 50ms after reset pulls to high

Figure 5.7: Power on sequence with PWRMD=1 and repair OP disable



Power off sequence PWRMD=1 → max. Power off time=4.5VS

When enter STB mode, the STBYB signal will be set to low then the power off sequence will start.

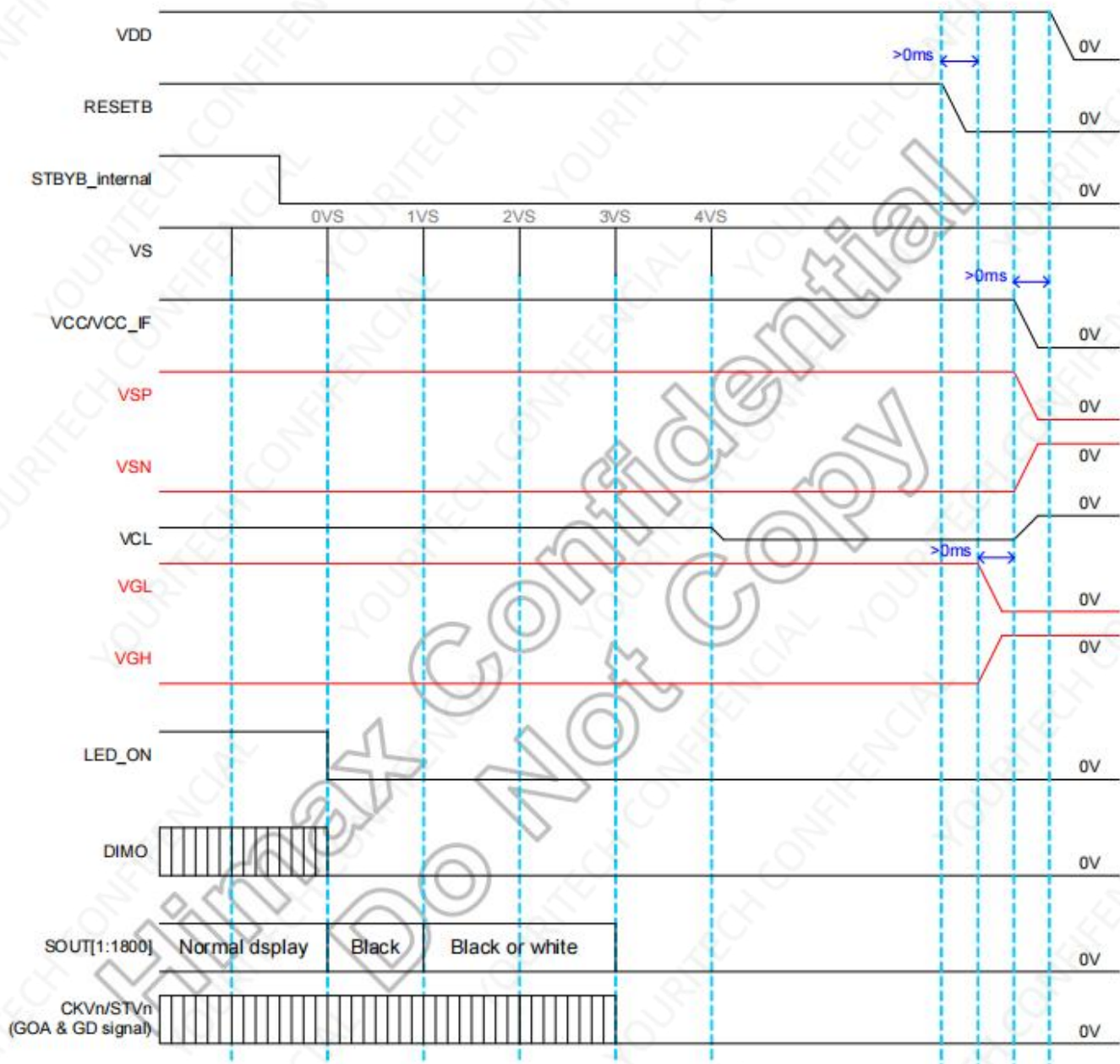


Figure 5.8: Power off sequence with PWRMD=1



MIPI AC characteristics

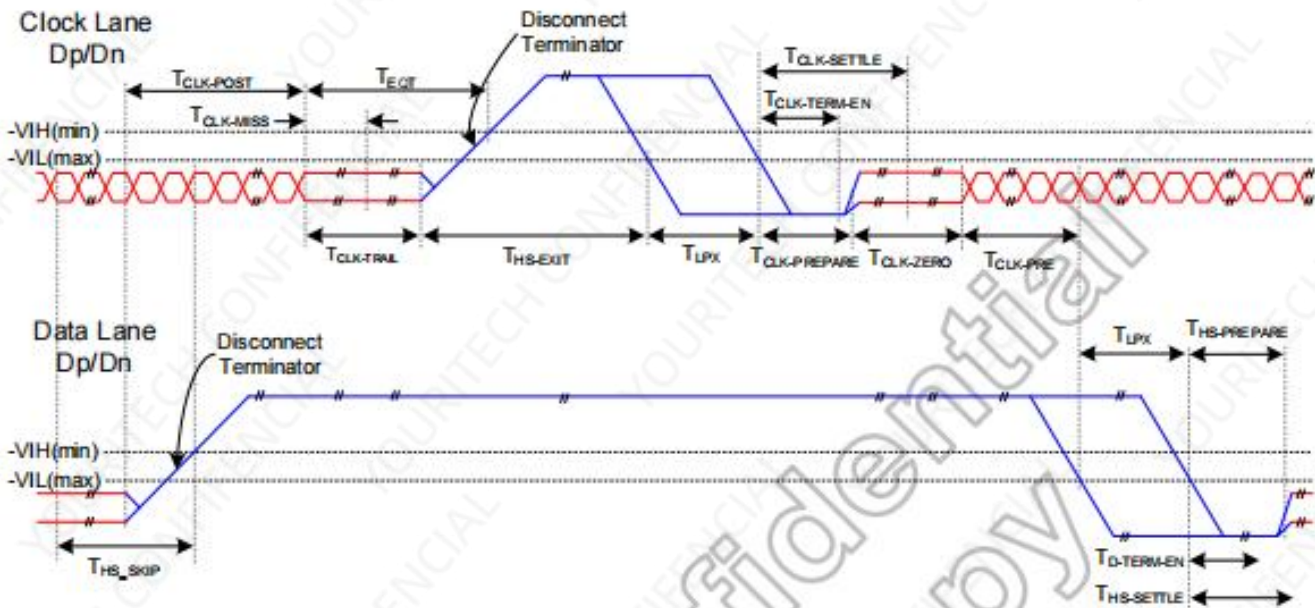


Figure 13.1: Switching the clock lane between clock transmission and low-power mode

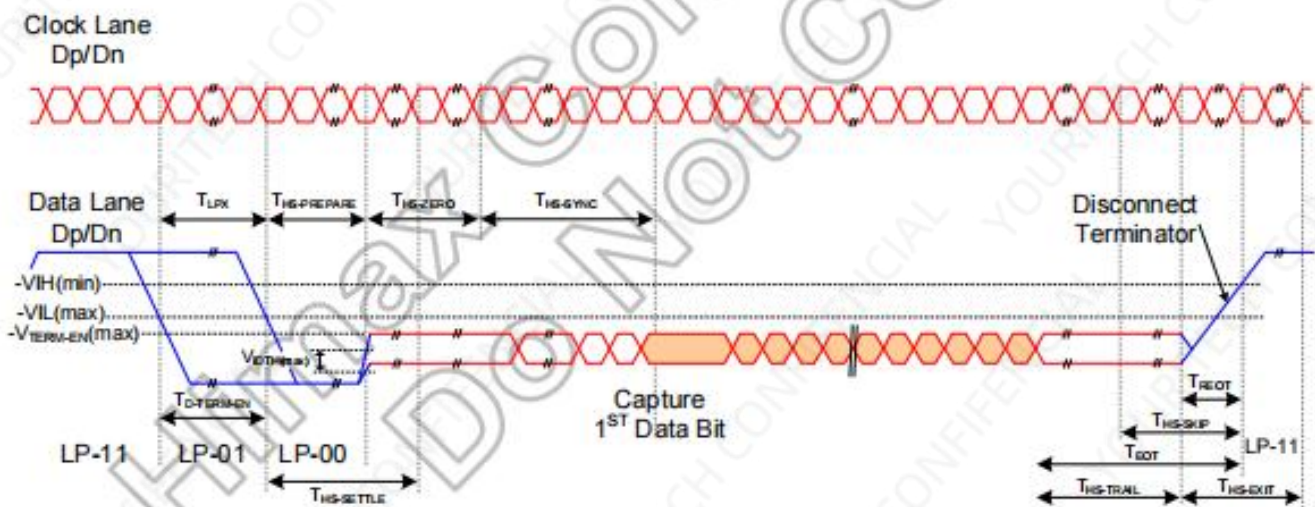


Figure 13.2: Timing of high-speed data transmission in bursts

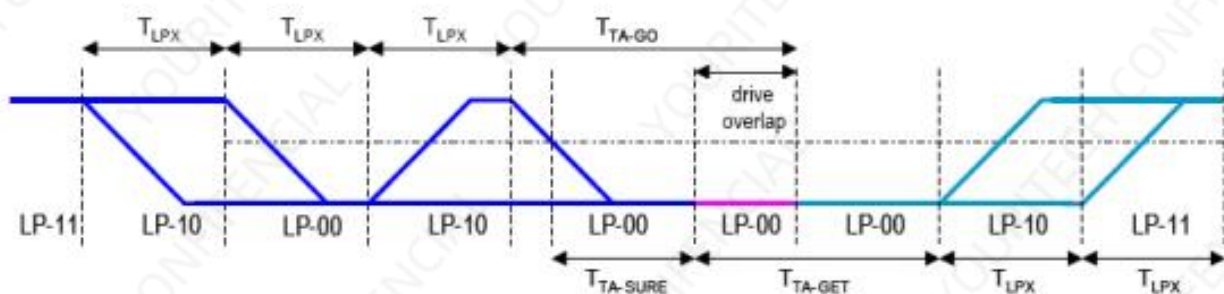


Figure 13.3: Turnaround Procedure



MIPI AC Characteristics

Parameter	Description	Spec.			Unit
		Min.	Typ.	Max.	
T_{REOT}	30%-85% rise time and fall time	-	-	35	ns
$T_{CLK-MISS}$	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.	-	-	60	ns
$T_{CLK-POST}^{*1}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of $T_{CLK-TRAIL}$.	60 ns + 52*UI (For DCS)	-	-	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8	-	-	ns
$T_{CLK-SETTLE}$	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of $T_{CLK-PRE}$.	95	-	300	ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$	-	38	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $T_{HSPREPRE}$.	85 ns + 6*UI	-	145 ns + 10*UI	ns
T_{EOT}	Time from start of $T_{HS-TRAIL}$ or $T_{CLK-TRAIL}$ period to start of LP-11 state	-	-	105ns+48*UI	-
$T_{HS-EXIT}^{(1)}$	time to drive LP-11 after HS burst	100	-	-	ns
$T_{HS-PREPRE}$	Time to drive LP-00 to prepare for HS transmission	40ns + 4*UI	-	85ns+6*UI	ns
$T_{HS-PREPRE} + T_{HS-ZERO}$	$T_{HS-PREPRE}$ + Time to drive HS-0 before the Sync sequence	145ns + 10*UI	-	-	ns
$T_{HS-SKIP}$	Time-out at RX to ignore transition period of EoT	40	-	55ns+4*UI	ns
$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60 + 4*UI	-	-	ns
T_{LPX}	Length of any Low-Power state period	50	-	-	ns
Ratio T_{LPX}	Ratio of $T_{LPX(MASTER)}/T_{LPX(SLAVE)}$ between Master and Slave side	2/3	-	3/2	-
T_{TA-GET}	Time to drive LP-00 by new TX	$5 \cdot T_{LPX}$			ns
T_{TA-GO}	Time to drive LP-00 after Turnaround Request	$4 \cdot T_{LPX}$			ns
$T_{TA-SURE}$	Time-out before new TX side starts driving	T_{LPX}	-	$2 \cdot T_{LPX}$	ns

Note: (1) For image transmission:

$T_{CLK-POST}$ min value =164 when MIPI max frequency per lane = 0.53Gbps.

$T_{CLK-POST}$ min value =112 when MIPI max frequency per lane = 1Gbps



Timing requirements for RESETB

When RESETB of the reset pin equals to Low, it will be in the condition of reset. When it is in the condition of reset, it will make the device recover the initial set.

However, in order to avoid the reset noise cause reset, there is a mechanism to judge about whether the reset is needed or not.

The closed interval of low can be shown as the following.

(VDD=1.7V~2.0V, VSS=0V, T_A=-20℃~+85℃)

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Reset low pulse width	Trst	-	20	-	-	μs

Table 13.5: Reset timing



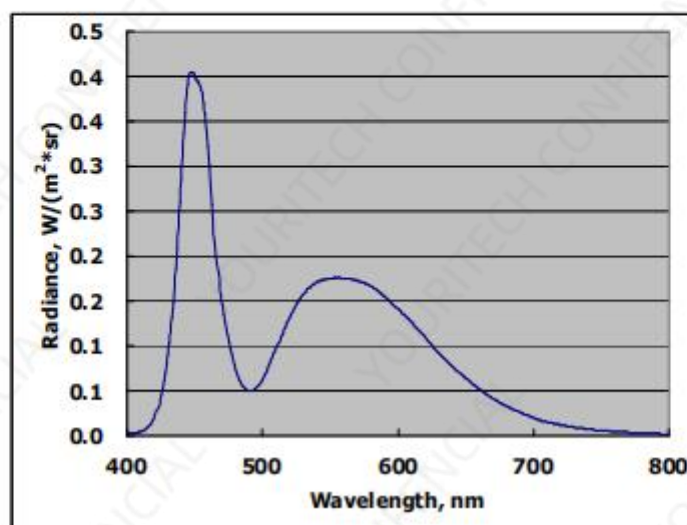
Figure 13.6: Reset timing



7. Optical Characteristics

Item		Symbol	Conditions	Specifications			Unit	Note	
				Min.	Typ.	Max.			
Transmittance (w/o APCF)		T%	Viewing normal angle $\theta_x = \theta_y = 0^\circ$	3.53%	4.04%		%	All left side data are based on INX's following condition – 1.LC : AAS . 2.CF : CG 70% CF. 3.Light Source : INX LED BLU. 4.Polarizer : CF:SRW062APN1LT4 TFT:SRW062AWL2/APFV3 5.Machine : DMS 803, (ConoScope for View Angle). 6. VLC dark ≤ 0.3 V, VLC white ≥ 4.1 V 7.Back light structure: Diffuser+BEF+BEF+ Diffuse	
Contrast Ratio		CR		800	1000		--		
Response Time		T _{on} + T _{off}			25		ms		
Viewing Angle	Hor.	θ_{x+}	80	85		deg.			
		θ_{x-}	80	85					
	Ver.	θ_{y+}	80	85					
		θ_{y-}	80	85					
CF only Color Chromaticity (CIE 1931)	Red	R _x	Viewing normal angle $\theta_x = \theta_y = 0^\circ$				-		Under C light Simulation
		R _y					-		
	Green	G _x					-		
		G _y					-		
	Blue	B _x					-		
		B _y					-		
	White	W _x		0.28	0.3	0.32	-		
		W _y		0.305	0.325	0.345	-		
	Color Gamut					65		%	

*Note(1) INX LED BLU Spectrum:



***Note (2) Definition of Contrast Ratio (CR):**

The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = L_{63} / L_0$$

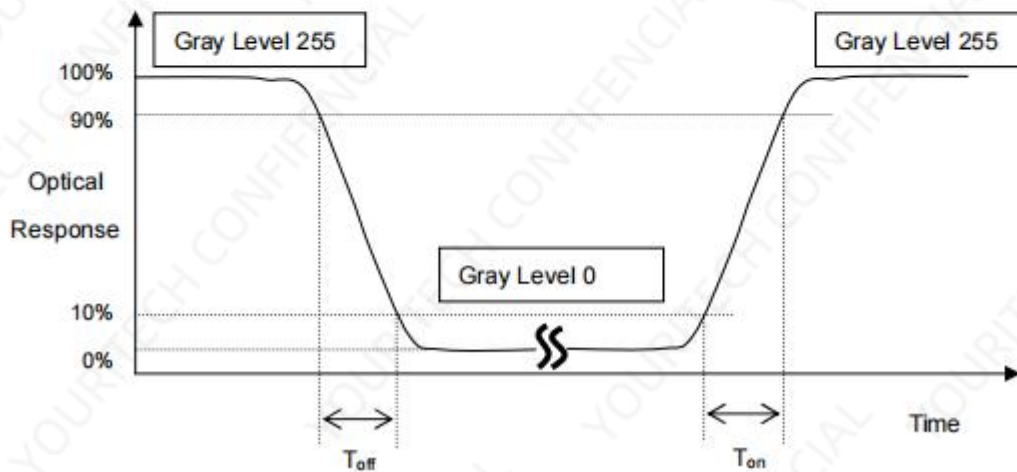
L63: Luminance of gray level 63

L 0: Luminance of gray level 0

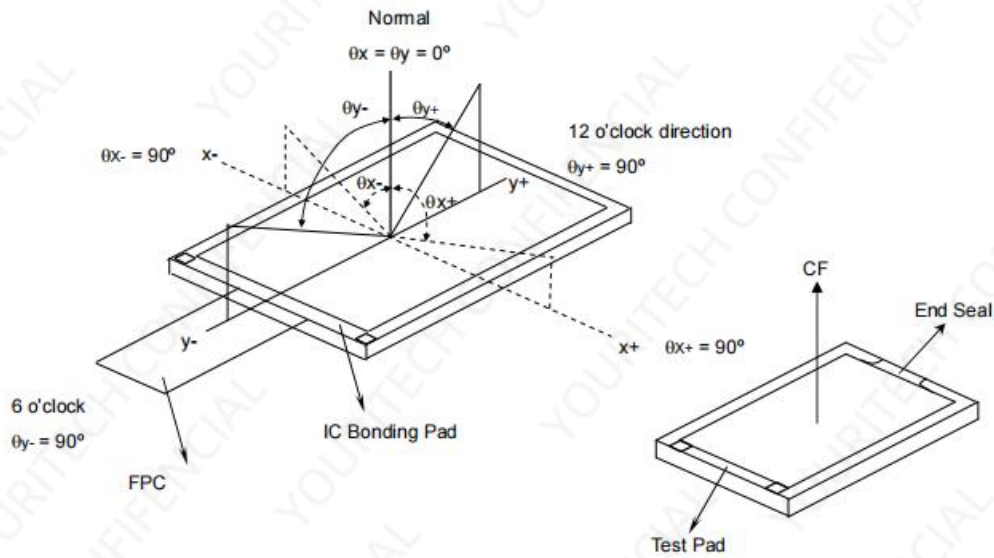
$$\text{CR} = \text{CR} (5)$$

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (5).

***Note (3) Definition of Response Time (T_{on} , T_{off}):**

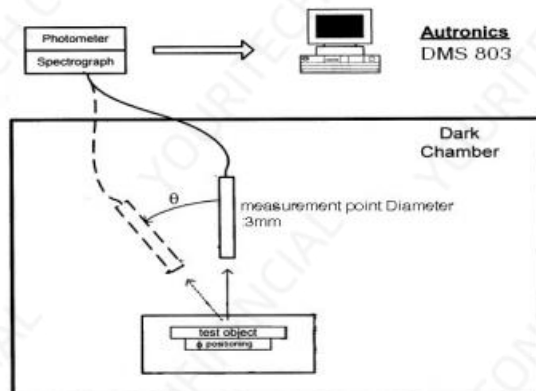


*Note(4) Definition of Viewing Angle

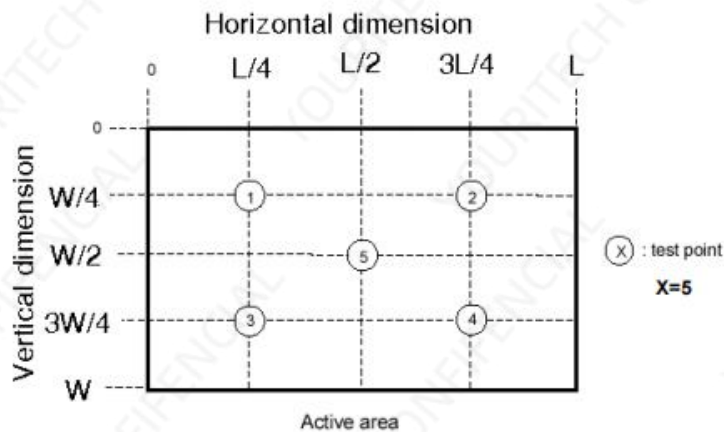


*Note (5) Measurement Set-Up:

The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



*Note (6)



8. Reliability Test Item

No.	Test Item	Test Condition	Notes
1	High Temp. Storage	+70°C / 96H	1. Functional test is OK. Missing Segment, short, unclear segment non-display, display abnormally and liquid crystal leakage un-allowed. 2. No low temperature bubbles, end seal loose and fall, frame rainbow.
2	Low Temp. Storage	-20°C / 96H	
3	High Temp. Operating	+60°C / 96H	
4	Low Temp. Operating	-10°C / 96H	
5	High Temperature / Humidity storage	50°C x 90%RH / 96H	
6	Thermal and cold shock	Static state, -10°C (30min) ~60°C (30min), 10 cycles	

9. Packing Method---TBD

- END -

