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Custom designs
Installation

Mechanical design



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Project No. 项目编号	ET101WX03-T
Customer 客户名称	
Module No. 客户型号	
Product type 产品内容	Standard LCD Module TFT: 800*RGBx1280Dots 10.1”TFT LCD

客户确认Customer Approval	
项目负责人Project Manager	
品质主管Director of Quality	
采购工程师Purchasing Engineer	

1. Introduction

1.1 Scope of application

LCD specification: Dots 800xRGBx1280

As to basic specification of the driver IC, refer to the IC (JD9365DA-H3) specification and data book.

All material & processing of the LCD module should be Lead Free.

1.2 TFT features:

Structure: TFT PANNEL+IC +FPC+BL;

ALL Viewing Type LCD

800 dot-segment and 1280 dot-common outputs;

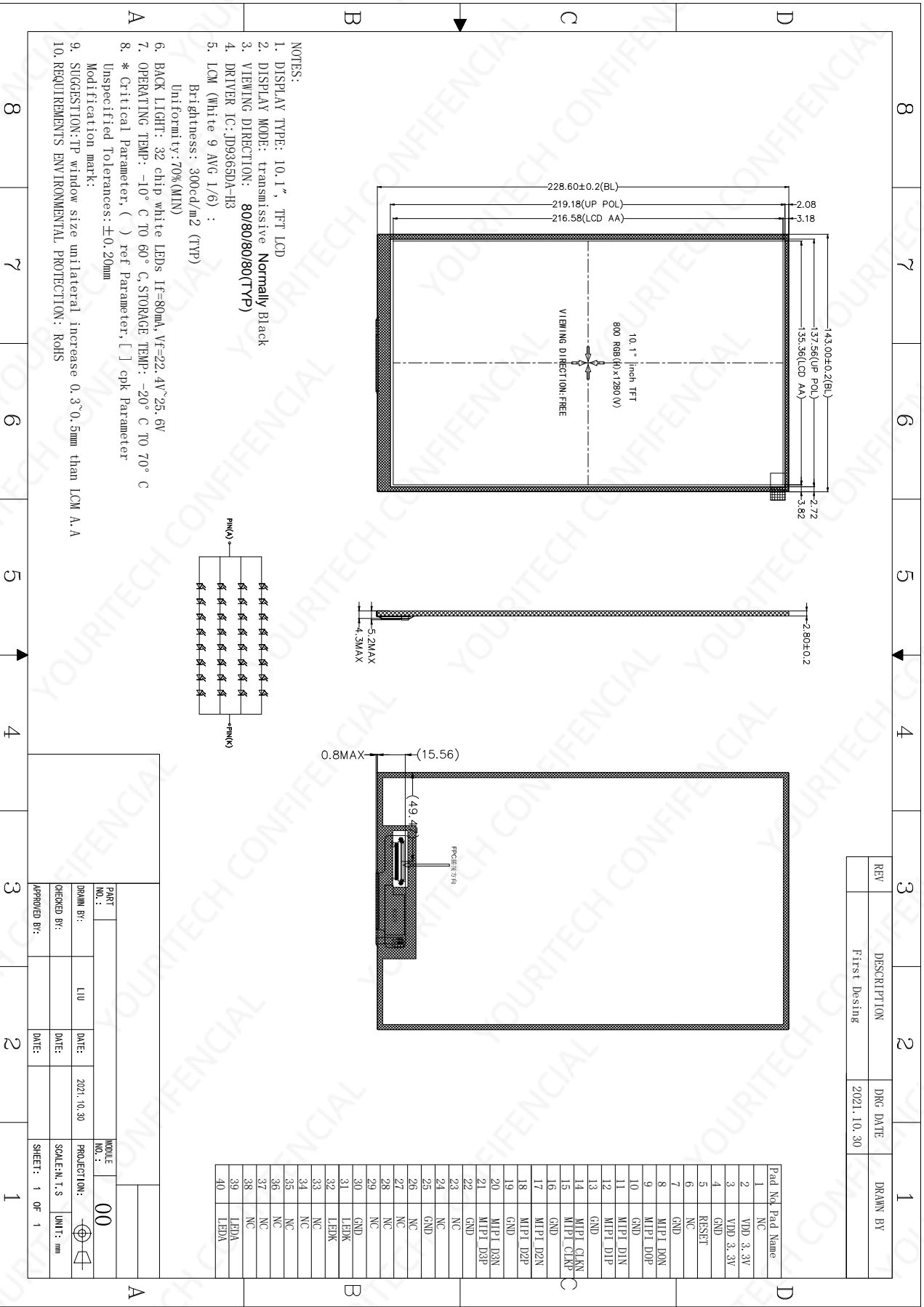
16.7M Color can be selected by software;

White LED back light;

4lane MIPI interface

2. LCM General specification

ITEM	Standard value	Unit
LCD Type	Normally Black	--
Drive element	TFT active matrix	--
Number of pixels	800*3RGB(H)X1280(V)	Dots
Pixel arrangement	RGB Vertical Stripe	--
Pixel Pitch (W*H)	0.1692(H)×0.1692(V)	mm
Active area	135.36(H)x216.576(V)	mm
Viewing direction	ALL O'CLOCK	-
TFT Driver IC	JD9365DA-H3	
TFT interface	4lane MIPI interface	-
Approx. Weight	TBD	g
LCM Size(W*H*T)	143(W) ×228.6(H) ×2.8(T)	mm
Touch structure	--	
Touch Driver IC	--	-
Touch Interface	--	



3.Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
LCM Operating Temperature	T _{OPR}	-10	+60	°C
LCM Storage Temperature	T _{STG}	-20	+70	°C
Humidity	RH	-	90	%

4.Electrical Characteristics

4.1 TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage for I/O	VDDIO	1.65	1.8	3.6	V
Supply Voltage for(DC/DC)	VDD	2.7	3.3	3.6	V
Current Consumption	I _{DD}	--	150	--	mA
	I _{DD-SLEEP}	--	40	80	uA

4.2 Back-Light Unit Characeristics

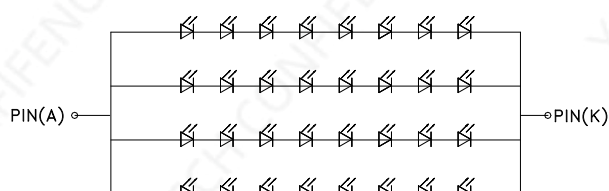
The back-light system is an edge-lighting type with 32 white LEDs. The characteristics of the back-light are shown in the following tables.

Characteristics	Symbol	Min.	Type	Max.	Unit	Notes
Forward Voltage	V _F	22.4		25.6	V	-
Forward current	I _F	--	80	-	mA	-
Luminance(With LCD)	L _v		300	--	cd/m ²	-
LED life time	N/A	----	30,000	--	Hr	Note 1

Note:

- (1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=20mA/LED. The LED life time could be decreased if operating I_L is larger than 25mA/LED.

Backlight circuit diagram shown in below:



5. Module Function Description

Pin No.	Symbol	LCM Functional	Notes
1	NC	NC	
2	VDD/3.3V	power supply for DC/DC circuit	
3	VDD/3.3V	power supply for DC/DC circuit	
4	GND	Power Ground	
5	RESET/3.3V	Reset pin. Setting either pin low initializes the LSI	
6	NC	NC	
7	GND	Power Ground	
8	MIPI_D0N	MIPI-DSI Data differential signal input pins	
9	MIPI_D0P	MIPI-DSI Data differential signal input pins	
10	GND	Power Ground	
11	MIPI_D1N	MIPI-DSI Data differential signal input pins	
12	MIPI_D1P	MIPI-DSI Data differential signal input pins	
13	GND	Power Ground	
14	MIPI_CLKN	MIPI-DSI CLOCK differential signal input pins	
15	MIPI_CLKP	MIPI-DSI CLOCK differential signal input pins	
16	GND	Power Ground	
17	MIPI_D2N	MIPI-DSI Data differential signal input pins	
18	MIPI_D2P	MIPI-DSI Data differential signal input pins	
19	GND	Power Ground	
20	MIPI_D3N	MIPI-DSI Data differential signal input pins	
21	MIPI_D3P	MIPI-DSI Data differential signal input pins	
22	GND	Power Ground	
23~24	NC	NC	
25	GND	Power Ground	
26~29	NC	NC	
30	GND	Power Ground	
31~32	LEDK	Power supply for backlight cathode input terminal.	
33~38	NC	NC	
39~40	LEDA	Power supply for backlight anode input terminal.	

6. Timing Characteristics

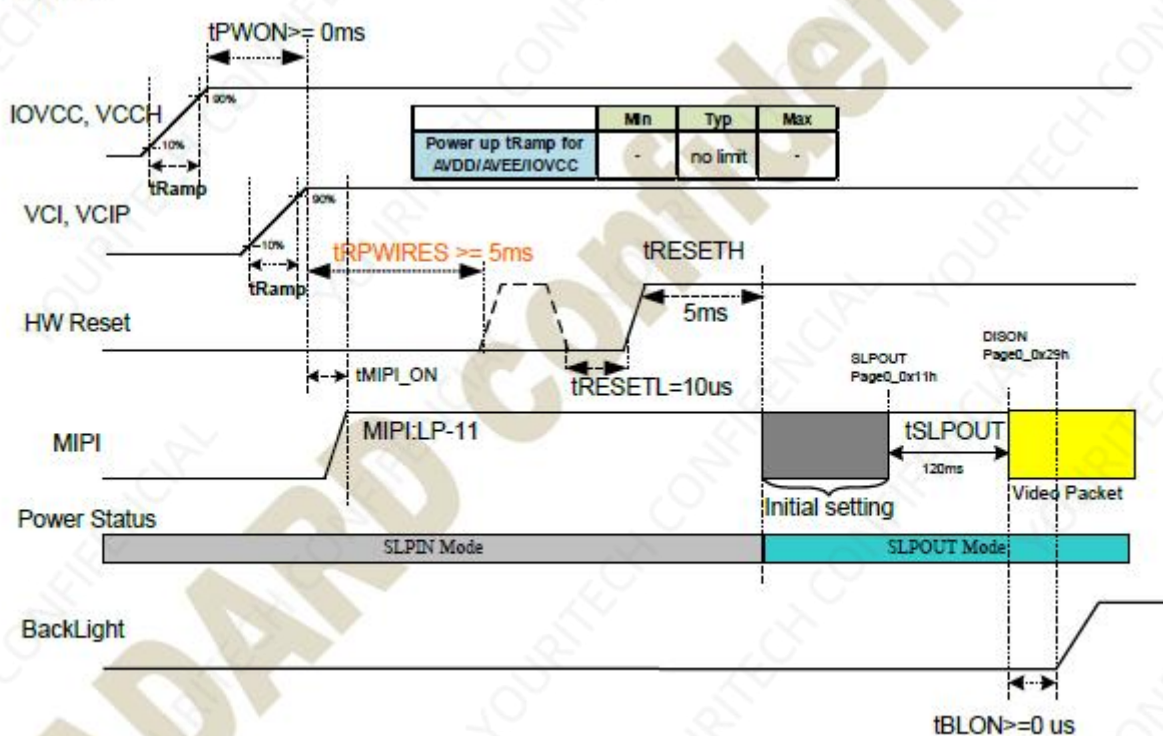
Power on sequence for differential power mode

Symbol	Min	Typ	Max	Unit	Remark
tRamp	-	no limit	-	us	
tPWON	0	-	-	ms	
tON1	0	-	-	ms	
tMIPI-ON	0	-	tRPWIRES	ms	
tRPWIRES	5	-	-	ms	
tRESETL	10	-	-	us	
tRESETH	5	-	-	ms	
tSLPOUT	120	-	-	ms	
tBLON	0	-	-	ms	

BOOSTM[1:0]=10 (Internal DC/DC power mode : Charge Pump, FP7721)

VCCD=IOVCC=VCCH=1.65V ~ 3.6V, VCI=VCIP=2.5V ~ 4.8V.

Power on:



Burst Mode Data Transmission

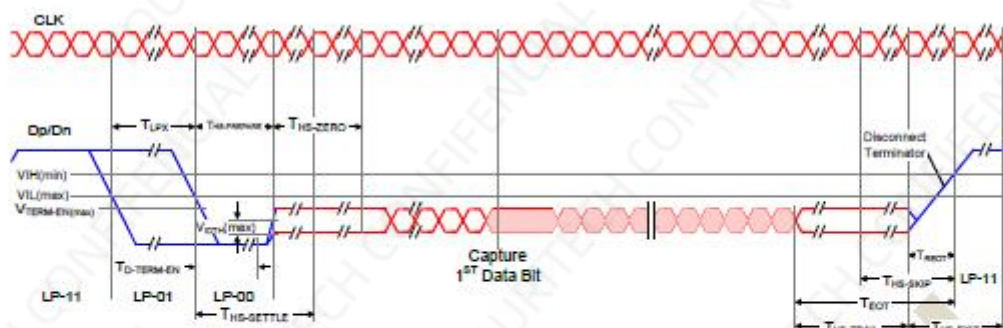


Figure 11.7: High-Speed Data Transmission in Bursts

Parameter	Description	Min	Typ	Max	UNIT
T_{LPX}	Transmitted length of any Low-Power state period	50	-	-	ns
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	$40 + 4 \cdot UI$	-	$85 + 6 \cdot UI$	ns
$T_{HS-PREPARE} + T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	$145 + 10 \cdot UI$	-	-	ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination.	-	-	$35 + 4 \cdot UI$	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions.	$85 + 6 \cdot UI$	-	$145 + 10 \cdot UI$	ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	$\max(n \cdot 8 \cdot UI, 60 + n \cdot 4 \cdot UI)$	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

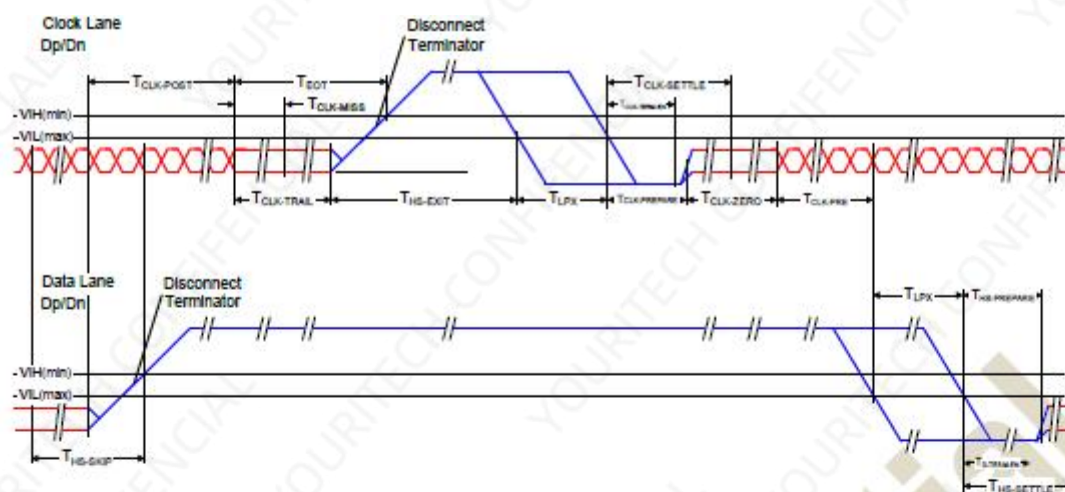


Figure 11.8: Switching the Clock Lane between Clock Transmission and Low-Power Mode

Parameter	Description	Min	Typ	Max	UNIT
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode.	$60 + 52 \cdot UI$	-	-	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	$8 \cdot UI$	-	-	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38	-	95	ns
$T_{CLK-PREPARE} + T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300	-	-	ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination.	-	-	38	ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

Reset input timings

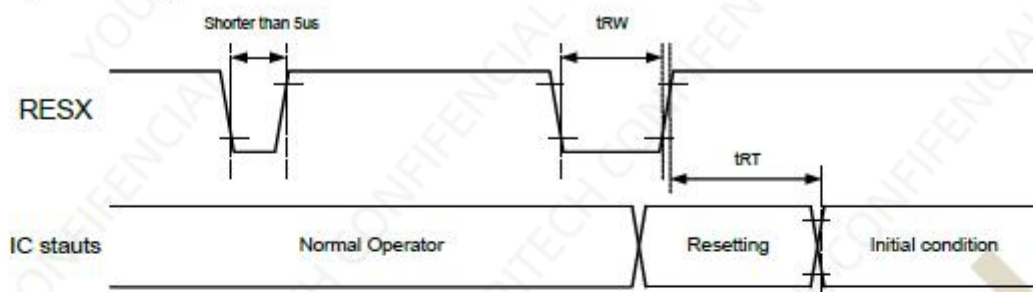


Figure 11.1: Reset input timings

Symbol	Parameter	Related pins	Min.	Max.	Unit
t_{RW}	Reset pulse width ⁽²⁾	RESX	10	-	μs
t_{RT}	Reset complete time ⁽³⁾	-	-	5 (Note 5)	ms
		-	-	120 (Note 6, 7)	ms

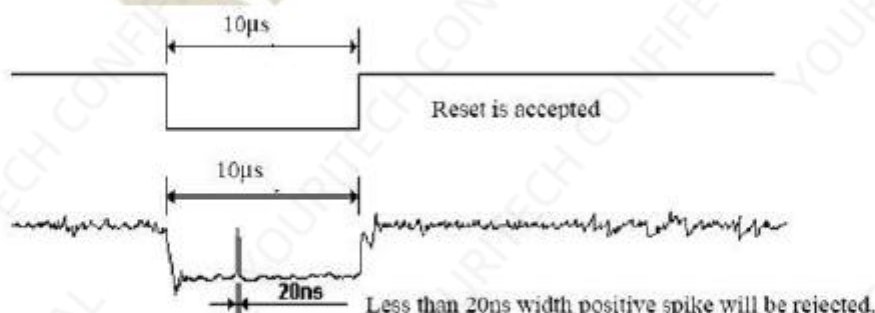
Note: (1) The reset complete time also required time for loading ID bytes from OTP to registers. This loading is done every time when there is HW reset cancel time (t_{RT}) within 5 ms after a rising edge of RESX.

(2) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5 μs	Reset Rejected
Longer than 10 μs	Reset
Between 5 μs and 10 μs	Reset Start

(3) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out -mode. The display remains the blank state in Sleep In -mode) and then returns to Default condition for H/W reset.

(4) Spike Rejection also applies during a valid reset pulse as shown below:



(5) When Reset is applied during Sleep In Mode.

(6) When Reset is applied during Sleep Out Mode.

(7) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

(8) After Sleep Out Command, it is necessary to wait 120msec then send RESX.

Table 11.3: Reset timings

7. Optical Characteristics

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle range	Horizontal	Θ_3	CR > 10	75	80	-	Deg.	Note 1
		Θ_9		75	80	-	Deg.	
	Vertical	Θ_{12}		75	80	-	Deg.	
		Θ_6		75	80	-	Deg.	
Color Gamut				52	56	-	%	@BLU
Luminance Contrast ratio		CR	$\Theta = 0^\circ$	800	1000			Note 2
Transmittance		T(%)	$\Theta = 0^\circ$		6.1		%	Base on BLU Note 3
White Chromaticity		x_w	$\Theta = 0^\circ$	0.257	0.287	0.317		Note 4 基于QE实测@BLU
		y_w		0.278	0.308	0.338		
Reproduction of color (BLU)	Red	x_R	$\Theta = 0^\circ$	0.583	0.613	0.643		
		y_R		0.333	0.363	0.393		
	Green	x_G		0.294	0.324	0.354		
		y_G		0.561	0.591	0.621		
	Blue	x_B		0.118	0.148	0.178		
		y_B		0.061	0.091	0.121		
Response Time (Rising + Falling)		T_{RT}	Ta= 25° C $\Theta = 0^\circ$	-	30		ms	Note 5

Notes : 1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see FIGURE 1).

2. Contrast measurements shall be made at viewing angle of $\Theta = 0$ and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (see FIGURE 1) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Transmittance is the Value with Polarizer
4. The color chromaticity coordinates specified in Table 5 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.
5. The electro-optical response time measurements shall be made as FIGURE 3 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is T_r , and 90% to 10% is T_d .

APPENDIX

Figure 1. The Definition of V_{th} & V_{sat}

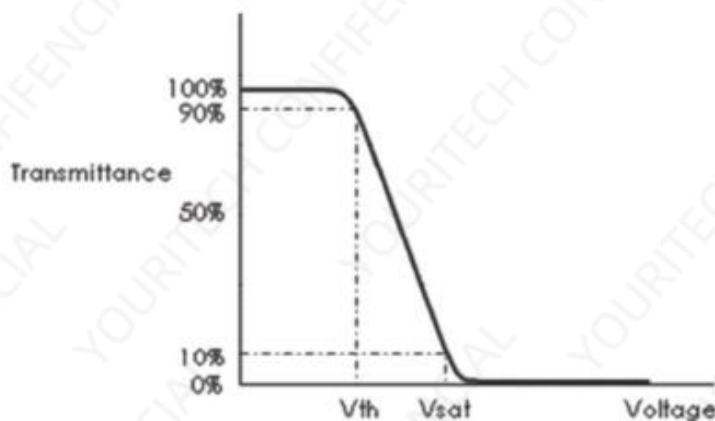


Figure 2. Measurement Set Up

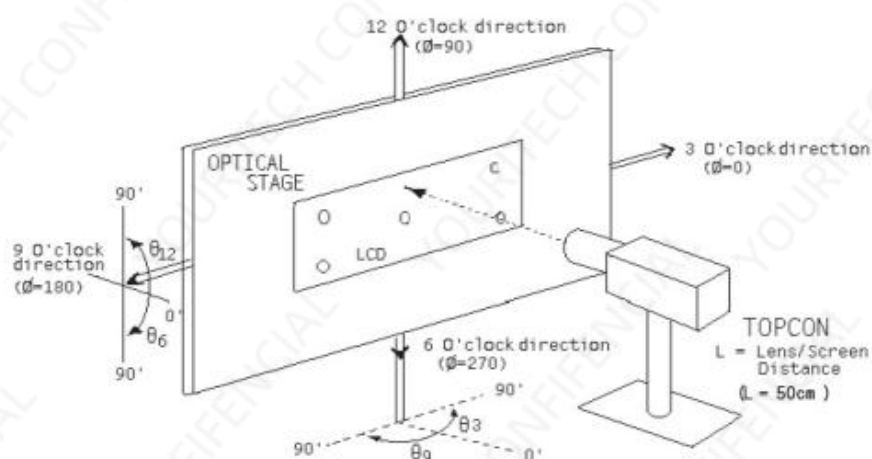
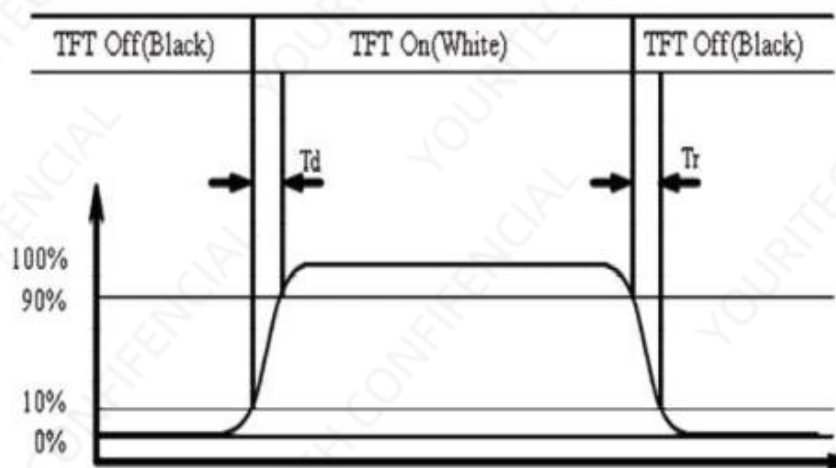


Figure 3. Response Time Testing



8. Reliability Test Item

No.	Test Item	Test Condition	Notes
1	High Temp. Storage	+70°C / 96H	1. Functional test is OK. Missing Segment, short, unclear segment non-display, display abnormally and liquid crystal leakage un-allowed. 2. No low temperature bubbles, end seal loose and fall, frame rainbow.
2	Low Temp. Storage	-20°C / 96H	
3	High Temp. Operating	+60°C / 96H	
4	Low Temp. Operating	-10°C / 96H	
5	High Temperature / Humidity storage	50°C x 90%RH / 96H	
6	Thermal and cold shock	Static state, -20°C (30min) ~60°C (30min), 50 cycles	

9. Packing Method----TBD

- END -