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Mechanical design



Product Specifications



Customer	Standard
Description	10.2" E-PAPER DISPLAY
Model Name	ET102EP02-J
Date	2024/01/31
Revision	1.0

	Design Engineering		
	Approval	Check	Design



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1. Over View

The display ET102EP02-J is a 10.2-inch TFT active matrix electrophoretic display, featuring a well-designed interface and reference system. It boasts a resolution of 640×960 pixels, offering 1-bit grayscale with full display capabilities in black, white, red and yellow. Each panel is equipped with an integrated circuit that includes a gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC converter, SRAM, look-up table (LUT), VCOM support, and border features.

2. Features

- ◆ 640×960pixels display
- ◆ High contrast High reflectance
- ◆ Ultra wide viewing angle Ultra low power consumption
- ◆ Pure reflective mode
- ◆ Bi-stable display
- ◆ Commercial temperature range
- ◆ Landscape portrait modes
- ◆ Hard-coat antiglare display surface
- ◆ Ultra Low current deep sleep mode
- ◆ On chip display RAM
- ◆ Waveform can stored in On-chip OTP or written by MCU
- ◆ Serial peripheral interface available
- ◆ On-chip oscillator
- ◆ On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- ◆ I²C signal master interface to read external temperature sensor
- ◆ Built-in temperature sensor



3. Mechanical and Optical Specification

Parameter	Specifications	Unit	Remark
Screen Size	10.2	Inch	
Display Resolution	960(H)×640(V)	Pixel	DPI:113
Active Area	215.52(H)×143.68(V)	mm	
Pixel Pitch	0.2245×0.2245	mm	
Pixel Configuration	Rectangle		
Outline Dimension	224(H)×157 (V) ×1.0±0.1 (D)	mm	
Weight	62.2±0.5	g	

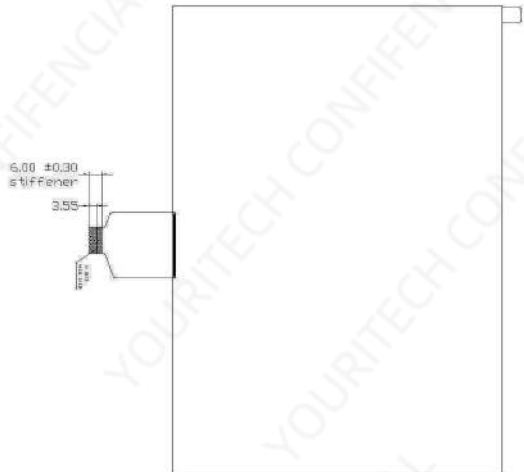
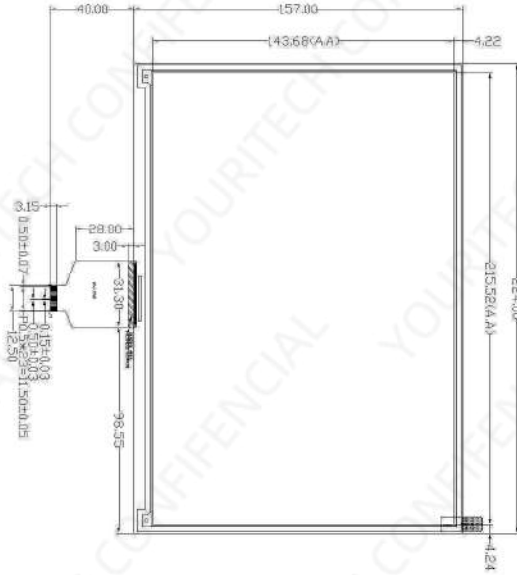


Confirmation:

FRONT VIEW

SIDE VIEW

BACK VIEW



NOTE

- 1 DISPLAY MODULE 10.2" ARRAY FOR EPD
- 2 DRIVER IC:SSD2677
- 3 RESOLUTION: 640gateX960source
- 4 PIXEL SIZE:0.2245mmX0.2245mm
- 5 FOR JX



TOLERANCES		TITLE		PROJECT		REV.		DATE		CUST. P/N	
UNMARKED		EPD		CHK.		APPR.		3RD ANGLE		PAGE	
ANGLES±5°		H GONG		JG CHEN		JH LU				1/1	
.X=±0.4mm											
.XX=±0.20mm											
.XXX=±0.20mm											



5.Input/output Pin Assignment

No.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	Keep Open
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC		Do not connect with other NC pins	Keep Open
5	VSH2	C	Positive Source driving voltage(Red)	
6	NC		Do not connect with other NC pins	
7	NC		Do not connect with other NC pins	
8	BS1	I	Bus Interface selection pin	Note 5-5
9	BUSY	O	Busy state output pin	Note 5-4
10	RES#	I	Reset signal input. Active Low.	Note 5-3
11	D/C#	I	Data /Command control pin	Note 5-2
12	CS#	I	Chip select input pin	Note 5-1
13	SCL	I	Serial Clock pin (SPI)	
14	SDA	I/O	Serial Data pin (SPI)	
15	VDDIO	P	Power Supply for interface logic pins It should be connected with VCI	
16	VCI	P	Power Supply for the chip	
17	VSS	P	Ground	
18	VDD	C	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS	
19	VPP	P	FOR TEST	Keep Open
20	VSH1	C	Positive Source driving voltage	
21	VGH	C	Power Supply pin for Positive Gate driving voltage and VSH1	
22	VSL	C	Negative Source driving voltage	
23	VGL	C	Power Supply pin for Negative Gate driving voltage VCOM and VSL	
24	VCOM	C	VCOM driving voltage	



I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/output), P = Power Pin, C = Capacitor Pin

Note 5-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.

Note 5-2: This pin is (D/C#) Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at SDA will be interpreted as data. When the pin is pulled LOW, the data at SDA will be interpreted as command.

Note 5-3: This pin (RES#) is reset signal input. The Reset is active low.

Note 5-4: This pin is Busy state output pin. When Busy is Low, the operation of chip should not be interrupted, command should not be sent. The chip would put Busy pin Low when -Outputting display waveform -Communicating with digital temperature sensor

Note 5-5: Bus interface selection pin

BS1 State	MCU Interface
L	4-lines serial peripheral interface(SPI) - 8 bits SPI
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

6. Electrical Characteristics

6.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	VCI	-0.5 to +4.0	V
Logic Input voltage	VIN	-0.5 to VCI +0.5	V
Logic Output voltage	VOUT	-0.5 to VCI +0.5	V
Operating Temp range	TOPR	0 to +40	°C.
Storage Temp range	TSTG	-25 to+70	°C.
Optimal Storage Temp	TST Go	23±2	°C.
Optimal Storage Humidity	HST Go	55±10	%RH

Note:

- Maximum ratings are those values beyond which damages to the device may occur.Functional operation should be restricted to the limits in the Panel DC Characteristics tables.
- The storage time is within 10 days for -25°C ~ 70°C.

The display screen should be kept white and face up.

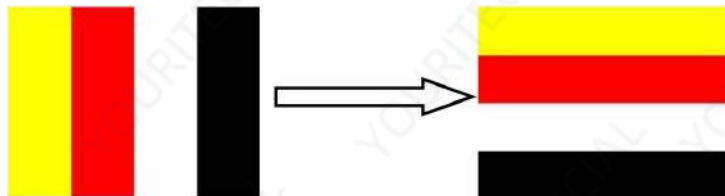


6.2 Panel DC Characteristics

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =23°C.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
Single ground	VSS	-		-	0	-	V
Logic supply voltage	Vci	-	VCI	2.3	3.0	3.6	V
Core logic voltage	VDD		VDD	2.3	3.0	3.6	V
High level input voltage	VIH	-	-	0.8 VCI	-	-	V
Low level input voltage	VIL	-	-	-	-	0.2 VCI	V
High level output voltage	VOH	IOH = -100uA	-	0.8 VCI	-	-	V
Low level output voltage	VOL	IOL = 100uA	-	-	-	0.2 VCI	V
Typical power	PTYP	Vci =3.0V	-	-	66		mW
Deep sleep mode	PSTPY	Vci =3.0V	-	-	0.0012		mW
Typical operating current	Iopr VC _r	Vci =3.0V	-	-	22		mA
Image update time	-	23 °C	-	-	20		sec
Deep sleep mode current	Idslp Vc _r	DC/DC off No clock No input load Ram data not retain	-	-	0.4	-	uA

Notes: 1. The typical power is measured with following transition from horizontal 4 scale pattern to vertical 4 scale pattern.



2. The deep sleep power is the consumed power when the panel controller is in deep sleep mode.
3. The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by YOURITECH.
4. Electrical measurement: Tektronix oscilloscope - MDO3024,
Tektronix current probe - TCP0030A.



6.3 Panel AC Characteristics

6.3.1 MCU Interface Selection

The pin assignment at different interface mode is summarized in Table 6-3-1. Different MCU mode can be set by hardware selection on BS1 pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

Pin Name	Data/Command Interface		Control Signal		
Bus interface	SDA	SCL	CS#	D/C#	RES#
BS1=L 4-wire SPI	SDA	SCL	CS#	D/C#	RES#
BS1=H 3-wire SPI	SDA	SCL	CS#	L	RES#

Table 6-3-1: MCU interface assignment under different bus interface mode

6.3.2 MCU Serial Interface (4-wire SPI)

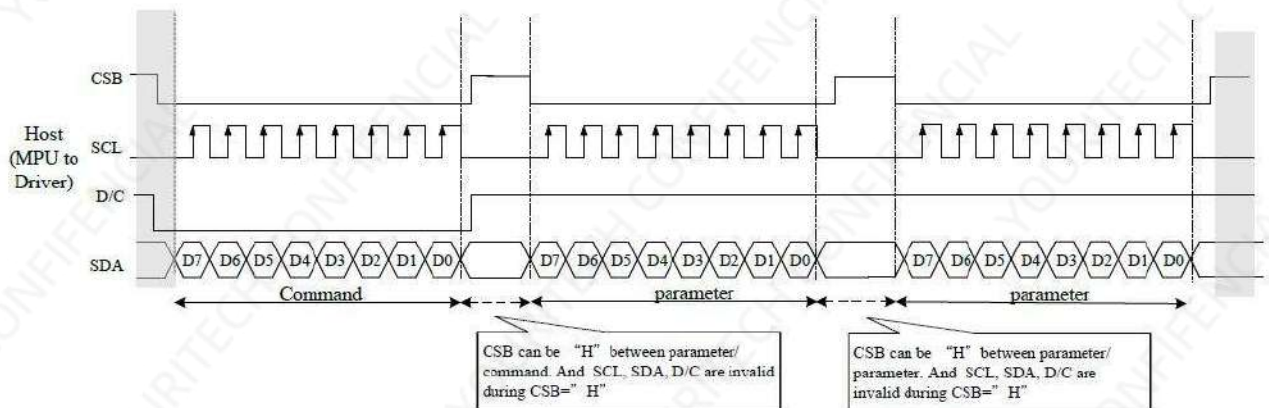
The serial interface consists of serial clock SCL, serial data SDA, D/C#, CS#. This interface supports Write mode and Read mode.

Function	CS#	D/C#	SCL
Write command	L	L	↑
Write data	L	H	↑

Table 6-3-2: Control pins of 4-wire Serial Peripheral interface

Note: ↑ stands for rising edge of signal

Figure 6-3-1: 4-wire SPI mode



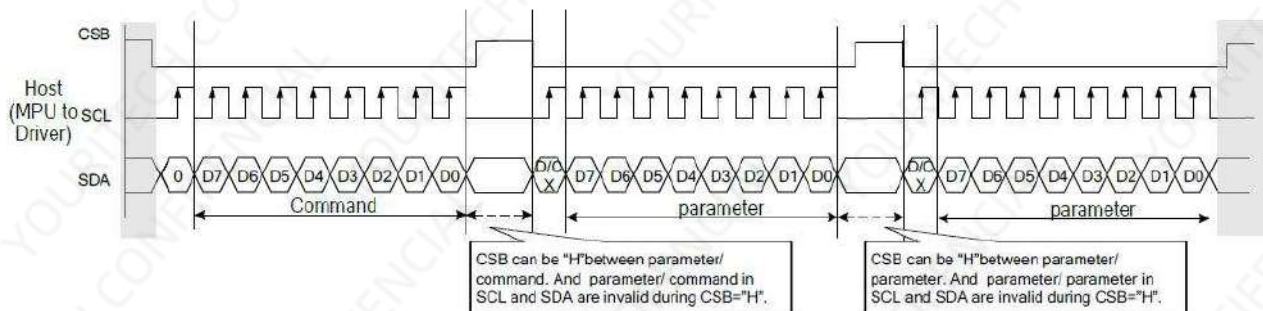
6.3.3 MCU Serial Interface (3-wire SPI)

Function	CS#	D/C#	SCL
Write command	L	Tie	↑
Write data	L	Tie	↑

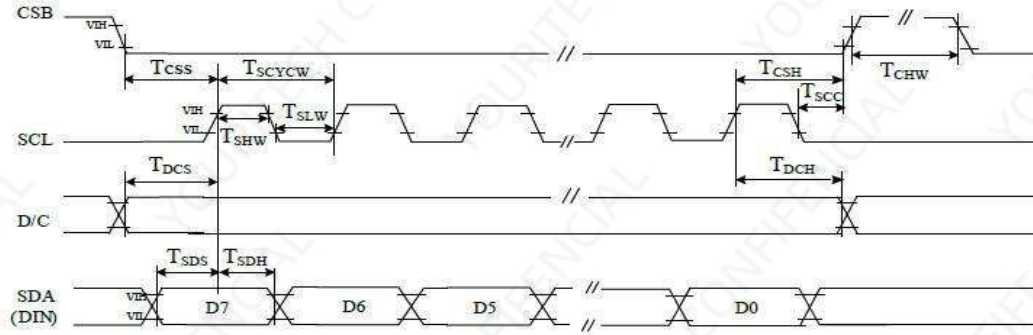
Table 6-3-3: Control pins of 4-wire Serial Peripheral interface

Note: ↑ stands for rising edge of signal

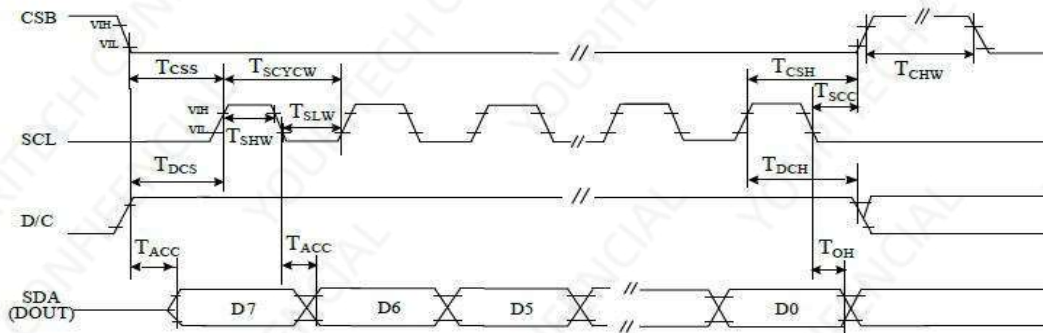
Figure 6-3-2: 3-wire SPI mode



6.3.4 Interface Timing



4 pin serial interface characteristics(write mode)



Serial Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
tcss	CSB select setup time	TBD			ns
tscch	CSB select hold time	TBD			ns
tsccl	CSB deselect setup time	TBD			ns
tchwh	CSB deselect hold time	TBD			ns
tscycw	Serial clock cycle (Write)	TBD			ns
tshw	SCL "H" pulse width (Write)	TBD			ns
tslw	SCL "L" pulse width (Write)	TBD			ns
tscycl	Serial clock cycle (Read)	TBD			ns
tshr	SCL "H" pulse width (Read)	TBD			ns
tslr	SCL "L" pulse width (Read)	TBD			ns
tsds	Data setup time	TBD			ns
tsdh	Data hold time	TBD			ns
tacc	Access time			TBD	ns
toh	Output disable time	TBD			ns



7.Command Table

R/W#	DC	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	00	0	0	0	0	0	0	0	0	PSR	Panel Setting Register A[7:0] = 0Fh [POR] B[7:0] = 09h [POR]
0	1		A7	A6	A5	0	A3	A2	A1	A0		A[7:6] ~ RES[1:0] Display Resolution setting (source x gate) 00b: 960 x 680 (Default) 01b: 960 x 672 10b: 960 x 640 11b: 880 x 528 A[3] ~ UD Gate Scan Direction: 0: Scan down. First line to Last line: Gn-1 ... G0 1: Scan up. (Default) First line to Last line: G0 ... Gn-1 A[2] ~ SHL Source Shift Direction: 0: Shift left. First data to Last data: Sn-1 ... S0 1: Shift right. (Default) First data to Last data: S0 ... Sn-1 A[1] ~ SHD_N Booster and Regulator Switch: 0: PON / POF command will not execute 1: PON / POF command will execute (Default) A[0] ~ RST_N Soft Reset: 0: The controller is reset. Reset all registers to their default value. Driver all function will be disabled. 1: Normal operation (Default). BUSY_N signal will become "0" until Soft reset is finished.



0	0	01	0	0	0	0	0	0	0	1	PWR	Power setting Register A[5:0] = 07h [POR] B[7:0] = F0h [POR]									
0	1		0	0	0	0	0	A ₂	A ₁	A ₀		A[2:0] = 111 [POR]									
0	1		1	1	1	1	0	0	B ₁	B ₀		B[1:0] ~ VGPN [1:0] Internal VGH / VGL Voltage Level Selection:									
												<table><tr><th>VGPN [1:0]</th><th>Gate Voltage Level</th></tr><tr><td>00</td><td>VGH=20V,VGL=-20V (Default) VSH=15V, VSL=-15V</td></tr><tr><td>01</td><td>VGH=17V ,VGL=-17V VSH=15V, VSL=-15V</td></tr><tr><td>10</td><td>VGH=15V,VGL=-15V VSH=15V, VSL=-15V</td></tr><tr><td>11</td><td>Reserved.</td></tr></table>	VGPN [1:0]	Gate Voltage Level	00	VGH=20V,VGL=-20V (Default) VSH=15V, VSL=-15V	01	VGH=17V ,VGL=-17V VSH=15V, VSL=-15V	10	VGH=15V,VGL=-15V VSH=15V, VSL=-15V	11
VGPN [1:0]	Gate Voltage Level																				
00	VGH=20V,VGL=-20V (Default) VSH=15V, VSL=-15V																				
01	VGH=17V ,VGL=-17V VSH=15V, VSL=-15V																				
10	VGH=15V,VGL=-15V VSH=15V, VSL=-15V																				
11	Reserved.																				

R/W#	DC	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	02	0	0	0	0	0	0	1	0	POF	Power OFF Command Register
0	1		0	0	0	0	0	0	0	0		After power off command, driver will power off based on the Power OFF Sequence, then BUSY_N signal will become "0". The Power OFF command will turn off DCDC, source driver, gate driver, VCOM driver, temperature sensor, but register and SRAM data will keep until VDD off. SD output will base on previous condition. *Remark: POF works at PON only
0	0	04	0	0	0	0	0	1	0	0	PON	Power ON Command Register
												After the Power ON command, driver will power on based on the Power ON Sequence. After power on command and all power sequence are ready, then BUSY_N signal will become "1". * Remark: PON Include booster on, VSHx/VSLx regulator on With default BTST, timing is >80ms





0	0	40	0	1	0	0	0	0	0	0	TSC	Temperature Sensor Command Register																						
1	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		This command enables internal temperature sensor. BUSY_N will go low during temperature sensor is under operation. Then the temperature value can be read in 1degC step A[7:0] ~ TS [7:0]																						
												<table><tr><th>TS [7:0]</th><th>Return Value(degC)</th></tr><tr><td>E7h</td><td>-25</td></tr><tr><td>...</td><td>...</td></tr><tr><td>FFh</td><td>-1</td></tr><tr><td>00h</td><td>0</td></tr><tr><td>01h</td><td>1</td></tr><tr><td>...</td><td>...</td></tr><tr><td>19h</td><td>25</td></tr><tr><td>...</td><td>...</td></tr><tr><td>31h</td><td>49</td></tr><tr><td>32h</td><td>50</td></tr></table>	TS [7:0]	Return Value(degC)	E7h	-25	...	...	FFh	-1	00h	0	01h	1	...	...	19h	25	...	...	31h	49	32h	50
TS [7:0]	Return Value(degC)																																	
E7h	-25																																	
...	...																																	
FFh	-1																																	
00h	0																																	
01h	1																																	
...	...																																	
19h	25																																	
...	...																																	
31h	49																																	
32h	50																																	

R/W#	DC	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description														
0	0	50	0	1	0	1	0	0	0	0	CDI	A[7:0] = 97h [POR]														
0	1		A ₇	A ₆	A ₅	0	0	0	0	0		A[7:5]~VBD [2:0] Border Output Selection: <table><tr><td></td><td>DDX=1</td></tr><tr><td>VBD[2:0]</td><td>LUT (Default)</td></tr><tr><td>000</td><td>Gray 0</td></tr><tr><td>001</td><td>Gray 1</td></tr><tr><td>010</td><td>Gray 2</td></tr><tr><td>011</td><td>Gray 3</td></tr><tr><td>100</td><td>HIZ(Default)</td></tr></table>		DDX=1	VBD[2:0]	LUT (Default)	000	Gray 0	001	Gray 1	010	Gray 2	011	Gray 3	100	HIZ(Default)
	DDX=1																									
VBD[2:0]	LUT (Default)																									
000	Gray 0																									
001	Gray 1																									
010	Gray 2																									
011	Gray 3																									
100	HIZ(Default)																									
0	0	61	0	1	1	0	0	0	0	1	TRES	Resolution setting Register This command defines alternative resolution														
0	1		0	0	0	0	0	0	A ₉	A ₈		A[7:0] ~ HRES[9:0] Horizontal Display Resolution														
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		Remark: Horizontal resolution should be 4-multiple.														
0	1		0	0	0	0	0	0	B ₉	B ₈		B[8:0] ~ VRES[9:0] Vertical Display Resolution														
0	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		e.g. HRES= 3C0h, VRES= 2A8h														
												<table><tr><td>UD,SHL</td><td>Source and gate sequence</td></tr><tr><td>00</td><td>S679,G959 to S0,G0</td></tr><tr><td>01</td><td>S0, G959 to S679,G0</td></tr><tr><td>10</td><td>S679,G0 to S0, G959</td></tr><tr><td>11</td><td>S0,G0 to S679, G295</td></tr></table>	UD,SHL	Source and gate sequence	00	S679,G959 to S0,G0	01	S0, G959 to S679,G0	10	S679,G0 to S0, G959	11	S0,G0 to S679, G295				
UD,SHL	Source and gate sequence																									
00	S679,G959 to S0,G0																									
01	S0, G959 to S679,G0																									
10	S679,G0 to S0, G959																									
11	S0,G0 to S679, G295																									
												Remark: 1) Both PSR.RES & TRES command can set panel resolution. Priority will be given to the last received PSR or TRES command. 2) VRES[8:0] >= 120														
0	0	70	0	1	1	1	0	0	0	0	REV	Chip Revision Register														
1	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		The command is to read the ID A[7:0] = 07h [POR]														



R/W#	DC	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description										
0	0	07	0	0	0	0	0	1	1	1	DSLTP	Deep Sleep Register This command makes the chip enter the deep-sleep mode. The deep sleep mode could return to stand-by mode by hardware reset assertion. The only one parameter is a check code, the command would be executed if check code is A5h.										
0	1		1	0	1	0	0	1	0	1												
0	0	17	0	0	0	1	0	1	1	1	AUTO	Auto Sequence Register This command makes the chip enter the auto sequence Single-chip application ONLY. Auto Sequence Option 0xA5: Start Auto Sequence (PON > DRF > POF) 0xA7: Start Auto Sequence (PON > DRF > POF > DSLTP). Others: No effect BUSY_N signal will become "0" until Auto Sequence is finished.										
0	1		A7	A6	A5	A4	A3	A2	A1	A0												
0	0	10	0	0	0	1	0	0	0	0	DTM	Data Start transmission Register This command indicates that user starts to transmit data. Then write to SRAM. While complete data transmission, user must send a Data Refresh command (R12H). Then the chip will start to send data/VCOM for panel.										
2 bit per pixel																						
0	1		KPixel1 [1:0]		KPixel2 [1:0]		KPixel3 [1:0]		KPixel4 [1:0]													
:																						
0	1		KPixel (4M-3) [1:0]		KPixel (4M-2) [1:0]		KPixel (4M-1) [1:0]		KPixel (4M) [1:0]													
												KPixel[1:0] Source Driver Output <table><tr><td></td><td>DDX=1 (Default)</td></tr><tr><td>00b</td><td>Gray 0</td></tr><tr><td>01b</td><td>Gray 1</td></tr><tr><td>10b</td><td>Gray 2</td></tr><tr><td>11b</td><td>Gray 3</td></tr></table> After issue this command, the host must send at least 1 byte data to the device.		DDX=1 (Default)	00b	Gray 0	01b	Gray 1	10b	Gray 2	11b	Gray 3
	DDX=1 (Default)																					
00b	Gray 0																					
01b	Gray 1																					
10b	Gray 2																					
11b	Gray 3																					
0	0	12	0	0	0	1	0	0	1	0	DRF	Display Refresh Command Register After this command is issued, driver will refresh display (data/VCOM) according to SRAM data and LUT. LUT can define DCVCOM/ACVCOM. After Display Refresh command, BUSY_N signal will become "0" until display update is finished.										
0	1		0	0	0	0	0	0	0	0												



R/W#	DC	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																	
0	0	80	1	0	0	0	0	0	0	0	AMV	Auto Measurement VCOM Register This command implements related VCOM sensing setting. A[7:0] = 00h [POR]																	
0	1		A ₇	A ₆	A ₅	A ₄	0	0	0	A ₀		A[7:6] ~ P[1:0] Number of sensing Points 00: 2 (Default) 01: 4 10: 8 11: 16 A[5:4] ~AMVT[1:0] Auto Measure Vcom Time: Sensing Time 00: 5 sec. (Default) 01: 10 sec. 10: 15 sec. 11: 20 sec. A[0] ~ AMVE Auto Measure Vcom Enable (/Disable): 0: Disabled (Default) 1: Enabled Requirement: 1) AMV works at PON only 2) BUSY_N signal will become "0" until Vcom sensing is finished.																	
0	0	81	1	0	0	0	0	0	0	1	VV	Auto Measurement VCOM Register This command gets the Vcom value after AMV.																	
1	1		1	0	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		A[5:0] ~ VV[5:0]: Vcom read Value , valid range from -0.2V to -4.0V. <table><tr><td>VV[5:0]</td><td>Vcom read value</td></tr><tr><td>00h</td><td>Reserved</td></tr><tr><td>04h</td><td>-0.2V</td></tr><tr><td>08h</td><td>-0.4V</td></tr><tr><td>0Ch</td><td>-0.6V</td></tr><tr><td>10h</td><td>-0.8V</td></tr><tr><td>...</td><td>...</td></tr><tr><td>50h</td><td>-4.0V</td></tr><tr><td>others</td><td>Reserved</td></tr></table>	VV[5:0]	Vcom read value	00h	Reserved	04h	-0.2V	08h	-0.4V	0Ch	-0.6V	10h	-0.8V	...	...	50h	-4.0V	others
VV[5:0]	Vcom read value																												
00h	Reserved																												
04h	-0.2V																												
08h	-0.4V																												
0Ch	-0.6V																												
10h	-0.8V																												
...	...																												
50h	-4.0V																												
others	Reserved																												

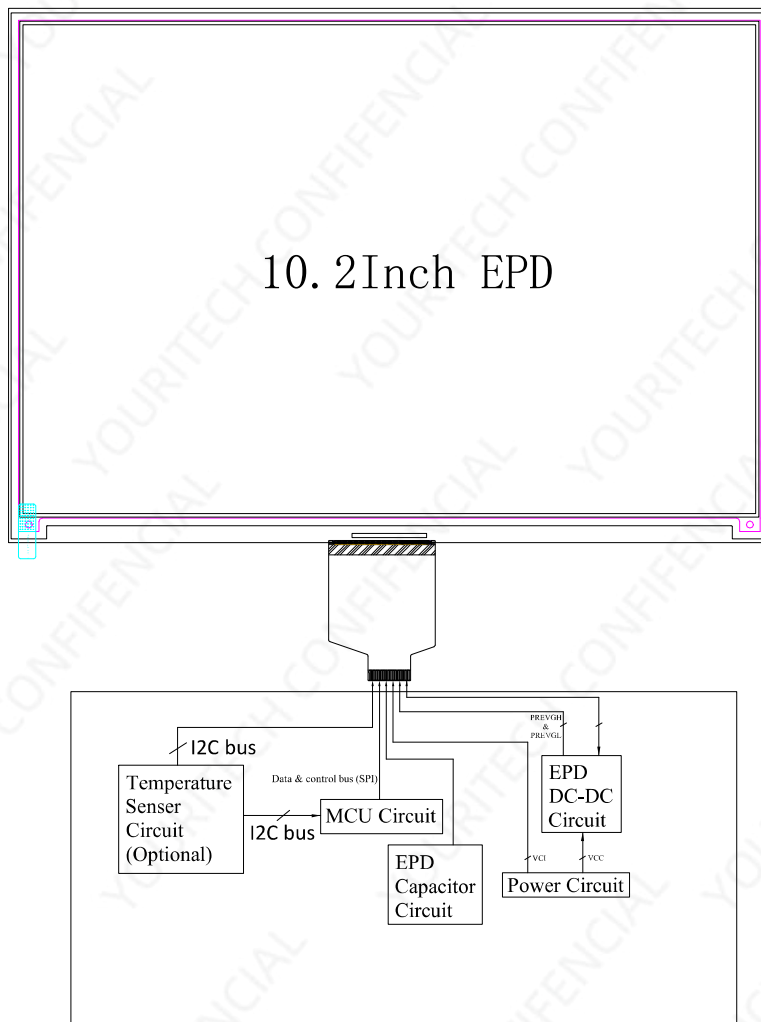


0	0	82	1	0	0	0	0	0	1	0	VDCS	VCM_DC Setting Register This command sets VCOM_DC value. A[7:0] = 00h [POR]																		
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	0	0		A[7] ~ OTP_VCM Vcom follow VDCS after RESET. 0: Disable (Default), auto load from OTP if it is valid. 1: Enable, VCOM value from the VDCS[6:0] A[6:0] ~ VDCS[6:0]: VCOM_DC Setting, 0.2V step from -0.2V to -4.0V. <table><tr><th>VDCS [6:0]</th><th>VCOM_DC Setting</th></tr><tr><td>00h</td><td>Reserved</td></tr><tr><td>04h</td><td>-0.2V</td></tr><tr><td>08h</td><td>-0.4V</td></tr><tr><td>0Ch</td><td>-0.6V</td></tr><tr><td>10h</td><td>-0.8V</td></tr><tr><td>...</td><td>...</td></tr><tr><td>50h</td><td>-4.0V</td></tr><tr><td>others</td><td>Reserved</td></tr></table>	VDCS [6:0]	VCOM_DC Setting	00h	Reserved	04h	-0.2V	08h	-0.4V	0Ch	-0.6V	10h	-0.8V	...	...	50h	-4.0V	others	Reserved
VDCS [6:0]	VCOM_DC Setting																													
00h	Reserved																													
04h	-0.2V																													
08h	-0.4V																													
0Ch	-0.6V																													
10h	-0.8V																													
...	...																													
50h	-4.0V																													
others	Reserved																													

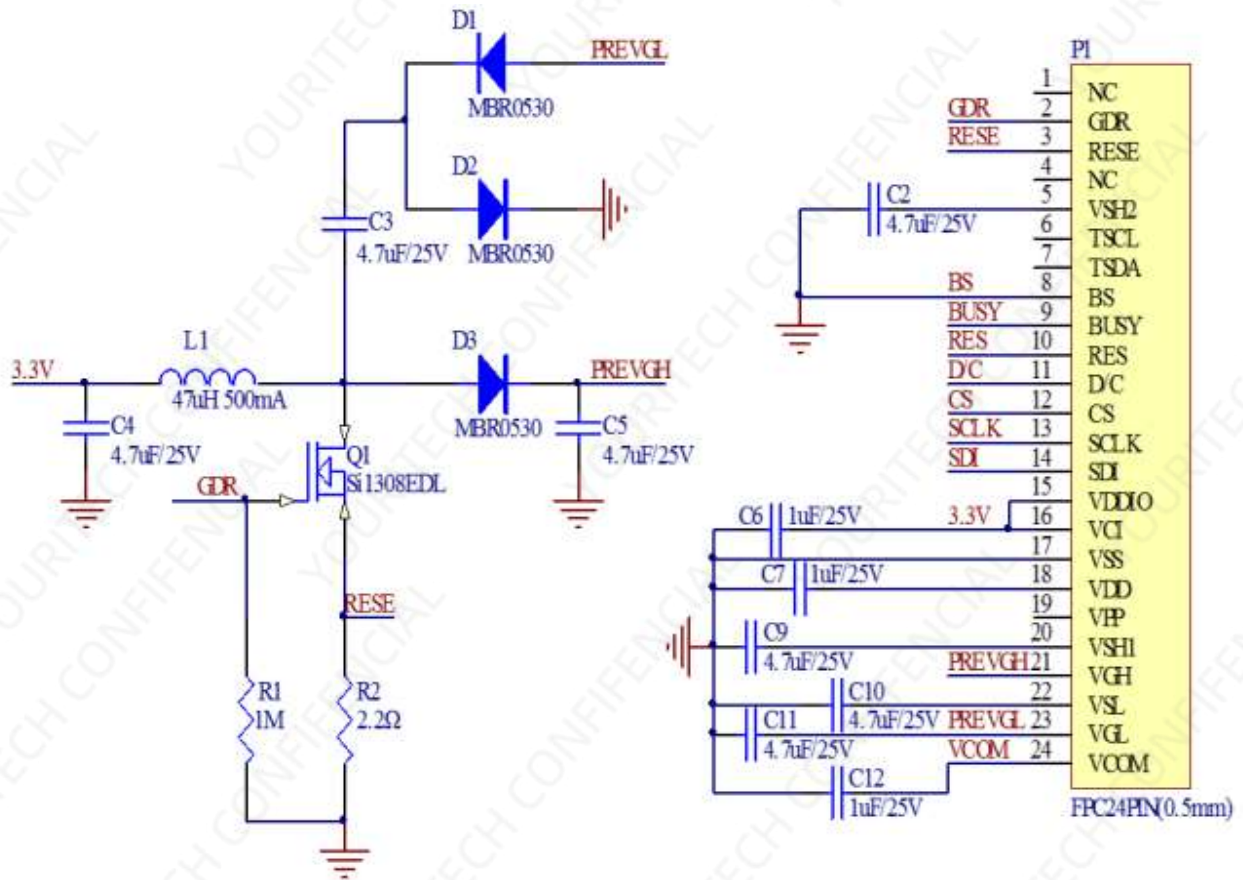
R/W#	DC	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	90	1	0	0	1	0	0	0	0	PGM	Program Mode This command is to set OTP program mode After this command is issued, the chip would enter the program mode. After the programming procedure completed, a hardware reset is necessary for leave the program mode BUSY_N signal will become 0 until PGM mode is ready.
0	0	91	1	0	0	1	0	0	0	1	APG	Active Program This command is to execute OTP program After this command is issued, the chip would program the OTP. BUSY_N signal will become 0 until the programming is completed. Requirement: In PON mode with internal programming power.
0	0	92	1	0	0	1	0	0	1	0	ROTP	Read OTP Data This command is to read the OTP content from SRAM. The 1 st byte read is dummy byte. The 2 nd byte read is the content of Address 0 in OTP The N+1 th byte read is the content of Address n in OTP After issue this command, the host must read at least 1 byte data from the device.
1	1											
0	0	E3	1	1	1	0	0	0	1	1	PWS	Power Saving Register This command is sets for saving power VCOM/Source power saving during display refresh period. A[7:0] = 65h [POR]
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		



8. Block Diagram

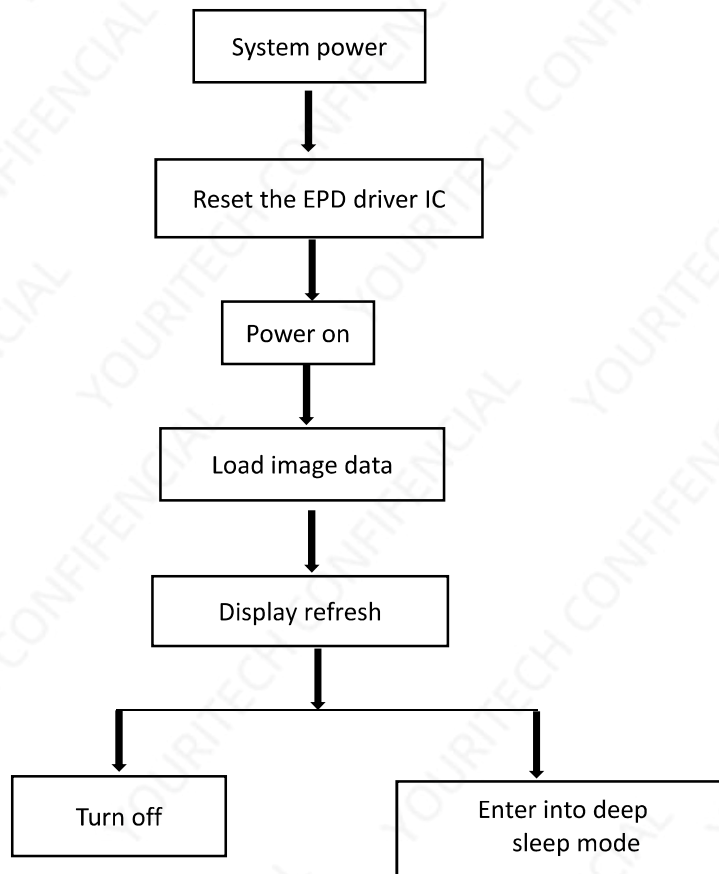


9. Typical Application Circuit with SPI Interface

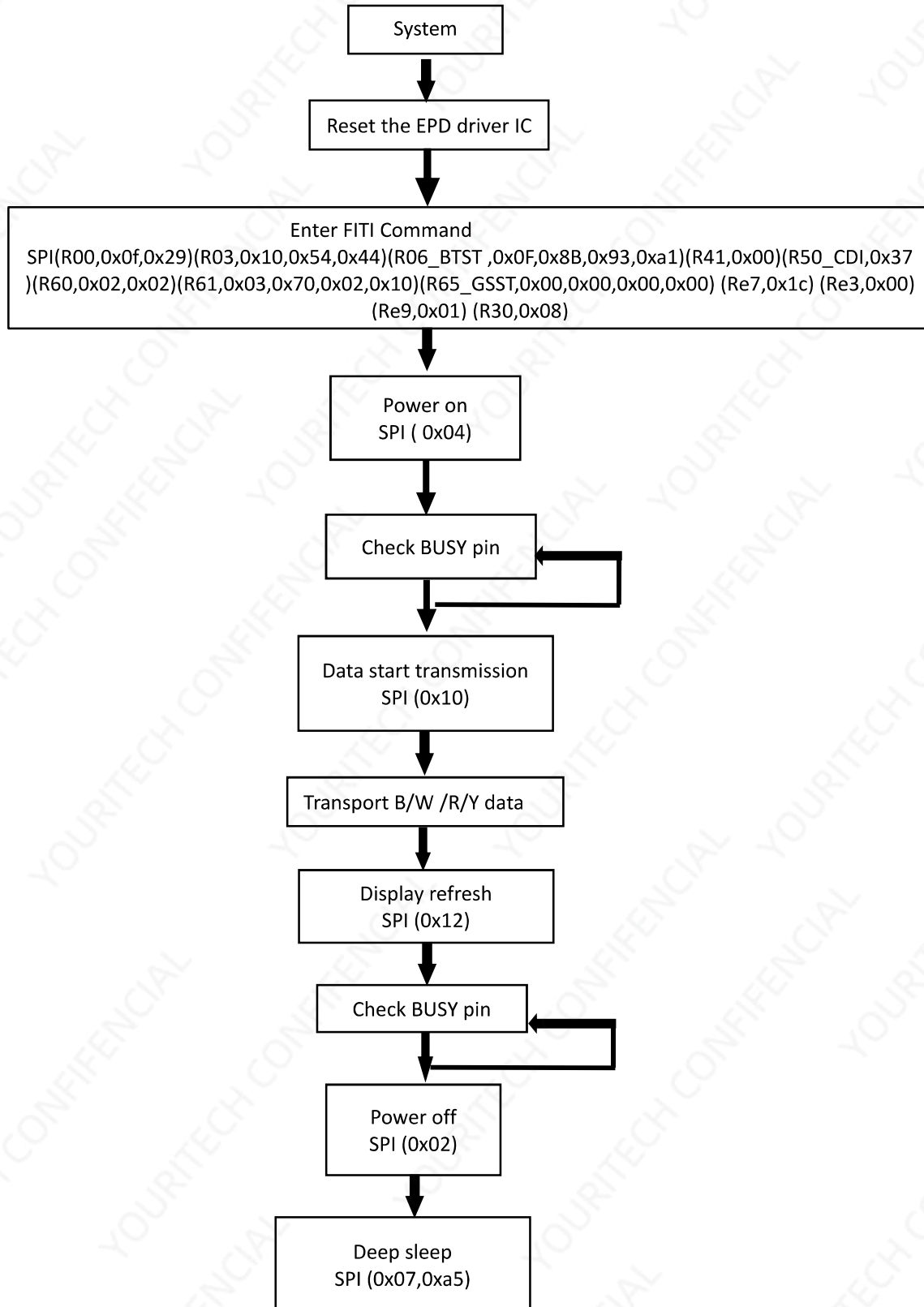


10. Typical Operating Sequence

10.1 LUT from OTP Operation Flow



10.2 OTP Operation Reference Program Code



11. Reliability Test

NO	Test items	Test condition
1	Low-Temperature Storage	T = -25°C, 500 h Test in white pattern
2	High-Temperature Storage	T=60°C, RH=35%, 500h Test in white pattern
3	High-Temperature Operation	T=50°C, RH=30%, 500h
4	Low-Temperature Operation	0°C, 500h
5	High-Temperature, High-Humidity Operation	T=40°C, RH=90%, 500h
6	High-Temperature, High-Humidity Storage	T=60°C, RH=80%, 500h Test in white pattern
7	Temperature Cycle	1 cycle:[-25°C 30min]→[+60 °C 30 min] : 100 cycles Test in white pattern

- Note:**
1. Stay white pattern for storage and non-operation test.
 2. Operation is black→white→red→yellow pattern, the interval is 150s.
 3. Put in 20°C--25°C for 1hour after test finished, The function ,appearance and display performance is OK.



12. Quality Assurance

12.1 Environment

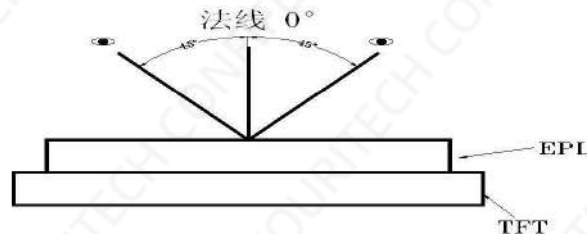
Temperature: 18~28℃

Humidity: 40%~70%RH

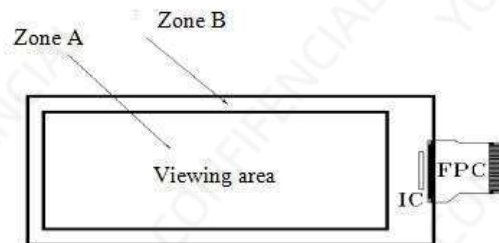
12.2 Illuminance

Brightness: 800 ~ 1500LUX; Angle: Relate $45 \pm 5^\circ$ surround; Function check when 150 ~ 200 LUX visual distance module surface 30CM

12.3 Inspect method



12.4 Display area



12.5 Ghosting test method

Four-color ghosting is measured with following transition from horizontal 4 scale pattern to vertical 4 scale pattern. The listed optical characteristics are only guaranteed under the controller & waveform provided by YOURITECH



1) Measurement Instruments: X-rite i1Pro

2) Ghosting formula:

W ghosting: $\Delta E = \text{Max} (\Delta E_{ab}(Y-W, R-W), \Delta E_{ab}(Y-W, W-W), \Delta E_{ab}(Y-W, B-W), \Delta E_{ab}(R-W, W-W), \Delta E_{ab}(R-W, B-W), \Delta E_{ab}(W-W, B-W))$

K ghosting: $\Delta E = \text{Max} (\Delta E_{ab}(Y-B, R-B), \Delta E_{ab}(Y-B, W-B), \Delta E_{ab}(Y-B, B-B), \Delta E_{ab}(R-B, W-B), \Delta E_{ab}(R-B, B-B), \Delta E_{ab}(W-B, B-B))$

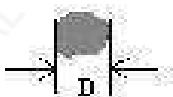
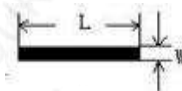
R ghosting: $\Delta E = \text{Max} (\Delta E_{ab}(Y-R, R-R), \Delta E_{ab}(Y-R, W-R), \Delta E_{ab}(Y-R, B-R), \Delta E_{ab}(R-R, W-R), \Delta E_{ab}(R-R, B-R), \Delta E_{ab}(W-R, B-R))$

Y ghosting: $\Delta E = \text{Max} (\Delta E_{ab}(Y-Y, R-Y), \Delta E_{ab}(Y-Y, W-Y), \Delta E_{ab}(Y-Y, B-Y), \Delta E_{ab}(R-Y, W-Y), \Delta E_{ab}(R-Y, B-Y), \Delta E_{ab}(W-Y, B-Y))$



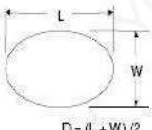
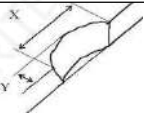
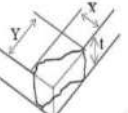
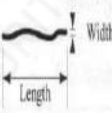
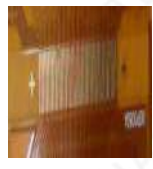
12.6 Inspection standard

12.6.1 Electric inspection standard

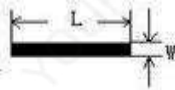
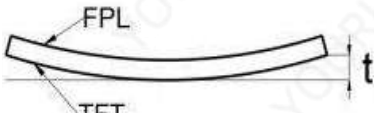
NO.	Item	Standard	Defect level	Method	Scope
1	Display	Clear display Display complete Display uniform	MA	Visual inspection	Zone A
2	Black/White spots	 $D \leq 0.3\text{mm}$, negligible $0.3\text{mm} < D \leq 0.5\text{mm}$, $N \leq 5$, Allowed $0.5\text{mm} < D$ Not Allow	MI		
3	Black/White lines (No switch)	 $L \leq 1.0\text{mm}, W \leq 0.15\text{mm}$ negligible $1.0\text{mm} < L \leq 4.0\text{mm}$ $0.15\text{mm} < W \leq 0.5\text{mm}$ $N \leq 4$ allowable $L > 4.0\text{mm} , W > 0.5\text{mm}$ is not allowed			
4	Ghost image	Allowed in switching process	MI	Visual inspection	
5	Flash dot / Multilateral	Flash points are allowed when switching screens Multilateral colors outside the frame are allowed for fixed screen time	MI	Visual/ Inspection card	Zone A Zone B
6	Segmented display	Selection segments are all displayed, and other segments are not displayed after the selection segment.	MA	Visual inspection	Zone A
7	Short circuit/ Circuit break/ Abnormal Display	Not Allow			



12.6.2 Appearance inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	B/W spots /Bubble/ Foreign bodies/ Dents	 $D \leq 0.3\text{mm}$, Allowed $0.3\text{mm} < D \leq 0.5\text{mm}$, $N \leq 5$ $D > 0.5\text{mm}$, Not Allow	MI	Visual inspection	Zone A
2	Glass crack	Not Allow	MA	Visual / Microscope	Zone A Zone B
3	Dirty	Allowed if can be removed	MI		Zone A Zone B
4	Chips/Scratch/ Edge crown	 $X \leq 3\text{mm}$, $Y \leq 0.5\text{mm}$, $t =$ not counted, and without affecting the electrode, permissible  $X \leq 2\text{mm}$ or $Y \leq 2\text{mm}$, $t =$ not counted, and without affecting the electrode, permissible  $W \leq 0.1\text{mm}$, $L \leq 5\text{mm}$ without affecting the electrode, $n \leq 2$	MI	Visual / Microscope	Zone A Zone B
5	TFT Cracks	 Not Allow	MA	Visual / Microscope	Zone A Zone B
6	Dirty/ foreign body	Allowed if can be removed/ allow	MI	Visual / Microscope	Zone A / Zone B
7	FPC broken/ FPC oxidation / scratch	  Not Allow	MA	Visual / Microscope	Zone B



8	B/W Line	 $L \leq 1.0\text{mm}, W \leq 0.15\text{mm}$ negligible $1.0\text{mm} < L \leq 4.0\text{mm}$ $0.15\text{mm} < W \leq 0.5\text{mm}$ $N \leq 4$ allowable $L > 4.0\text{mm}, W > 0.5\text{mm}$ is not allowed	MI	Visual / Ruler	Zone B
9	TFT edge bulge /TFT chromatic aberration	TFT edge bulge : $X \leq 3\text{mm}, Y \leq 0.3\text{mm}$ Allowed TFT chromatic aberration :Allowed	MI	Visual / Microscope	Zone A Zone B
10	Electrostatic point	$D \leq 0.25\text{mm}$, allow $0.25\text{mm} < D \leq 0.4\text{mm}$, $n \leq 4$ allow $D > 0.4\text{mm}$ is not allowed ($n \leq 8$ items are allowed within 5 mm in diameter)	MI	Visual / Microscope	Zone A
11	PCB damaged/ Poor welding/ Curl	PCB (Circuit area) damaged Not Allow PCB Poor welding Not Allow PCB Curl $\leq 1\%$	MI	Visual / Ruler	Zone B
12	Edge glue height/ Edge glue bubble	Edge Adhesives $H \leq$ PS surface (Including protect film) Edge adhesives seep in $\leq 1/2$ Margin width Length excluding Edge adhesives bubble: bubble Width $\leq 1/2$ Margin width; Length $\leq 5.0\text{mm}$. $n \leq 5$	MI		
13	Protect film	Surface scratch but not effect protect function, Allow	MI	Visual Inspection	
14	Silicon glue	Thickness $\leq$ PS surface (With protect film): Full cover the IC; Shape: The width on the FPC $\leq 0.5\text{mm}$ (Front) The width on the FPC $\leq 1.0\text{mm}$ (Back) smooth surface, No obvious raised.	MI	Visual Inspection	
15	Warp degree (TFT substrate)	 $t \leq 1.5\text{mm}$	MI	Ruler	Zone B
16	Color difference in COM area (Silver point area)	Allowed		Visual Inspection	



13. Matched Development Kit

Our Development Kit designed for SPI E-paper Display aims to help users to learn how to use E-paper Display more easily. It can refresh black-white E-paper Display, three-color (black, white and red/Yellow) E-paper Display and four-color (black, white, red and yellow) YOURITECH's E-paper Display. And it is also added the functions of USB serial port, FLASH chip, font chip, current detection ect.

Development Kit consists of the development board and the pinboard.

Supported development platforms include STM32, ESP32, ESP8266, Arduino UNO, etc.



14. Handling, Safety and Environmental Requirements

WARNING
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

Data sheet status	
Product specification	The data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

Product Environmental certification
RoHS



15. Precautions

- (1) Do not apply pressure to the EPD panel in order to prevent damaging it.
- (2) Do not connect or disconnect the interface connector while the EPD panel is in operation.
- (3) Do not touch IC bonding area. It may scratch TFT lead or damage IC function.
- (4) Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.
- (5) If the EPD Panel / Module is not refreshed every 24 hours, a phenomena known as “Ghosting” or “Image Sticking” may occur. It is recommended to refreshed the ESL /EPD Tag every 24 hours in use case. It is recommended that customer ships or stores the ESL / EPD Tag with a completely white image to avoid this issue
- (6) High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel’s performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time.

