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深圳市优瑞泰克科技有限公司
SHENZHEN YOURITECH TECHNOLOGY CO.,LTD

Doc. Number: V2

□ **Tentative Specification**
■ **Preliminary Specification(DR2)**
□ **Approval Specification**

MODEL NO.: ET103IPS-27A
SUFFIX:

Customer:

APPROVED BY **SIGNATURE**

Name / Title _____ _____

Note :

_____

Approved By	Checked By	Prepared By

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REVISION HISTORY

Version	Date	Page	Description
V1	2018/11/20	All	Pre-Spec Ver.0.0 was first issued.
V2	2018/11/27	7	Update pin assignment discussion

1. GENERAL DESCRIPTION

1.1 OVERVIEW

is a 10.25” (10.25” diagonal) TFT Liquid Crystal Display FOG without LED Backlight unit and with 50 pins LVDS interface. This FOG supports 1920 X 720 display mode.

1.2 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Screen Size	10.25” diagonal		
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1920 x R.G.B. x 720	pixel	-
Pixel Pitch	0.1269 (H) x 0.1269 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16,777,216 (8bit color depth)	color	-
Transmissive Mode	Normally black	-	-
Surface Treatment	HC	-	-
Transmittance	4.2	%	Typ.
Power Consumption	650	*mW*	(1)

Note (1) The specified power consumption (with converter efficiency) is under the conditions at VDD = 3.3 V, f = 60 Hz, and Ta = 25 ± 2 ºC, whereas white pattern is displayed.

2. MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Outline Dimension	Horizontal (H)	265.00	265.20	265.45	mm	(1)
	Vertical (V)	109.50	109.80	110.10	mm	
	Thickness (T)	4.76	5.06	5.36	mm	
CF Polarizer	Horizontal	247.85	248.05	248.25	mm	(1)
	Vertical	95.97	96.17	96.37	mm	
TFT Polarizer	Horizontal	247.85	248.05	248.25	mm	(1)
	Vertical	95.84	96.04	96.24	mm	
Active Area	Horizontal		243.65		mm	
	Vertical		91.37		mm	
Weight			83		g	

Note (1) Please refer to the attached drawings.

3. ABSOLUTE MAXIMUM RATINGS

3.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Voltage	V_{DD}	-0.3	4.0	V	
Storage Temperature	T_{ST}	-30	85	ºC	(1)(2)
Operating Ambient Temperature	T_{OP}	-40	90	ºC	(1)(2)

Note 1 : The absolute maximum rating values of this product are not allowed to be exceeded at any times. Should a module be used with any of the absolute maximum ratings exceeded, the characteristics of the module may not be recovered, or in an extreme case, the module may be permanently destroyed.

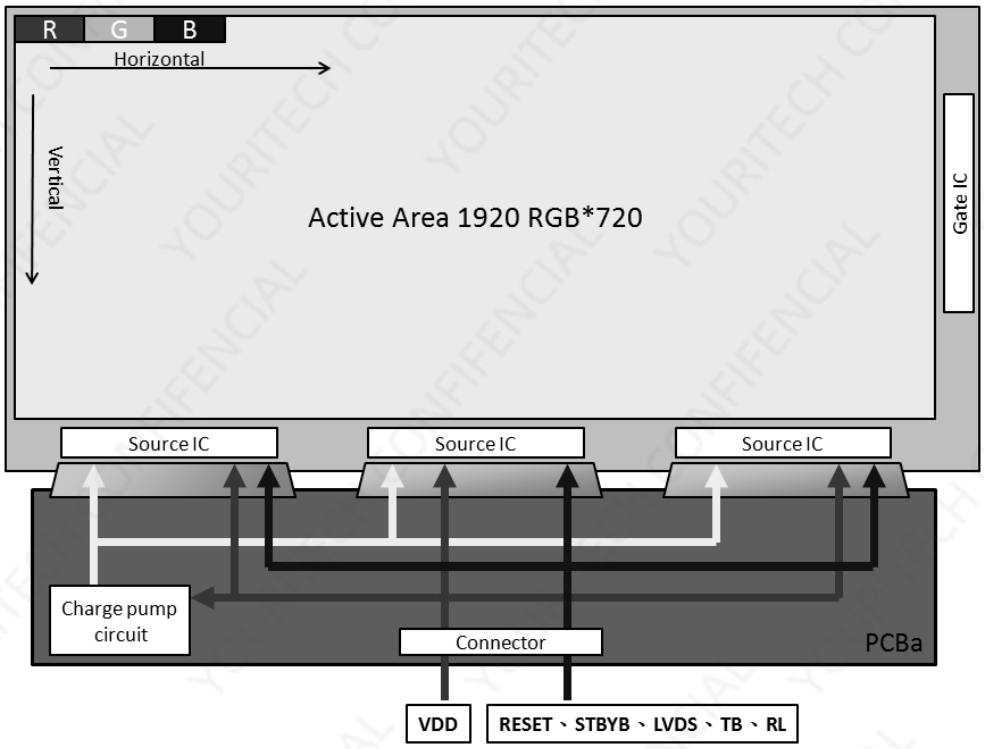
Note 2 : This rating applies to all parts of the module and should not be exceeded.

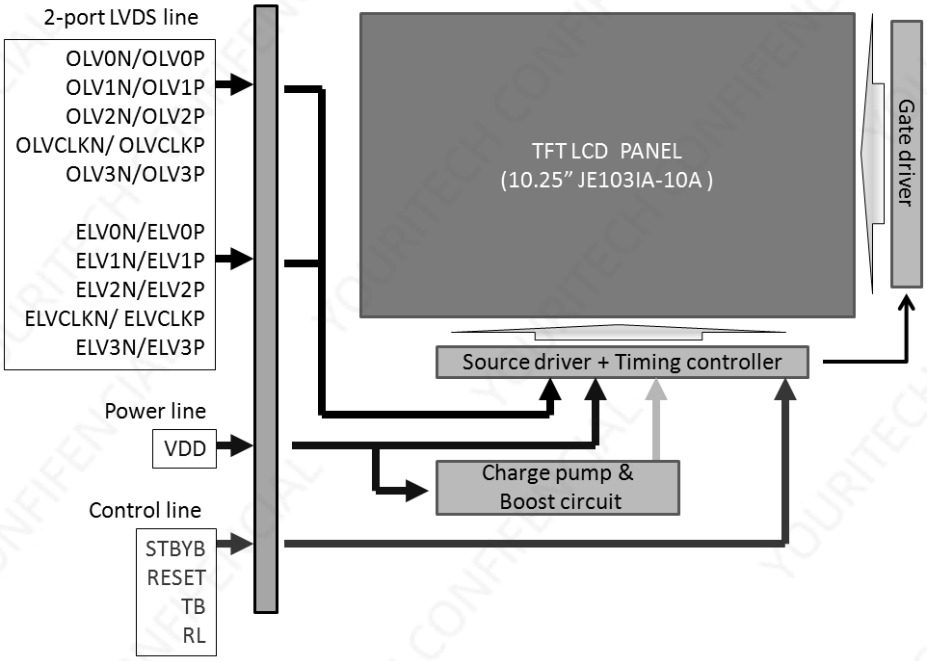
4. ELECTRICAL SPECIFICATIONS

4.1 DESCRIPTION DISPLAY ELECTRONICS

The display module comes with an 8 bits LVDS interface. The display's data and control signals (RESET, STBYB …) , which generates all necessary control signals for the source driver and gate driver. Single VDD voltage inputs are required for display functional operation. Gamma setting adjustment is done by Innolux with default value. Please refer to the block diagram in section 4.2.

4.2 BLOCK DIAGRAM





4.3 TYPICAL OPERATION CONDITIONS

Ta=25℃

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Power voltage	V_{DD}	3.1	3.3	3.6	V	Note 1,2
Power Supply Input Current	I_{DD}	145	165	185	mA	Note 3
Input logic high voltage	V_{IH}	0.7 V_{DD}	-	V_{DD}	V	Note 4
Input logic low voltage	V_{IL}	GND	-	0.3 V_{DD}	V	

Note 1: VDD setting should match the signals output voltage of customer's system board.

Note 2: The ripple voltage should be controlled under 5% of VDD

Note 3: Full white pattern.

Note 4: RESET, STBYB , RL, TB

4.4 INTERFACE CONNECTIONS

The Connector recommended model is 20647-050E-01 manufactured by I-PEX.

Connector type：I-PEX 20647-050E-01			
Pin	Input signal name	I/O pin (I:input, O:output, P:power)	Description
1	GND	P	Ground
2	VDD	P	External main and I/O power supply ; Power3.3V
3	VDD	P	External main and I/O power supply : Power3.3V
4	VDD	P	LCD Maker Use, keep connecting 3.3 V
5	RESET	I	Global reset pin (Default high), active low.
6	STBYB	I	Standby mode setting pin (Default high), active low.
7	GND	P	Ground
8	OLV0N	I	LVDS odd data 0-
9	OLV0P	I	LVDS odd data 0+
10	GND	P	Ground
11	OLV1N	I	LVDS odd data 1-
12	OLV1P	I	LVDS odd data 1+
13	GND	P	Ground
14	OLV2N	I	LVDS odd data 2-

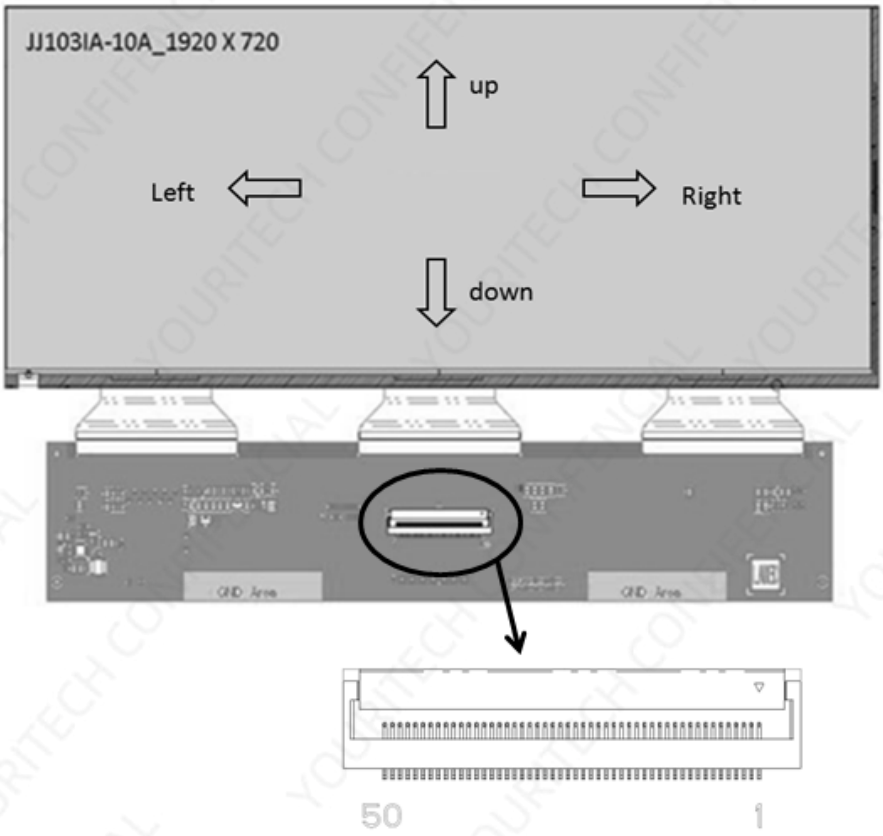
15	OLV2P	I	LVDS odd data 2+
16	GND	P	Ground
17	OLVCLKN	I	LVDS odd clk -
18	OLVCLKP	I	LVDS odd clk +
19	GND	P	Ground
20	OLV3N	I	LVDS odd data 3-
21	OLV3P	I	LVDS odd data 3+
22	GND	P	Ground
23	ELV0N	I	LVDS even data 0-
24	ELV0P	I	LVDS even data 0+
25	GND	P	Ground
26	ELV1N	I	LVDS even data 1-
27	ELV1P	I	LVDS even data 1+
28	GND	P	Ground
29	ELV2N	I	LVDS even data 2-
30	ELV2P	I	LVDS even data 2+
31	GND	P	Ground
32	ELVCLKN	I	LVDS even clk -
33	ELVCLKP	I	LVDS even clk +
34	GND	P	Ground
35	ELV3N	I	LVDS even data 3-
36	ELV3P	I	LVDS even data 3+
37	GND	P	Ground
38	GND	P	LCD Maker Use,keep connect Ground
39	RL	I	Horizontal shift direction (source output) selection. RL = 1: Left -> Right(default: Customer to Pull high, internal IC Pull high*) RL = 0: Right -> Left
40	TB	I	Vertical shift direction (gate output) selection. TB = 0: Bottom->Top TB = 1: Top ->Bottom (default: Customer to Pull high, internal IC Pull high*)
41	GND	P	LCD Maker Use,keep connect Ground
42	GND	P	LCD Maker Use,keep connect Ground
43	VDD	P	LCD Maker Use,keep connecting 3.3 V
44	VDD	P	LCD Maker Use,keep connecting 3.3 V
45	NC		Ground
46	NC		Ground
47	NC		Ground

48	NC		Ground
49	NC		Ground
50	NC		Ground

Note (1)

SHLR	UPDN	Data shifting
VDD	VDD	Left→Right，UP→Down(default)
VDD	GND	Left→Right，Down→UP
GND	VDD	Right→Left，UP→Down
GND	GND	Right→Left，Down→UP

Refer to the figure as below:

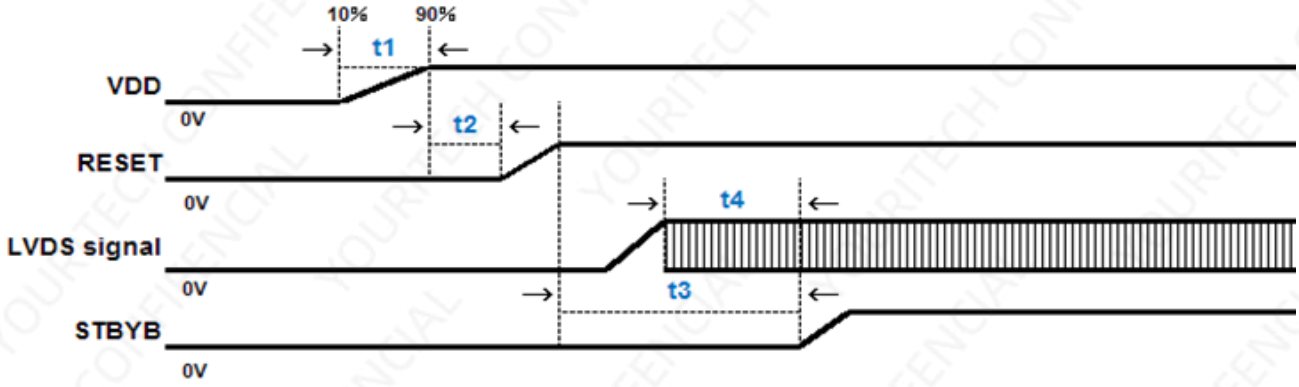


4.5 POWER ON/OFF TIMING SEQUENCE

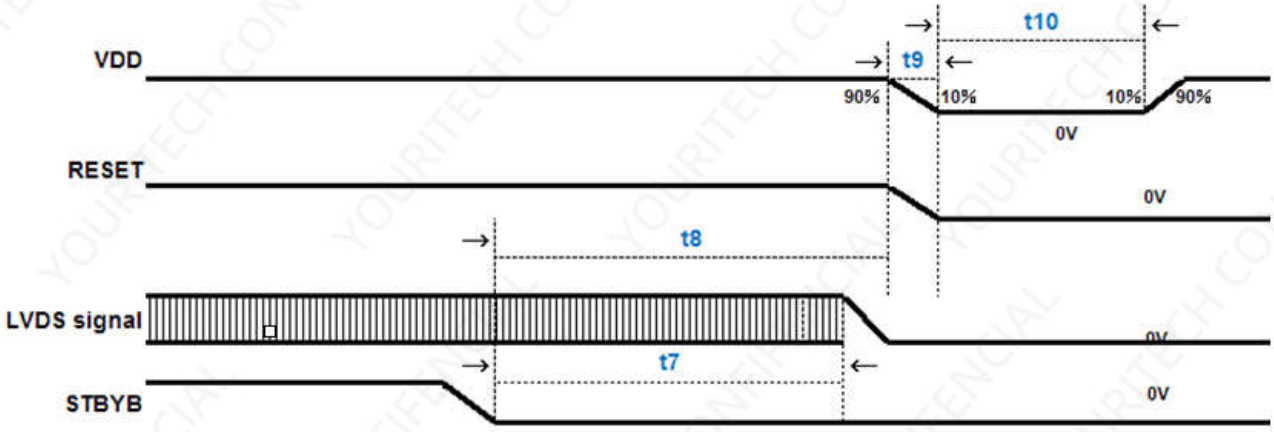
The recommended power on sequence should be: VDD → RESET → STBYB. To power off, reverse this sequence, or turn off all signals and power simultaneously.

VDD=3.0~3.6V

Power on：



Power off：



Symbol	SPEC.			Unit
	Min.	Typ.	Max.	
t1	1.5	2	3	ms
t2	1	5	10	ms
t3	0	30	50	ms
t4	0	5	10	ms
t7	7(117)	9(150.3)	10(167)	frame(ms)
t8	8(133.6)	10(167)	11(183.7)	frame(ms)
t9	0	1	3	ms
t10	1000	2000	3000	ms

4.6 Timing Characteristics

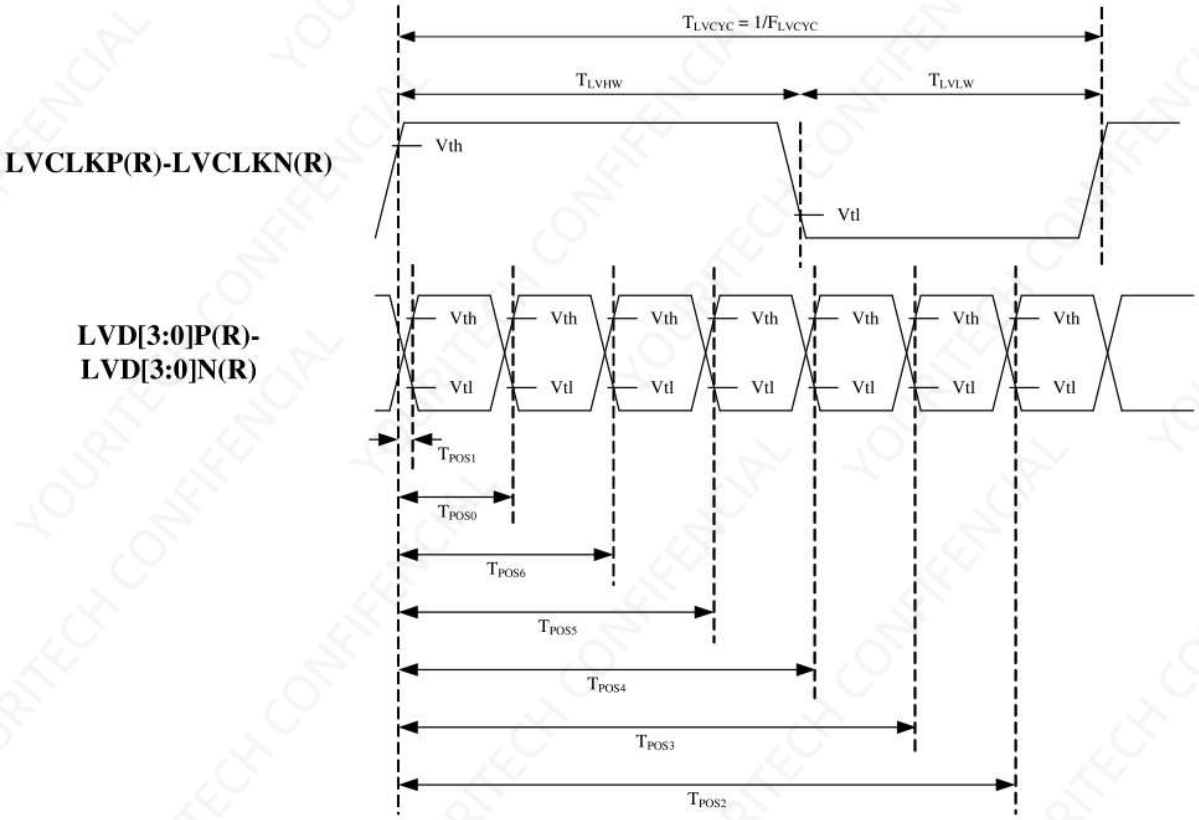
4.6.1. AC Electrical Characteristics

Parameter	Symbol	Spec.			Unit	Remark
		Min.	Typ.	Max.		
Clock frequency	FLVCYC	20	-	85	MHz	Frame rate=60Hz
Clock Period	TLVCYC	11.76	-	50	Nsec	Frame rate=60Hz
1 data bit time	UI	-	1/7	-	TLVCYC	
Position 1	TPOS1	-0.2	0	0.2	UI	Note 1
Position 0	TPOS0	0.8	1	1.2	UI	
Position 6	TPOS6	1.8	2	2.2	UI	
Position 5	TPOS5	2.8	3	3.2	UI	
Position 4	TPOS4	3.8	4	4.2	UI	
Position 3	TPOS3	4.8	5	5.2	UI	
Position 2	TPOS2	5.8	6	6.2	UI	
Input eye width	TEYEW	0.6	-	-	UI	
Input eye border	TEX	-	-	0.2	UI	
LVDS wake up time	TENLVDS	-	-	150	ns	

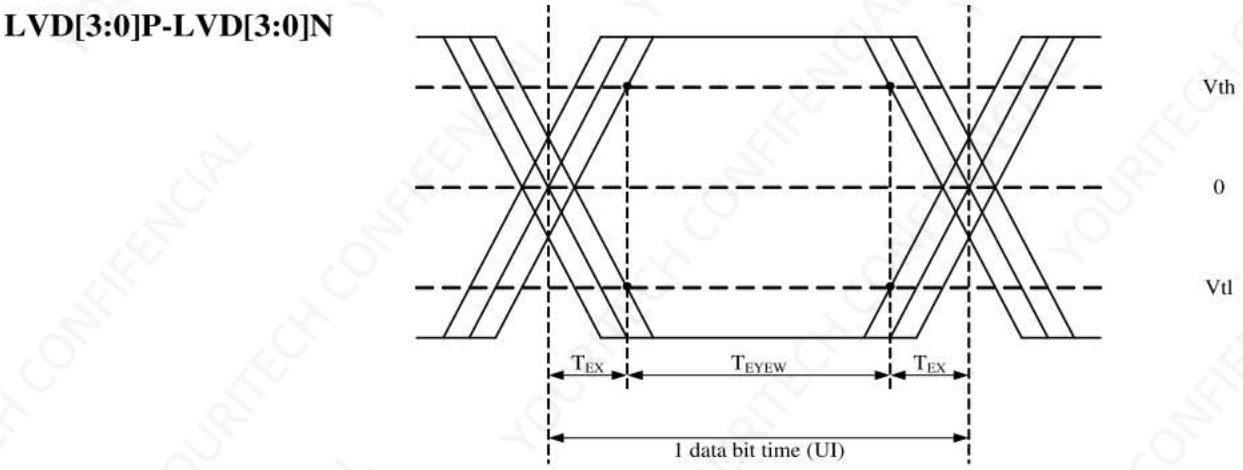
Note1 : Please refer to “4.6.2 LVDS input timing Diagram”

4.6.2. AC Electrical Characteristics

LVDS input timing:



Differential:

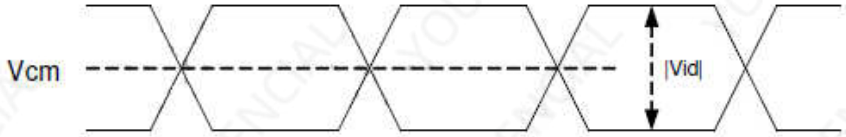


LVDS input eye diagram

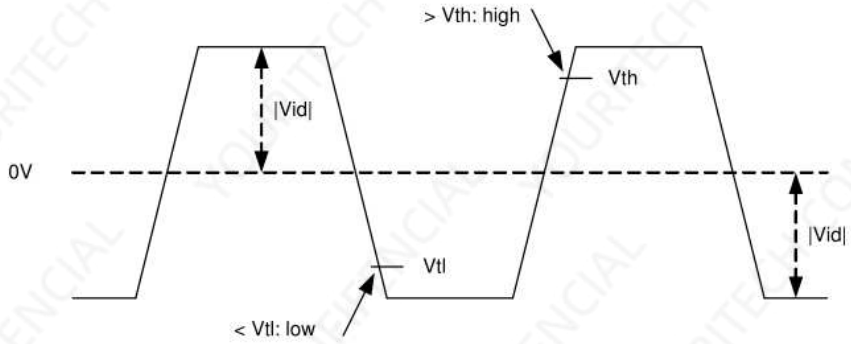
4.6.3. DC Electrical Characteristics

Parameter	Symbol	Spec.			Unit	Remark
		Min.	Typ.	Max.		
Differential input high Threshold voltage	Vth	-	-	+0.1	V	Vcm=1.2V
Differential input low Threshold voltage	Vtl	-0.1	-	-	V	
Differential input common Mode voltage	Vcm	1	1.2	$1.7-\|V_{id}\|/2$	V	-
Differential input voltage	|Vid|	0.2	-	0.6	V	-
Differential input leakage Current	Vleak	-10	-	+10	μA	-

Single-ended:
LVCLKP(R),
LVCLKN(R),
LVD[3:0]P(R),
LVD[3:0]N(R)



Differential:
LVCLKP(R)-LVCLKN(R),
LVD[3:0]P(R)-
LVD[3:0]N(R)



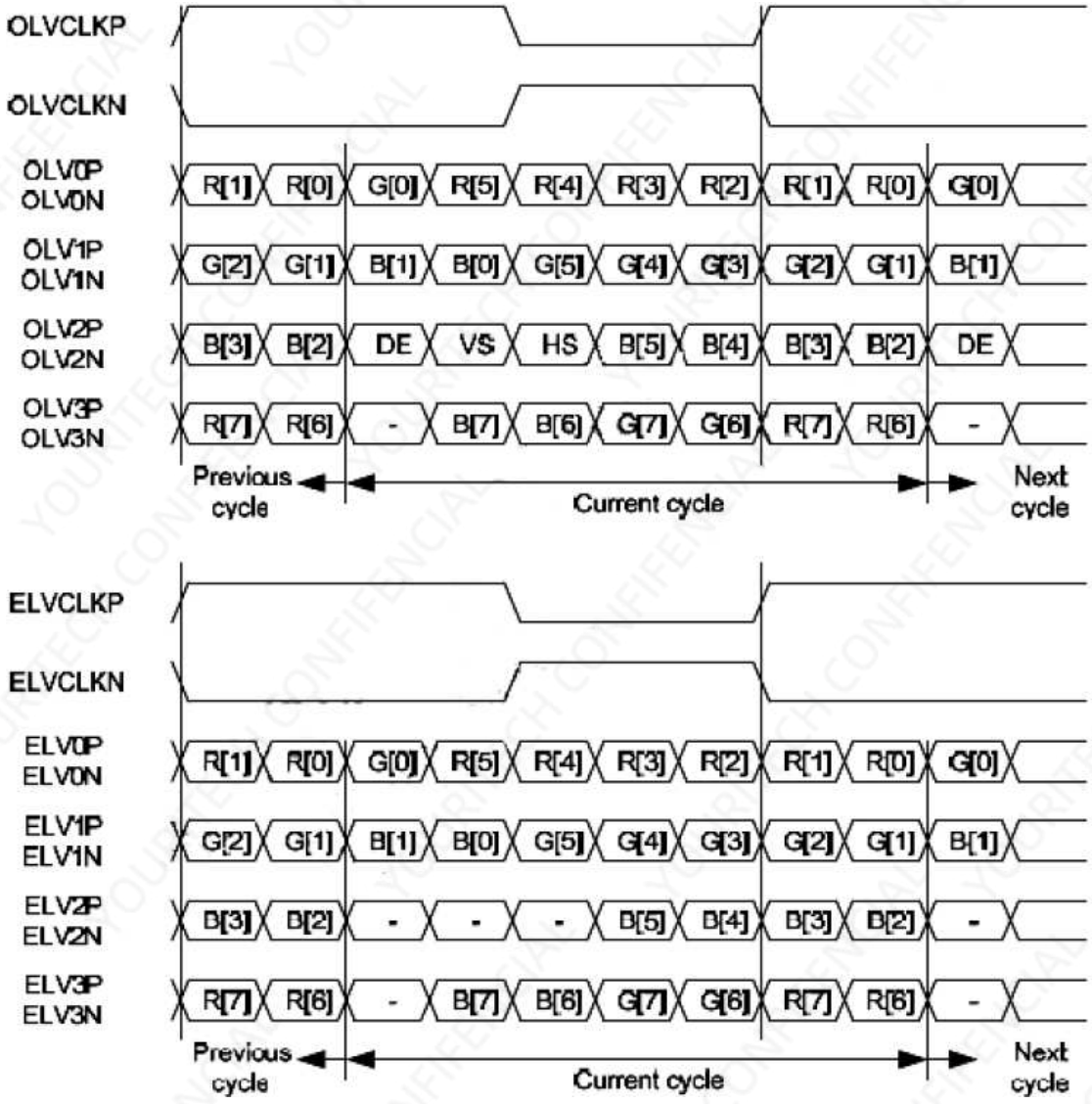
4.6.4. Timing

Parameter	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
CLK Frequency	F_{CLK}	-	44.1	-	MHz	
Horizontal valid data	t_{hd}		960		DCLK	
1 Horizontal Line	th	989	1002	1248	DCLK	
Vertical valid data	t_{vd}		720		H	
1 Vertical field	tv	727	733	936	H	
Frame rate	FR	-	60	-	Hz	

Note: DE mode only.

4.6.5. Data Input Format

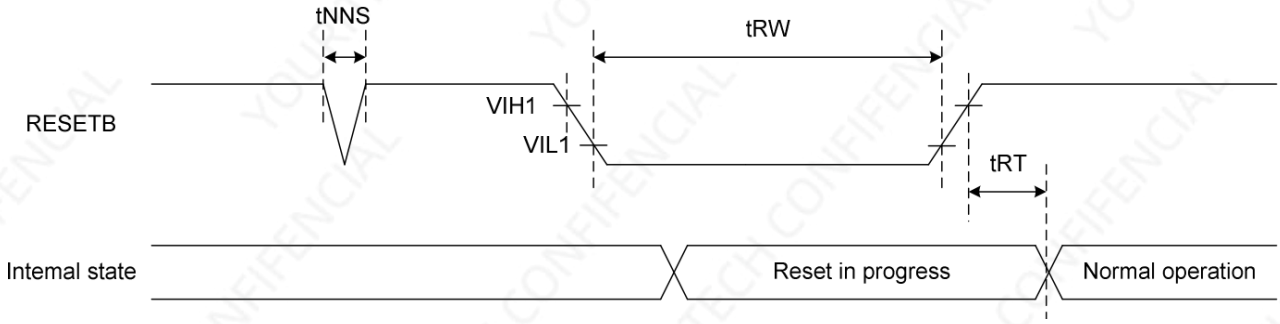
Panel LVDS format follow standard LVDS format:



VESA format (8bit)

Notice: Panel LVDS interface Spec, Odd = 1st Pixel, Even = 2nd Pixel

4.6.6. Resting timing



Signal	Parameter	Symbol	Spec.			Unit	Remark
			Min.	Typ.	Max.		
RESET	Reset pulse width	tRW	10	-	-	μs	-
	Reset complete time	tRT	-	-	5	μs	-
	Negative spike noise width	tNNS	-	-	100	ns	-

5. OPTICAL CHARACTERISTICS

5.1 TEST CONDITIONS

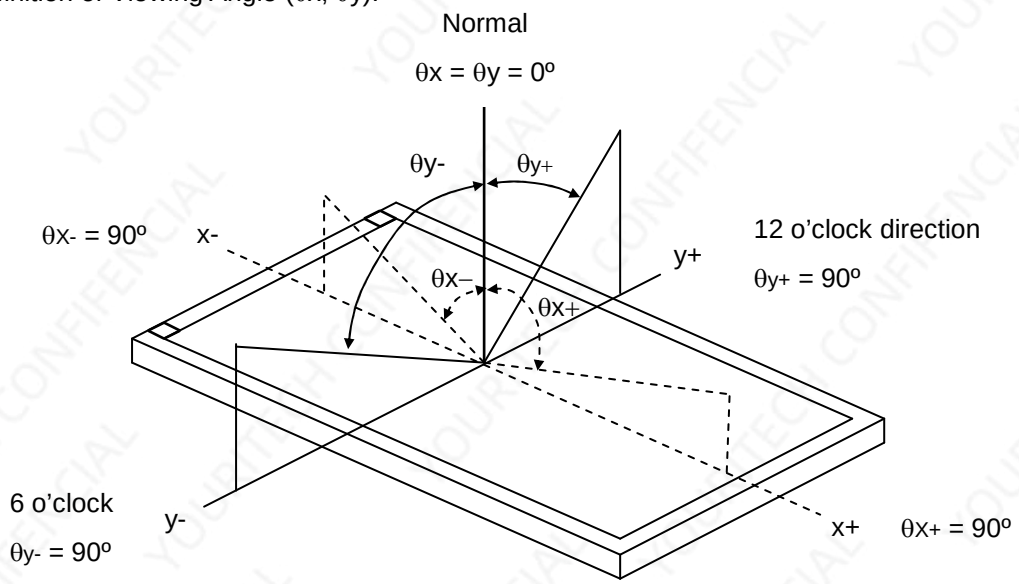
Item	Symbol	Value	Unit
Ambient Temperature	Ta	25	°C
Ambient Humidity	Ha	50	%RH
Supply Voltage	VDD	3.3	V
Input Signal	According to typical value in "4. ELECTRICAL CHARACTERISTICS"		

The measurement methods of optical characteristics are shown in Section 5.2. The following items should be measured under the test conditions described in Section 5.1 and stable environment shown in Note (5).

5.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Viewing Angle	Horizontal	x+	CR > 10	80	-	-	Deg.	(1), (4), (5)
		x-		80	-	-		
	Vertical	y+		80	-	-		
		y-		80	-	-		
Transmittance		T%	θ_x=0°, θ_Y =0°	3.68	4.22	-	%	(4), (5)
Contrast Ratio		CR		800	1000	-	-	(2), (4), (5)
Response Time		$T_{R+}T_F$		-	25	35	ms	(3), (5)
Color Coordinates	White	Wx		0.283	0.313	0.343	-	Panel under C light
		Wy		0.334	0.364	0.394		
	Red	Rx		0.628	0.658	0.688		
		Ry		0.300	0.330	0.360		
	Green	Gx		0.252	0.282	0.312		
		Gy		0.543	0.573	0.603		
	Blue	Bx		0.104	0.134	0.164		
		By		0.074	0.104	0.134		
NTSC				62	67		-	

Note (1) Definition of Viewing Angle (θx, θy):



Note (2) Definition of Contrast Ratio (CR):

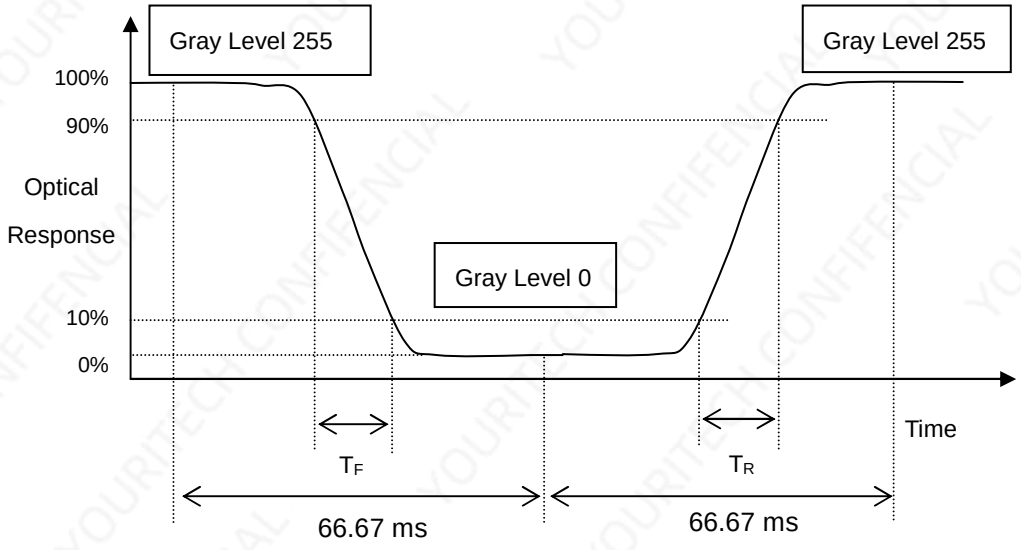
The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L255 / L0

L255: Luminance of gray level 255

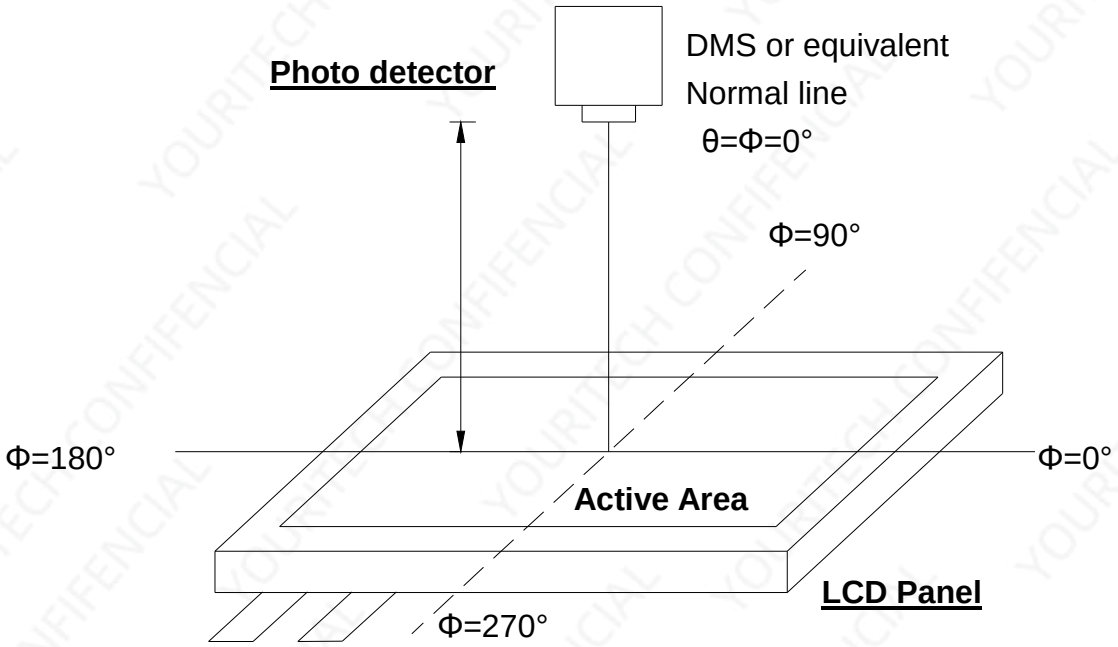
L 0: Luminance of gray level 0

Note (3) Definition of Response Time (T_R, T_F):



Note (4) Measurement Setup:

The LCD module should be stabilized at given temperature(T=+25℃) for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



Note (5) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted.

6. RELIABILITY TEST ITEM

Test Item	Test Condition	Note
High Temperature Storage Test	Ta=90ºC, 500 hours	Note 1 Note 2 Note 3 Note 4
Low Temperature Storage Test	Ta=-40ºC, 500 hours	
High Temperature Operation Test	Tp=85ºC, 500 hours	
Low Temperature Operation Test	Ta=-30ºC, 500 hours	
High Temperature & High Humidity Operation Test	Ta=60ºC, RH 90%, 500hours	
Thermal Shock	[(Ta=-30℃ 30min)→(Ta=85℃ 30min)]/cycle , 100cycles	
ESD Test	[Human Body Model] C=100pF, R=1.5KΩ ; Discharge: ±2KV	Note 2
Packaging Vibration Test	1.14Grms X, Y, Z three axes (30min /axis) [Frequency： 5Hz(0.015G2/Hz) , 100Hz(0.015G2/Hz)， 200Hz(0.0037G2/Hz)]	
Packaging Drop Test	1corner, 3edges, 6faces (1 time/direction) <follow ISTA(1A) height> 0kg≦W <10kg：76cm, 10kg≦W <19kg：61cm, 19kg≦W <28kg：46cm, 28kg≦W <45kg：31cm, 45kg≦W ≦68kg：20cm	

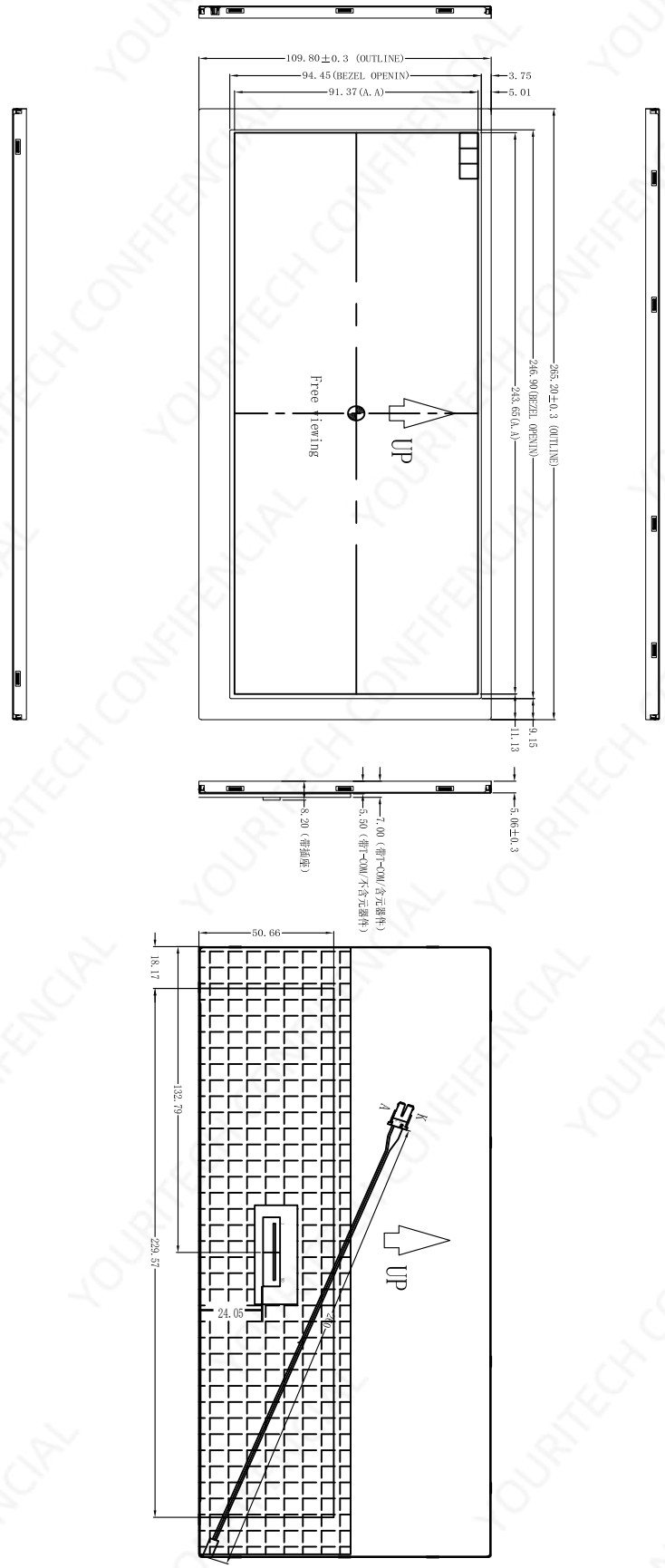
Note 1: Ta = Ambient Temperature, Tp = Panel Surface Temperature.

Note 2: Criteria: Normal display image with no obvious non-uniformity and no line defect.

Note 3: Evaluation should be tested after storage at room temperature for more than two hour

Note 4: A certain level of Mura (non-uniformity) of dark / black image will happen several days after high temperature testing (H.T.T.). There is a slowly part recovery over a long time (several months). Such a long exposure time like in H.T.T. will normally not happen in a real application. Therefore the test H.T.T. was introduced to simulate cycles with normal conditions in-between but with the same total exposure time what show a significant reduced Mura.The root cause is related to tension generated due to different amount of shrinking in the stack of layers in the polarizer sheet. The effect is more significant on larger displays like this size. An investigation into alternative polarizer material showed that there is no better alternative currently available.

MECHANICAL OUTLINE, UNIT:mm
(Unspecified Tolerances is: ±0.3 mm)

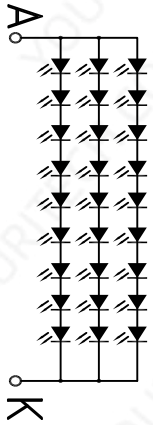


REV	DESCRIPTION:	DATE
V0	新发行	2021.05.10

ELECTRICAL-OPTICAL CHARACTERISTICS
(Ta=25℃. The Ambient temperature Ta=25℃)

Item		Symbol	Condition	min.	typ.	max.	Unit
Forward Current		U	If= 120 mA	24.3	26.8	31.5	V
Reverse Current		Ir	Vr= 5 V			10	μA
Power dissipation		Pd	If= 120 mA			5.67	W
Colour Coordinates	x		If= 120 mA		100		
	y				100		
BL Luminance (Center Area)		Lv	If= 120 mA	—	100		cd/m²
Luminous Uniformity			If= 120 mA	70	75		%
LCM Luminance(reference???)		Lv	If= 120 mA	400	500	—	cd/m²

Operating Temperature Range	Topr	normal use	-10	+60	℃
Storage Temperature Range	Tstg	normal use	-20	+65	℃



电路原理图：9串X3并=27 LED

PRODUCT NANE: 产品名称	CUST NUMBER: 客户型号	PROJECTION 三角法	SHEET: 页次 1 of 1
			APPROVALS 签字
			DESIGN: 设计
			CHECK: 核对
			APPROVE: 批准
			DATE 日期
			SCALE: 比例 FIT

8. PRECAUTIONS

8.1 HANDLING PRECAUTIONS

(1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9) Do not disassemble the module.

(10) Do not pull or fold the LED wire.

(11) Pins of I/F connector should not be touched directly with bare hands.

8.2 STORAGE PRECAUTIONS

(1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(3) It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slowly, and the starting voltage of LED will be higher than the room temperature.

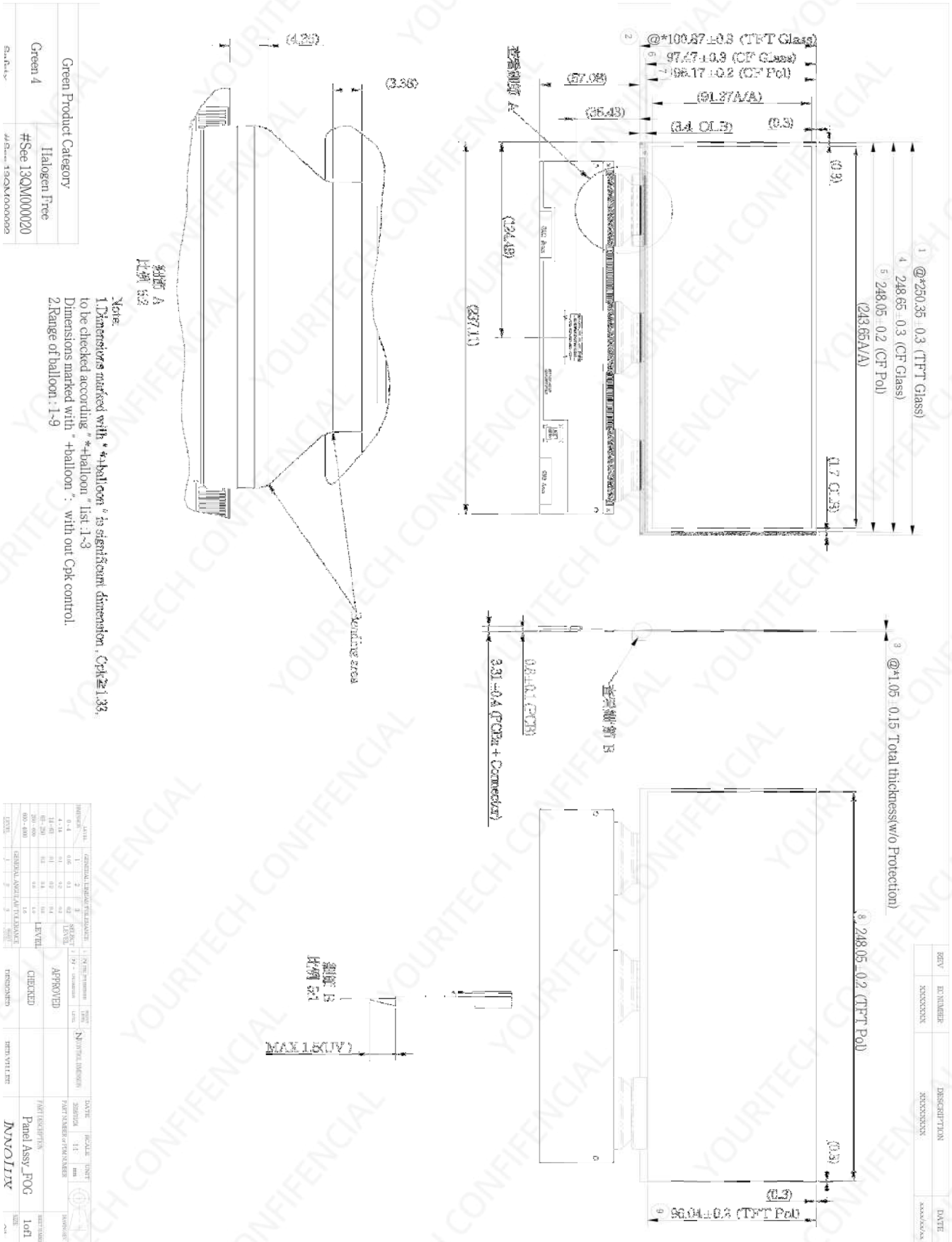
8.3 OPERATION PRECAUTIONS

(1) Do not pull the I/F connector in or out while the module is operating.

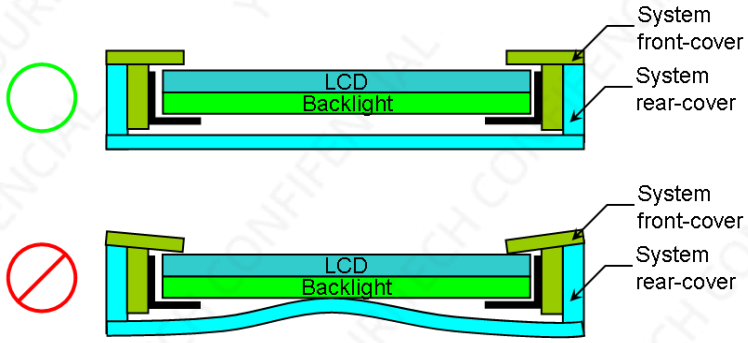
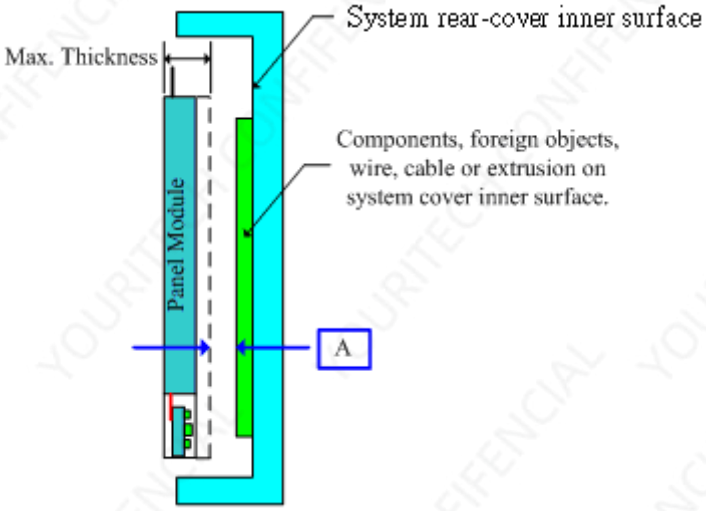
(2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.

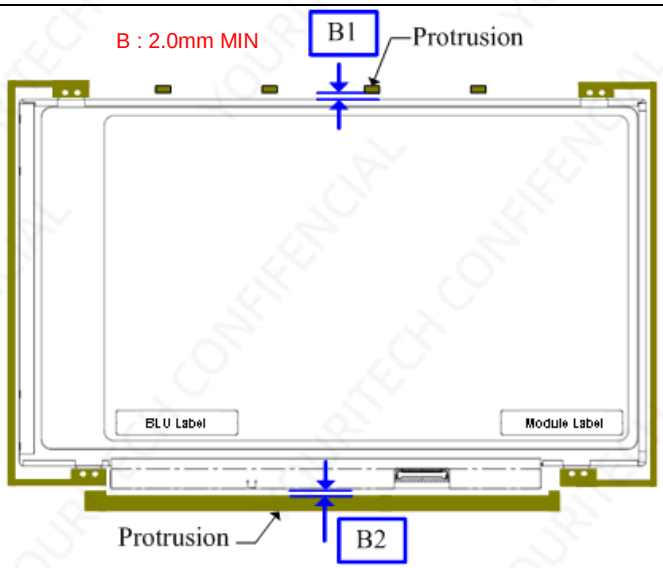
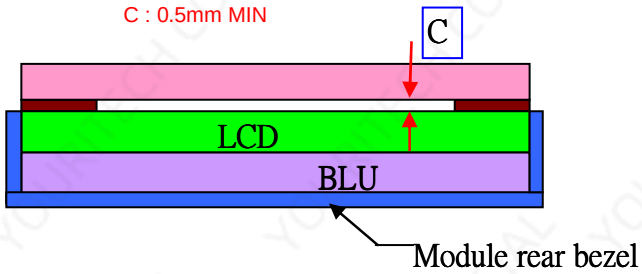
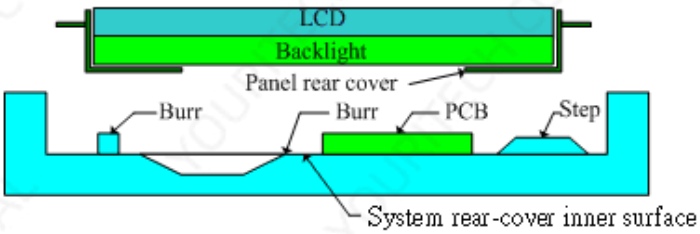
(3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with converter. Do not disassemble the module or insert anything into the backlight unit.

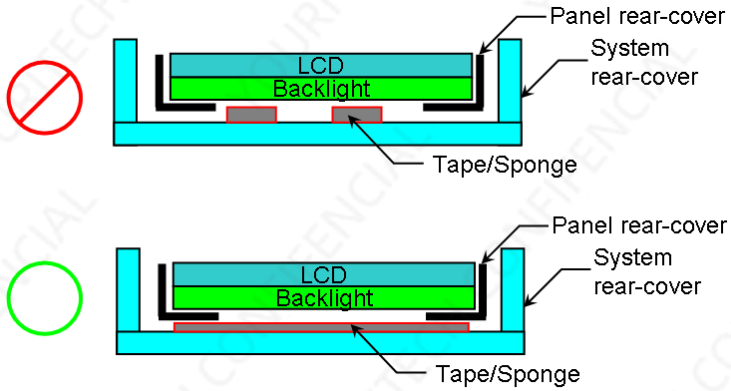
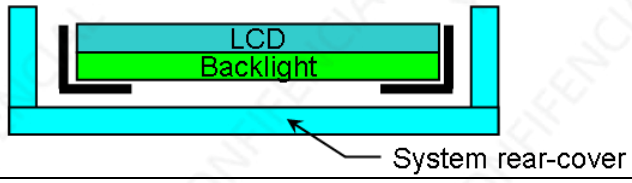
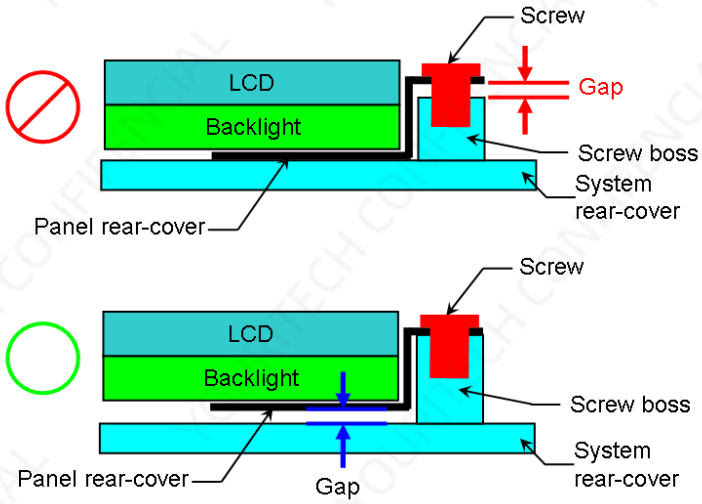
Appendix. OUTLINE DRAWING

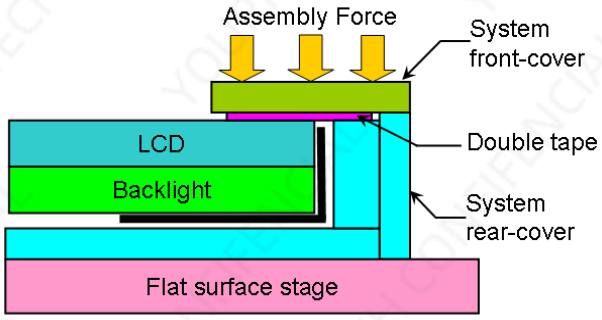


Appendix II. SYSTEM COVER DESIGN GUIDANCE

1.	**Permanent deformation of system cover after reliability test**
	
Definition	System cover including front and rear cover may deform during reliability test. Permanent deformation of system front and rear cover after reliability test should not interfere with panel. Because it may cause issues such as pooling, abnormal display, white spot, and also cell crack.
2.	**Design gap A between panel & any components on system rear-cover**
	
Definition	Gap between panel's maximum thickness boundary & system's inner surface components such as wire, cable, extrusion is needed for preventing from backpack or pogo test fail. Because zero gap or interference may cause stress concentration. Issues such as pooling, abnormal display, white spot, and cell crack may occur. Flatness of panel and system rear-cover should be taken into account for gap design.
3	**Design gap B1 & B2 between panel & protrusions**

	
Definition	Gap between panel & protrusions is needed to prevent shock test failure. Because protrusions with small gap may hit panel during the test. Issue such as cell crack, abnormal display may occur.
4	**Design gap C between touch panel & panel surface.**
	
Definition	Air gap design between touch panel & panel surface is needed to prevent pooling, newton ring or glass broken. Compression ration of double side tape may cause pooling issue or newton ring. This phenomenon is obvious during pooling inspection procedure. To remain sufficient gap between touch panel and panel surface is recommended.
5	**System rear-cover inner surface examination**
	
Definition	Burr at logo edge, steps, protrusions or PCB board may cause stress concentration. White spot or glass broken issue may occur during reliability test.
6	**Tape/sponge design on system inner surface**

<table>
<tr><td colspan="2"> 
</td></tr>
<tr><td>Definition</td><td>To prevent abnormal display & white spot after scuffing test, hinge test, pogo test, backpack test, tape/sponge should be well covered under panel rear-cover. Because tape/sponge in separate location may act as pressure concentration location.</td></tr>
<tr><td>7</td><td>Material used for system rear-cover</td></tr>
<tr><td colspan="2"> 
</td></tr>
<tr><td>Definition</td><td>System rear-cover material with high rigidity is needed to resist deformation during scuffing test, hinge test, pogo test, or backpack test. Abnormal display, white spot, pooling issue may occur if low rigidity material is used. Pooling issue may occur because screw’s boss positioning for module’s bracket are deformed during open-close test.
Solid structure design of system rear-cover may also influence the rigidity of system rear-cover. The deformation of system rear-cover should not caused interference.</td></tr>
<tr><td>8</td><td>Screw boss height design</td></tr>
<tr><td colspan="2"> 
</td></tr>
<tr><td>Definition</td><td>Screw boss height should be designed with respect to the height of bracket bottom surface to panel bottom surface + flatness change of panel itself. Because gap will exist between screw boss and bracket, if the screw boss height is smaller. As result while fastening screw, bracket will deformed and pooling issue may occur.</td></tr>
<tr><td>9</td><td>Assembly SOP examination for touch panel with double side tape design</td></tr>
</table>

<table>
<tr><td colspan="2"> 
</td></tr>
<tr><td>Definition</td><td>To prevent panel crack during touch panel assembly process with double tape design, it is only allowed to give slight pressure with large contact area. This can help to distribute the stress and prevent stress concentration. We also suggest putting the system on a flat surface stage to prevent unequal stress distribution during the assembly.</td></tr>
</table>