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Custom Display

Production Custom designs Installation

Mechanical design



MODEL NO : ET113BA01-T

MODEL VERSION: 01

SPEC VERSION : 1.0

ISSUED DATE: 2021-03-05

☐ Preliminary Specification

☒ Final Product Specification

Customer : _____

Approved by	Notes

Youri Confirmation

Prepared by	Reviewed by	Approved by
John	Johnny	Wang

1. Introduction

1.1 Scope of application

LCD specification: Dots 440xRGBx1920.

As to basic specification of the driver IC, refer to the IC (TBD) specification and data book.

All material & processing of the LCD module should be Lead Free.

1.2 TFT features:

Structure: TFT PANNEL+IC +FPC+BL;

ALL O'CLOCK Type LCD

440 dot-segment and 1920 dot-common outputs;

16.7M Color can be selected by software;

White LED back light;

4lane MIPI interface

1.3 Applications:

2. LCM General specification

ITEM	Standard value	Unit
LCD Type	Normally Black	--
Drive element	TFT active matrix	--
Number of pixels	440*3RGB(H)X1920(V)	Dots
Pixel arrangement	RGB stripe	--
Pixel Pitch (W*H)	0.1317(H) x0.1317 (V)	mm
Active area	57.90(H) x 252.69V)	mm
Module Size(W*H*T)	64.98(W) x266.39(H) x4.60(T)	mm
Viewing direction	ALL O'CLOCK	
TFT Driver IC	TBD	-
TFT interface	4lane MIPI interface	-
Approx. Weight	TBD	g
Touch structure	--	
Touch Driver IC		-
Touch Interface		

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3.Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
LCM Operating Temperature	T _{OPR}	-20	+70	°C
LCM Storage Temperature	T _{STG}	-30	+80	°C
Humidity	RH	10	90	%

4.Electrical Characteristics

4.1 TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage for I/O	VDDIO	3.0	3.3	3.3	V
Supply Voltage for(DC/DC)	VDD	3.0	3.3	3.6	V
Supply Voltage for(VGH)	VGH	10	12	14	V
Supply Voltage for(VGL)	VGL	-14	-12	-10	V
Supply Voltage for(AVDD)	AVDD	--	--	--	V
Supply Voltage for(VCOM)	VCOM	-2.5	TBD	0	V

4.2 Back-Light Unit Characteristics

The back-light system is an edge-lighting type with 16 white LEDs. The characteristics of the back-light are shown in the following tables.

Characteristics	Symbol	Min.	Type	Max.	Unit	Notes
Forward Voltage	V _F	--	27.3	--	V	-
Forward current	I _F	--	120	--	mA	-
Luminance(With LCD)	L _v	--	450	--	cd/m ²	-
LED life time	N/A	--	10000	--	Hr	Note 1

Note:

- (1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=30mA/LED. The LED life time could be decreased if operating I_L is larger than 45mA/LED.

5. Module Function Description

Pin No.	Symbol	Functional	Notes
1	GND	Ground	
2	NOP	MIPI data input	
3	DON	MIPI data input	
4	GND	Ground	
5	D1P	MIPI data input	
6	D1N	MIPI data input	
7	GND	Ground	
8	CLKP	MIPI data input	
9	CLKN	MIPI data input	
10	GND	Ground	
11	D2P	MIPI data input	
12	D2N	MIPI data input	
13	GND	Ground	
14	D3P	MIPI data input	
15	D3N	MIPI data input	
16	GND	Ground	
17	GND	Ground	
18-19	NC	Power supply(I/O) for digital circuits +3.3V input	
20-23	NC	No connection	
24	RSTB	Global reset pin	
25	STBYB	Standby mode, Normally pulled high	
26	NC	No connection	
27	GND	Ground	
28-29	BL-K	Back light-K	
30	GND	Ground	
31	NC	No connection	
32-33	GND	Ground	
34	NC	No connection	
35-36	BL-A	Back light-A	
37	GND	Ground	
38-39	VDD	Power supply for digital circuits +3.3V input	
40	NC	No connection	

6. Timing Characteristics

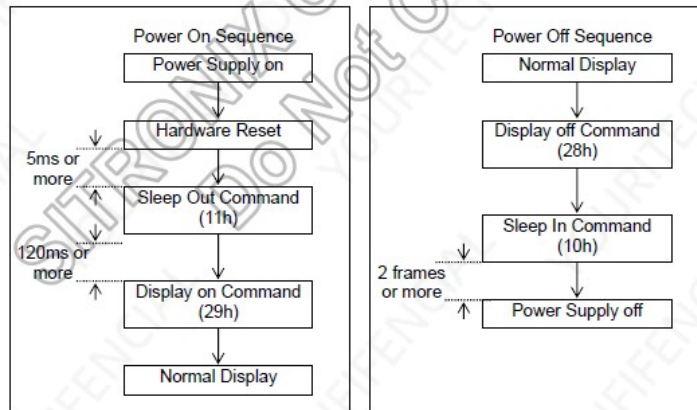
Power on/off sequence

Power source IOVCC, VCI can be applied and powered down in any order. IOVCC, VCI can be powered down in any order.

During power off, if LCD is in the Sleep Out mode, IOVCC, VCI must be powered down minimum 120msec after NRESET has been released.

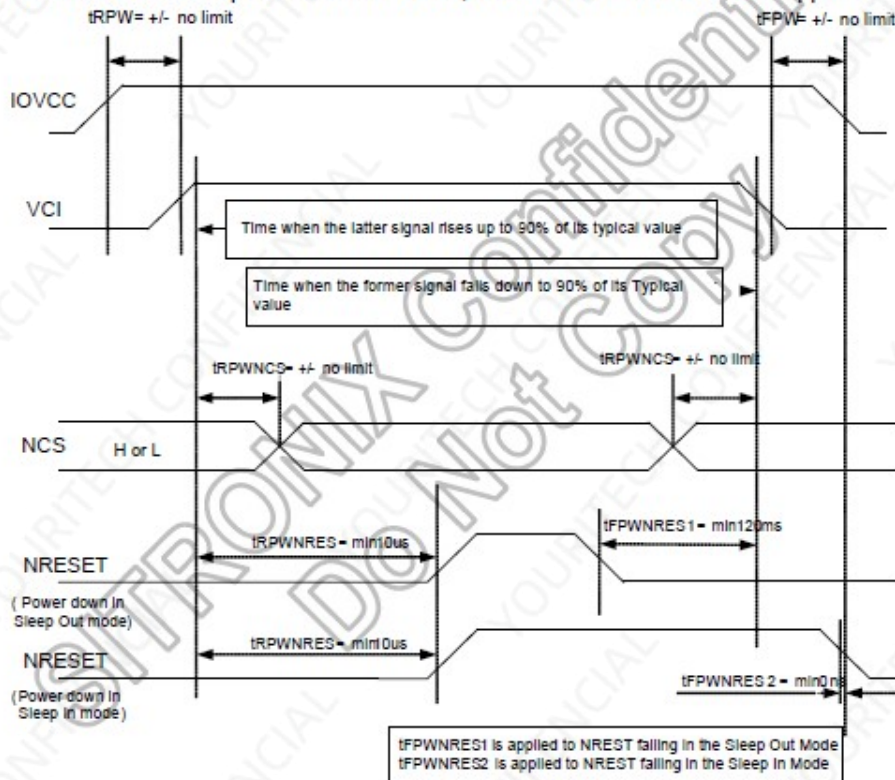
During power off, if LCD is in the Sleep In mode, IOVCC, VCI can be powered down minimum 0msec after NRESET has been released.

NCS can be applied at any timing or can be permanently grounded. NRESET has priority over NCS.



RESX line is held low by host at power on

If RESX line is held low (and stable) by the host during power on, then the RESX must be held low for minimum 10μsec after both VDD1, VDD2 and VDD3 have been applied.



Note: Unless otherwise specified timings herein show cross point at 50% of signal/power level

DSI Interface Timing Characteristics

High Speed Mode

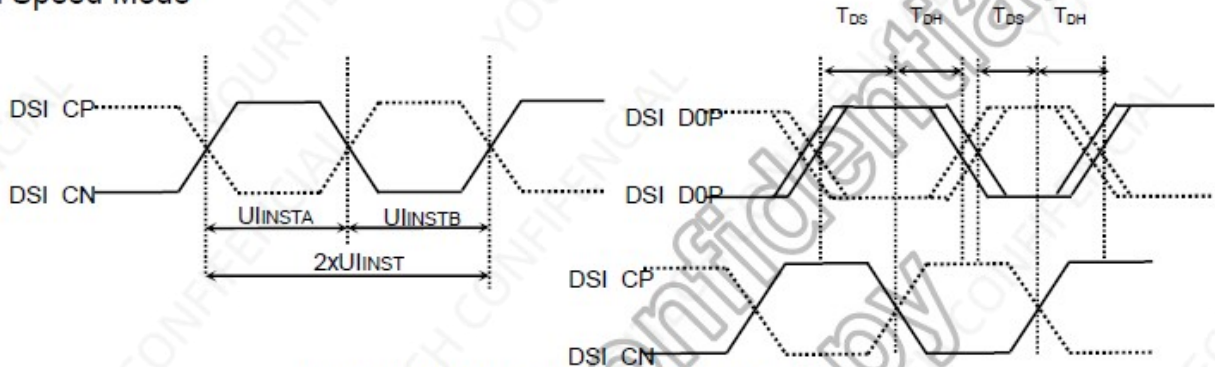


Figure 7.4: DSI clock timing Characteristics

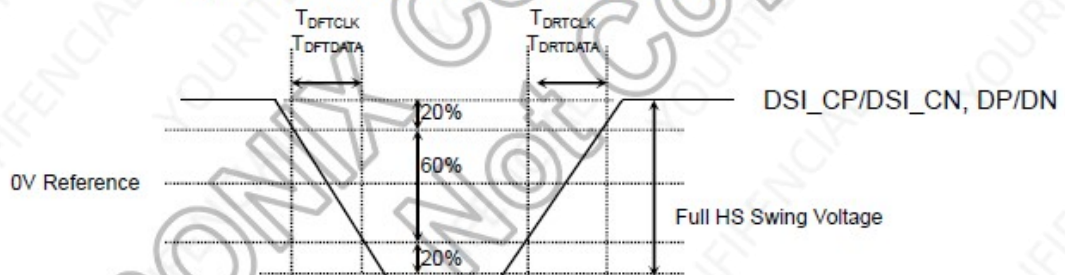


Figure 7.5: Rising and falling time on clock and data channel

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, TA = -30 to 70°C)

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Double UI instantaneous	2xUIINST	TBD	-	25	ns
	UI instantaneous	UIINSTA UIINSTB	TBD	-	12.5	ns
DP/DN	Data to clock setup time	T _{DS}	0.15xUI	-	-	ps
	Data to clock hold time	T _{DH}	0.15xUI	-	-	ps
DSI_CP/ DSI_CN	Differential rise time for clock	T _{DRTCLK}	150	-	0.3UI	ps
	Differential fall time for clock	T _{DFTCLK}	150	-	0.3UI	ps
DP/DN	Differential rise time for data	T _{DRTDATA}	150	-	0.3UI	ps
	Differential fall time for data	T _{DFTDATA}	150	-	0.3UI	ps

Table 7.3: DSI High Speed Mode characteristics

Low Power Mode

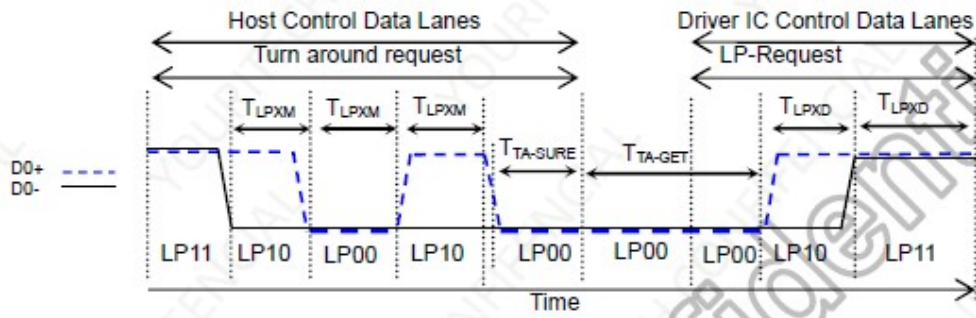


Figure 7.6: BTA from HOST to Display module Timing

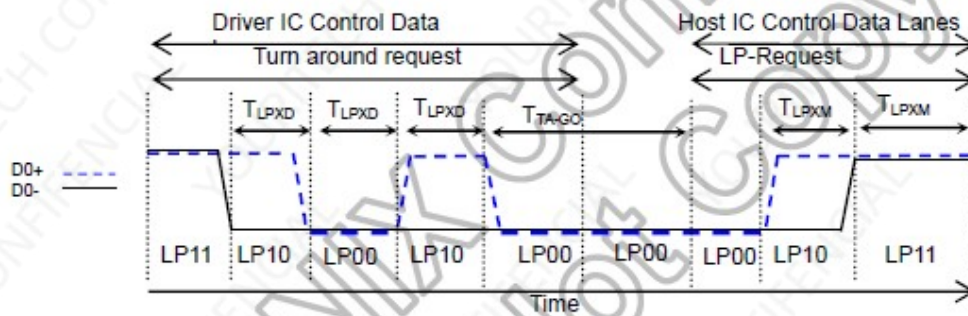
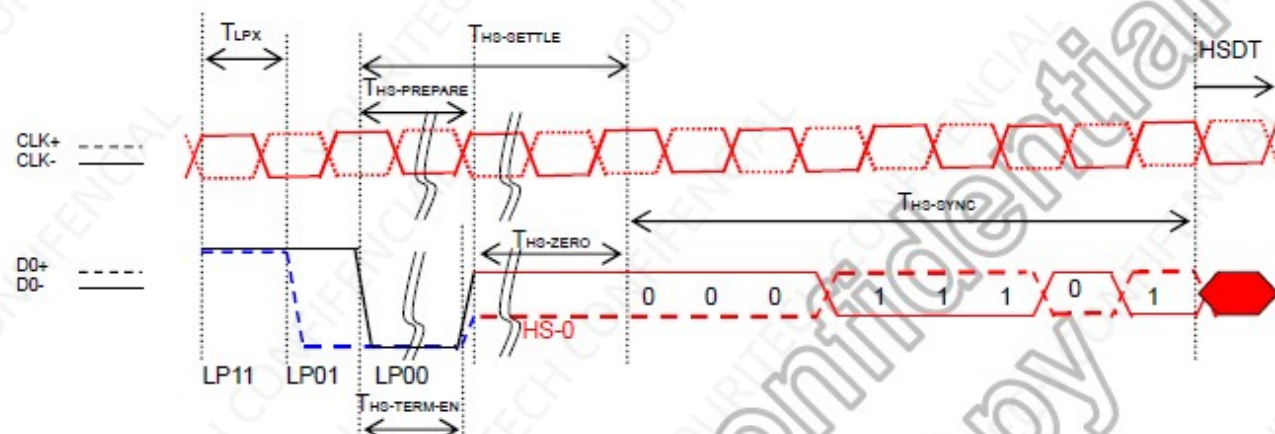


Figure 7.7: BTA from Display module Timing to HOST

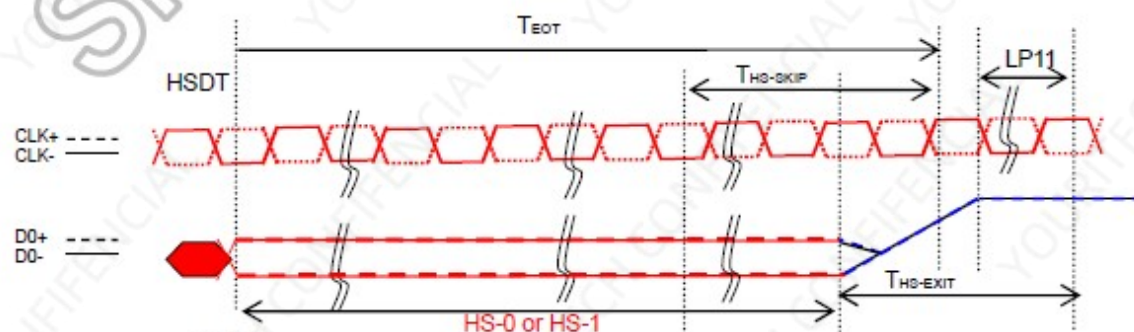
(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V, $T_A = -30$ to 70°C)

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11 Host → Display module	T_{LPXM}	50	-	-	ns
	Length of LP-00/LP01/LP10/LP11 Display module → Host	T_{LPXD}	50	-	-	ns
	Time-out before the MPU start driver	$T_{TA-SURE}$	T_{LPXD}	-	$2 \times T_{LPXD}$	ns
	Time to drive LP-00 by display module	T_{TA-GET}	$5 \times T_{LPXD}$	-	-	ns
	Time to drive LP-00 after turnaround request Host	T_{TAGO}	$4 \times T_{LPXD}$	-	-	ns

Table 7.4: DSI Low Power Mode characteristics

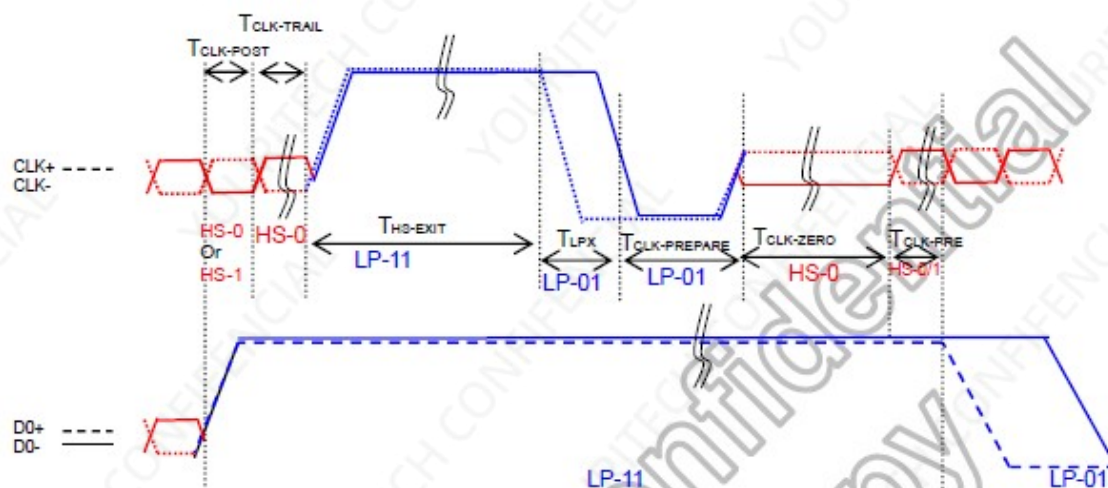


Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11	TLPX	50	-	-	ns
	Time to Driver LP-00 to prepare for HS transmission	T _{HS-PREPARE}	40+4UI	-	85+6UI	ns
	Time to enable data receiver line termination	T _{HS-TERM-EN}	-	-	35+4xUI	ns
	Time to drive LP-00 by display module	T _{TA-GET}	5xT _{LPXD}	-	-	ns
	Time to drive LP-00 after turnaround request Host	T _{TAGO}	4xT _{LPXD}	-	-	ns



NOTE:
If the last bit is HS-0, the transmitter changes from HS-0 to HS-1
If the last bit is HS-0, the transmitter changes from HS-1 to HS-0

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Time-Out at Display Module to Ignore Transition Period of EoT	T _{HS-SKIP}	40	-	55+4xUI	ns
	Time to Driver LP-11 after HS Burst	T _{HS-EXIT}	100	-	-	ns



Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Time that the MCU shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	T _{CLK-POST}	60+52xUI	-	-	ns
	Time to drive HS differential state after last payload clock bit of a HS transmission burst	T _{CLK-TRAIL}	60	-	-	ns
	Time to drive LP-11 after HS burst	T _{HS-EXIT}	100	-	-	ns
	Time to drive LP-00 to prepare for HS transmission	T _{CLK-PREPARE}	38	-	95	ns
	Time-out at Clock Lane Display Module to enable HS Termination	T _{CLK-TERM-EN}	-	-	38	ns
	Minimum lead HS-0 drive period before starting Clock	T _{CLK-PREPARE} + T _{CLK-ZERO}	300	-	-	ns
	Time that the HS clock shall be driven prior to any associated data Lane beginning the transition from LP to HS mode	T _{CLK-PRE}	8xUI			

Table 7.7: Clock Lanes High Speed Mode to/from Low Power Mode Timings

Reset input timing

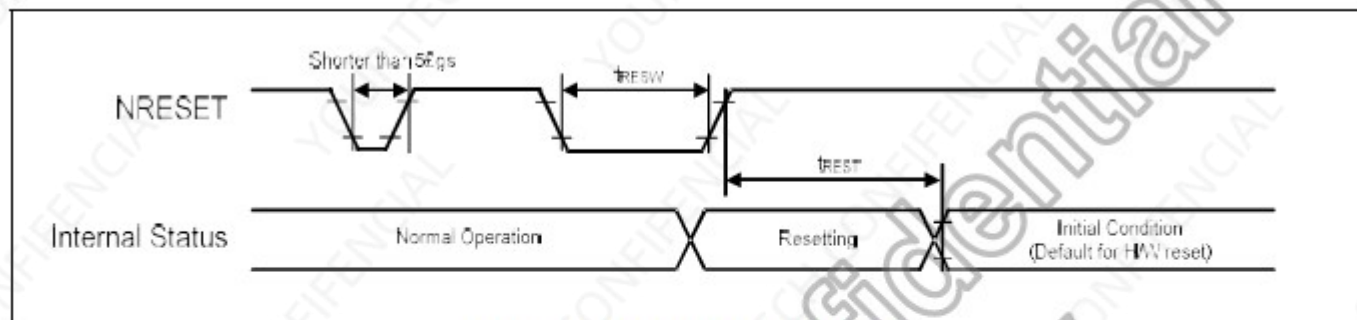


Figure 7.8: Reset input timing

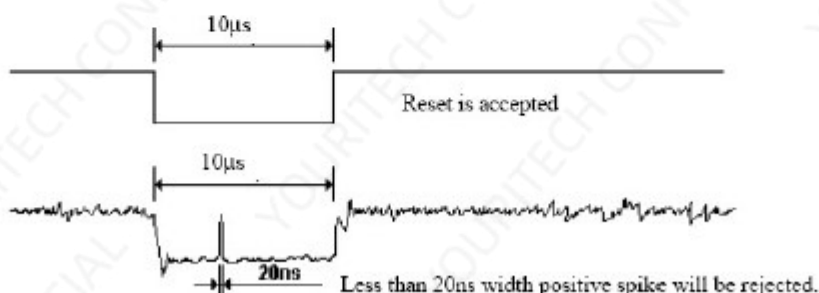
Symbol	Parameter	Related Pins	Spec.			Note	Unit
			Min.	Typ.	Max.		
tRESW	Reset low pulse width ⁽¹⁾	NRESET	10	-	-	-	µs
tREST	Reset complete time ⁽²⁾	-	5	-	-	When reset applied during SLPIN mode	ms
		-	120	-	-	When reset applied during SLPOUT mode	ms

Table 7.8: Reset input timing

Note: (1) Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the following table.

NRESET Pulse	Action
Shorter than 5 µs	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

- (2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which Maximum time is 120 ms, when Reset Starts in Sleep Out -mode. The display remains the blank state in Sleep In -mode) and then return to Default condition for H/W reset.
- (3) During Reset Complete Time, ID and VCOM value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of NRESET.
- (4) Spike Rejection also applies during a valid reset pulse as shown as below:



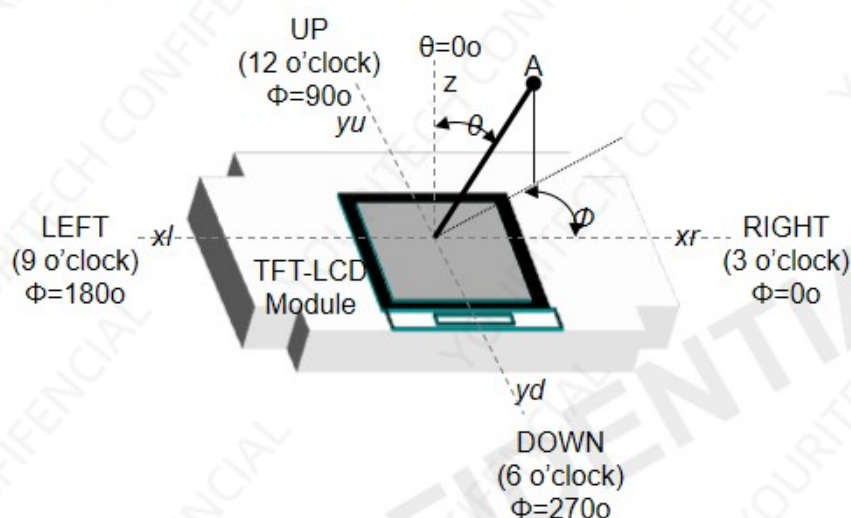
- (5) It is necessary to wait 5msec after releasing NRESET before sending commands. Also Sleep Out command cannot be sent for 120msec.

7. Optical Characteristics

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle Range	Horizontal	Θ_3	CR > 10	80	85	-	Deg.	Note 4.1
		Θ_9		80	85	-	Deg.	
	Vertical	Θ_{12}		80	85	-	Deg.	
		Θ_6		80	85	-	Deg.	
Contrast Ratio		CR	$\Theta = 0^\circ$	800	1000	-		APF Note 4.2/4.3
Cell Transmittance		Tr		4.7	5.65	-	%	
Reproduction of color		Rx	$\Theta = 0^\circ$	0.629	0.659	0.689		CF@C Light Note 4.4
		Ry		0.288	0.318	0.348		
		Gx		0.233	0.263	0.293		
		Gy		0.538	0.568	0.598		
		Bx		0.107	0.137	0.167		
		By		0.054	0.084	0.114		
		Wx		0.275	0.305	0.335		
		Wy		0.303	0.333	0.363		
Color Gamut			$\Theta = 0^\circ$	65	70	-	%	
Response Time		Tr	Ta= 25° C $\Theta = 0^\circ$	-	30	35	ms	Note 4.5
		Tf		-			ms	
		Tgray		-	-	-	ms	

Note 4.1: Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see Figure 8).

<Figure 6. Viewing Angle Range Is Defined As Follows>



Note 4.2: Contrast measurements shall be made at viewing angle of $\Theta=0^\circ$ and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. Luminance Contrast Ratio (CR) is defined mathematically.

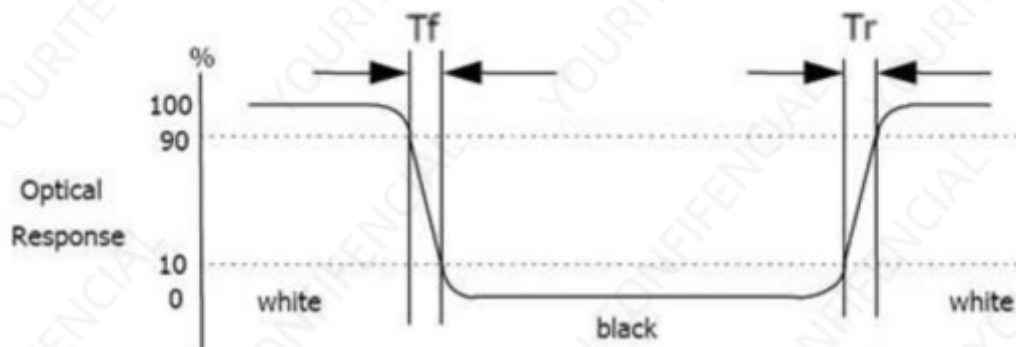
$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

Note 4.3: Transmittance is the Value with Polarizer.

Note 4.4: The color chromaticity coordinates specified in Table 5 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

Note 4.5: The electro-optical response time measurements shall be made as Figure 9 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is T_r , and 90% to 10% is T_f .

<Figure 7. Response Time Testing>



8. Reliability Test Item

No.	Test Item	Test Condition	Notes
1	High Temp. Storage	+80°C / 96H	1. Functional test isOK. Missing Segment,short, unclear segment non-display,display abnormally and liquid crystal leakare un-allowed. 2. No low temperature bubbles,end seal loose andfall, frame rainbow.
2	Low Temp. Storage	-30°C / 96H	
3	High Tempe. Operating	+70°C / 96H	
4	Low Tempe. Operating	-20°C / 96H	
5	High Temperature /Humidity storage	50°C x 90%RH /96H	
6	Thermal and cold shock	Static state, -20°C (30min) ~70°C (30min), 50 cycles	

9. Packing Method----TBD

- END -