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**MODEL NO : ET113BA02-T**

**MODEL VERSION: 01**

**SPEC VERSION : 1.0**

**ISSUED DATE: 2021-07-26**

**□Preliminary Specification**

**■Final Product Specification**

**Customer :**_____

| Approved by | Notes |
|---|---|
| | |

**Youri Confirmation**

| Prepared by | Reviewed by | Approved by |
|---|---|---|
| John | Johnny | Wang |

# 1. Introduction

## 1.1 Scope of application

LCD specification: Dots 440xRGBx1920.
As to basic specification of the driver IC, refer to the IC (SC7707) specification and data book.
All material & processing of the LCD module should be Lead Free.

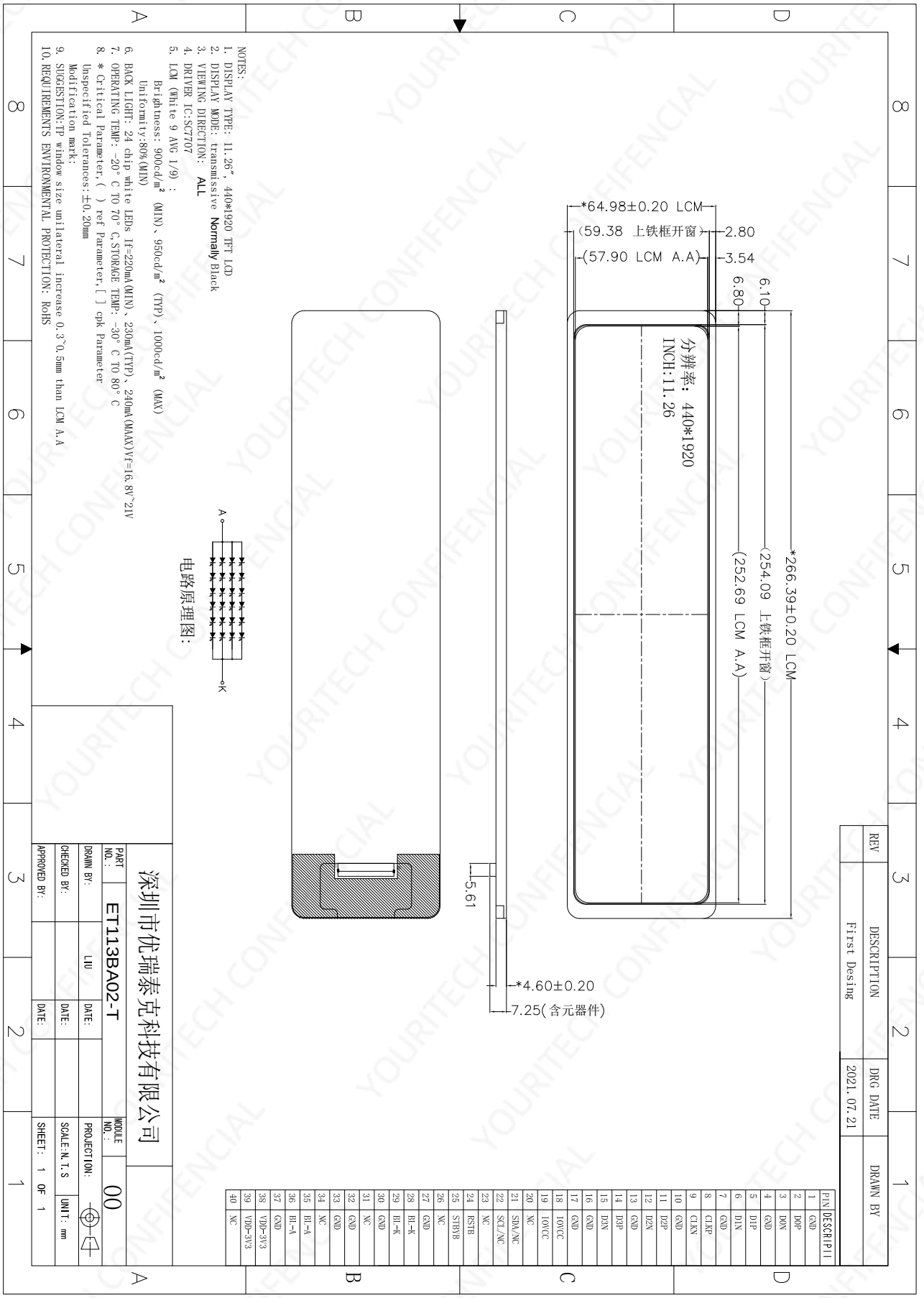
## 1.2 TFT features:

Structure: TFT PANNEL+IC +FPC+BL;
ALL O'CLOCK Type LCD
440 dot-segment and 1920 dot-common outputs;
16.7M Color can be selected by software;
White LED back light;
4lane MIPI interface

## 1.3 Applications:

## 2. LCM General specification

| ITEM | Sandard value | Unit |
|---|---|---|
| LCD Type | Normally Black | -- |
| Drive element | TFT active matrix | -- |
| Number of pixels | 440*3RGB(H)X1920(V) | Dots |
| Pixel arrangement | RGB stripe | -- |
| Pixel Pitch (W*H) | 0.1317(H) x0.1317 (V) | mm |
| Active area | 57.90(H) x 252.69V) | mm |
| Module Size(W*H*T) | 64.98(W) x266.39(H) x4.60(T) | mm |
| Viewing direction | ALL O'CLOCK | |
| TFT Driver IC | SC7707 | - |
| TFT interface | 4lane MIPI interface | - |
| Approx. Weight | TBD | g |
| Touch structure | -- | |
| Touch Driver IC | -- | - |
| Touch Interface | -- | |


*64.98±0.20 LCM
(59.38 上铁框开窗)
(57.90 LCM A.A)
2.80
3.54
6.10
6.80
*266.39±0.20 LCM
(254.09 上铁框开窗)
(252.69 LCM A.A)
分辨率：440*1920
INCH:11.26
5.61
*4.60±0.20
7.25(含元器件)
A
K
电路原理图：
NOTES:
1. DISPLAY TYPE: 11.26", 440*1920 TFT LCD
2. DISPLAY MODE: transmissive Normally Black
3. VIEWING DIRECTION: ALL
4. DRIVER IC:SC7707
5. LCM (White 9 AVG 1/9) :
Brightness: 900cd/m² (MIN)、950cd/m² (TYP)、1000cd/m² (MAX)
Uniformity:80%(MIN)
6. BACK LIGHT: 24 chip white LEDs If=220mA(MIN)、230mA(TYP)、240mA(MAAX)Vf=16.8V~21V
7. OPERATING TEMP: -20° C TO 70° C,STORAGE TEMP: -30° C TO 80° C
8. * Critical Parameter,( ) ref Parameter,[ ] cpk Parameter
Unspecified Tolerances:±0.20mm
Modification mark:
9. SUGGESTION:TP window size unilateral increase 0.3~0.5mm than LCM A.A
10. REQUIREMENTS ENVIRONMENTAL PROTECTION: RoHS
REV
DESCRIPTION
First Desing
DRG DATE
2021.07.21
DRAWN BY
PIN DESCRIPTION
1 GND
2 D0P
3 D0N
4 GND
5 D1P
6 D1N
7 GND
8 CLKP
9 CLKN
10 GND
11 D2P
12 D2N
13 GND
14 D3P
15 D3N
16 GND
17 GND
18 IOVCC
19 IOVCC
20 NC
21 SDA/NC
22 SCL/NC
23 NC
24 RSTB
25 STBYB
26 NC
27 GND
28 BL-K
29 BL-K
30 GND
31 NC
32 GND
33 GND
34 NC
35 BL-A
36 BL-A
37 GND
38 VDD=3V3
39 VDD=3V3
40 NC
深圳市优瑞泰克科技有限公司
PART NO.: ET113BA02-T
MODULE NO.: 00
DRAWN BY: LIU
DATE:
CHECKED BY:
DATE:
APPROVED BY:
DATE:
PROJECTION:
SCALE:N.T.S
UNIT: mm
SHEET: 1 OF 1

# 3.Absolute Maximum Rating

| Characteristics | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| LCM Operating Temperature | $T_{OPR}$ | -20 | +70 | °C |
| LCM Storage Temperature | $T_{STG}$ | -30 | +80 | °C |
| Humidity | RH | 10 | 90 | % |

# 4.Electrical Characteristics

## 4.1 TFT DC Characteristics

| Characteristics | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Supply Voltage for I/O | VDDIO | 3.0 | 3.3 | 3.3 | V |
| Supply Voltage for(DC/DC) | VDD | 3.0 | 3.3 | 3.6 | V |
| Supply Voltage for(VGH) | VGH | 10 | 12 | 14 | V |
| Supply Voltage for(VGL) | VGL | -14 | -12 | -10 | V |
| Supply Voltage for(AVDD) | AVDD | -- | -- | -- | V |
| Supply Voltage for(VCOM) | VCOM | -2.5 | TBD | 0 | V |

## 4.2 Back-Light Unit Characeristics

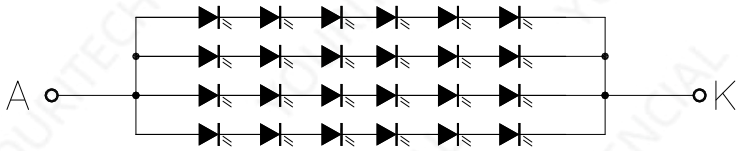
The back-light system is an edge-lighting type with 24 white LEDs. The characteristics of the back-light are shown in the following tables.

| Characteristics | Symbol | Min. | Type | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| Forward Voltage | $V_F$ | 16.8 | -- | 21 | V | - |
| Forward current | $I_F$ | 220 | 230 | 240 | mA | - |
| Luminance(With LCD) | Lv | 900 | 950 | 1000 | $cd/m^2$ | - |
| LED life time | N/A | -- | 10000 | -- | Hr | Note 1 |

Note:

(1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at $I_L$=30mA/LED. The LED life time could be decreased if operating $I_L$ is larger than 45mA/LED.

Backlight circuit diagram shown in below:




## 5. Module Function Description

| Pin No. | Symbol | Functional | Notes |
|---|---|---|---|
| 1 | GND | Ground | |
| 2 | NOP | MIPI data input | |
| 3 | DON | MIPI data input | |
| 4 | GND | Ground | |
| 5 | D1P | MIPI data input | |
| 6 | D1N | MIPI data input | |
| 7 | GND | Ground | |
| 8 | CLKP | MIPI data input | |
| 9 | CLKN | MIPI data input | |
| 10 | GND | Ground | |
| 11 | D2P | MIPI data input | |
| 12 | D2N | MIPI data input | |
| 13 | GND | Ground | |
| 14 | D3P | MIPI data input | |
| 15 | D3N | MIPI data input | |
| 16~17 | GND | Ground | |
| 18-19 | NC | Power supply(I/O) for digital circuits +3.3V input | |
| 20-23 | NC | No connection | |
| 24 | RSTB | Global reset pin | |
| 25 | STBYB | Standby mode, Normally pulled high | |
| 26 | NC | No connection | |
| 27 | GND | Ground | |
| 28-29 | BL-K | Back light-K | |
| 30 | GND | Ground | |
| 31 | NC | No connection | |
| 32-33 | GND | Ground | |
| 34 | NC | No connection | |
| 35-36 | BL-A | Back light-A | |
| 37 | GND | Ground | |
| 38-39 | VDD | Power supply for digital circuits +3.3V input | |
| 40 | NC | No connection | |

# 6. Timing Characteristics

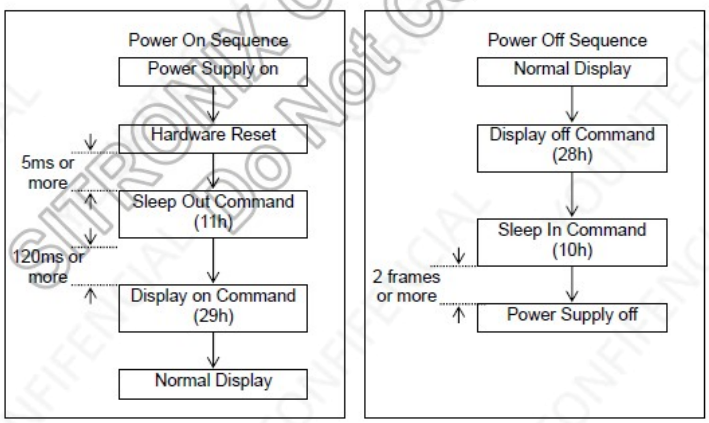
### Power on/off sequence

Power source IOVCC, VCI can be applied and powered down in any order. IOVCC, VCI can be powered down in any order.

During power off, if LCD is in the Sleep Out mode, IOVCC, VCI must be powered down minimum 120msec after NRESET has been released.

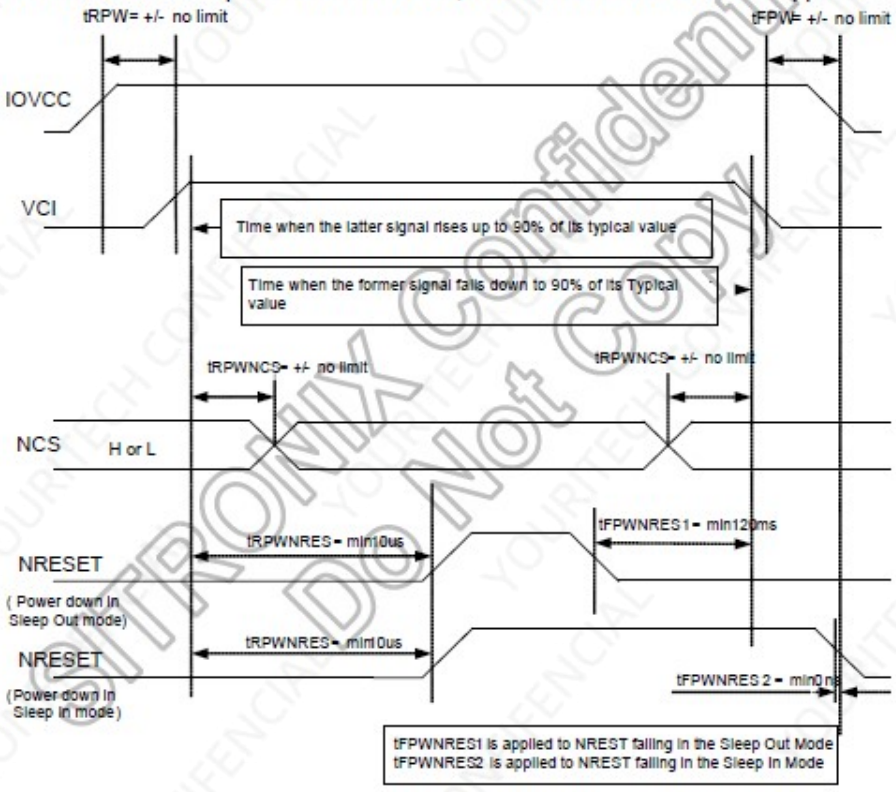
During power off, if LCD is in the Sleep In mode, IOVCC, VCI can be powered down minimum 0msec after NRESET has been released.

NCS can be applied at any timing or can be permanently grounded. NRESET has priority over NCS.




### RESX line is held low by host at power on

If RESX line is held low (and stable) by the host during power on, then the RESX must be held low for minimum 10µsec after both VDD1, VDD2 and VDD3 have been applied.




Note: Unless otherwise specified timings herein show cross point at 50% of signal/power level

## DSI Interface Timing Characteristics

### High Speed Mode

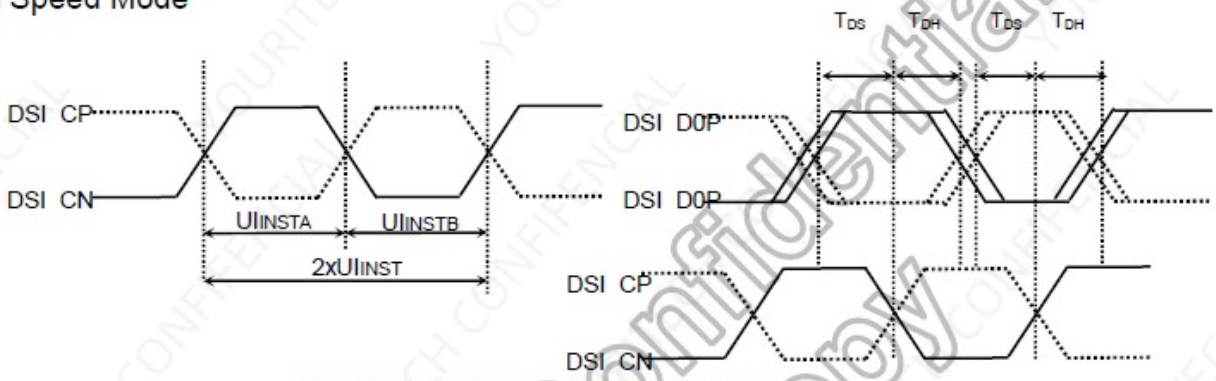



**Figure 7.4: DSI clock timing Characteristics**

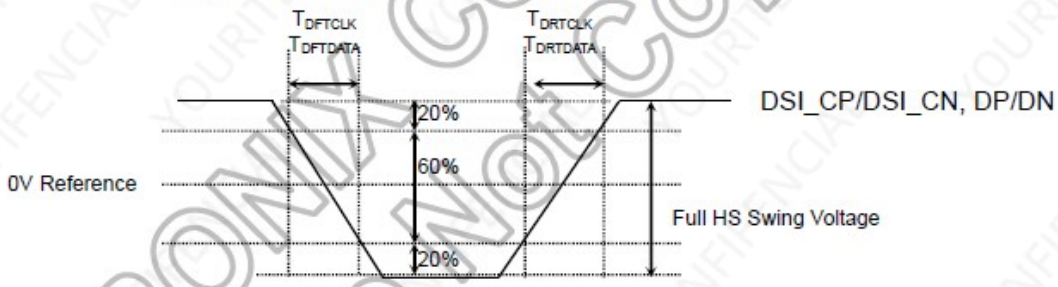



**Figure 7.5: Rising and falling time on clock and data channel**

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, $T_A$ = -30 to 70°C)

| Signal | Item | Symbol | Spec. | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| DSI_CP/ DSI_CN | Double UI instantaneous | $2xU_{INST}$ | TBD | - | 25 | ns |
| | UI instantaneous | $U_{INSTA}$ $U_{INSTB}$ | TBD | - | 12.5 | ns |
| DP/DN | Data to clock setup time | $T_{DS}$ | 0.15xUI | - | - | ps |
| | Data to clock hold time | $T_{DH}$ | 0.15xUI | - | - | ps |
| DSI_CP/ DSI_CN | Differential rise time for clock | $T_{DRTCLK}$ | 150 | - | 0.3UI | ps |
| | Differential fall time for clock | $T_{DFTCLK}$ | 150 | - | 0.3UI | ps |
| DP/DN | Differential rise time for data | $T_{DRTDATA}$ | 150 | - | 0.3UI | ps |
| | Differential fall time for data | $T_{DFTDATA}$ | 150 | - | 0.3UI | ps |

**Table 7.3: DSI High Speed Mode characteristics**

## Low Power Mode

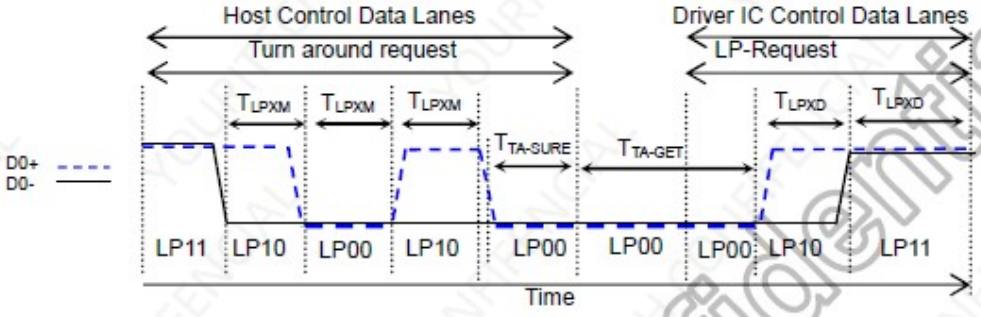



**Figure 7.6: BTA from HOST to Display module Timing**

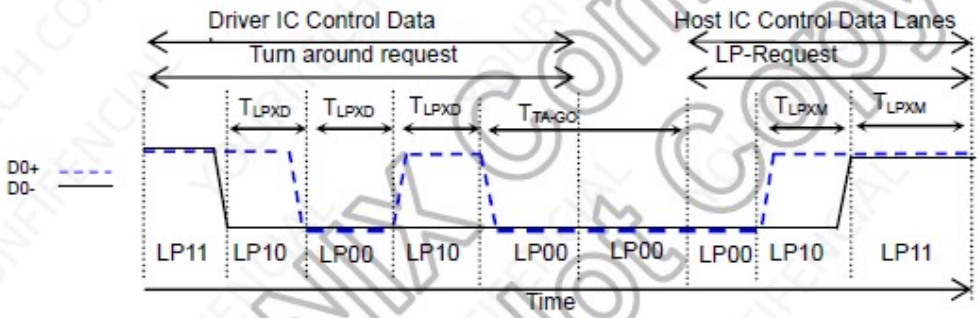


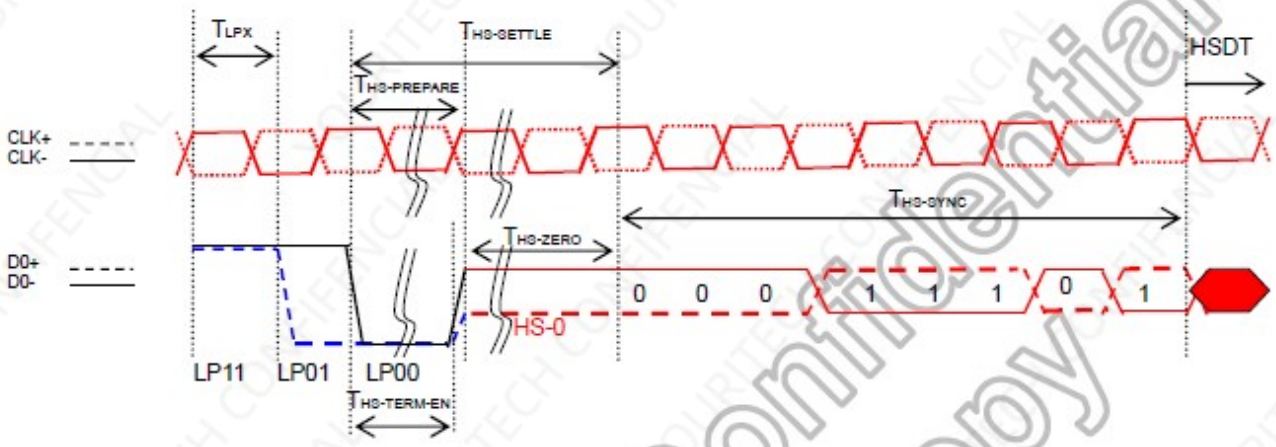

**Figure 7.7: BTA from Display module Timing to HOST**

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V, $T_A$ = -30 to 70°C)

| Signal | Item | Symbol | Spec. | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| DSI_D0P/ DSI_D0P | Length of LP-00/LP01/LP10/LP11 Host→ Display module | $T_{LPXM}$ | 50 | - | - | ns |
| | Length of LP-00/LP01/LP10/LP11 Display module →Host | $T_{LPXD}$ | 50 | - | - | ns |
| | Time-out before the MPU start driver | $T_{TA-SURE}$ | $T_{LPXD}$ | - | 2x$T_{LPXD}$ | ns |
| | Time to drive LP-00 by display module | $T_{TA-GET}$ | 5x$T_{LPXD}$ | - | - | ns |
| | Time to drive LP-00 after turnaround request Host | $T_{TAGO}$ | 4x$T_{LPXD}$ | - | - | ns |

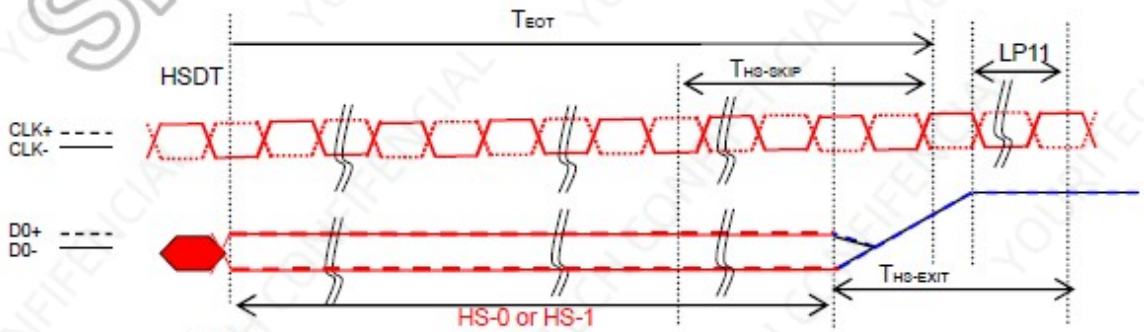
**Table 7.4: DSI Low Power Mode characteristics**

## DSI BURSTS




| Signal | Item | Symbol | Spec. | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| DSI_D0P/ DSI_D0P | Length of LP-00/LP01/LP10/LP11 | $T_{LPX}$ | 50 | - | - | ns |
| | Time to Driver LP-00 to prepare for HS transmission | $T_{HS-PREPARE}$ | 40+4UI | - | 85+6UI | ns |
| | Time to enable data receiver line termination | $T_{HS-TERM-EN}$ | - | - | 35+4xUI | ns |
| | Time to drive LP-00 by display module | $T_{TA-GET}$ | 5x$T_{LPXD}$ | - | - | ns |
| | Time to drive LP-00 after turnaround request Host | $T_{TAGO}$ | 4x$T_{LPXD}$ | - | - | ns |

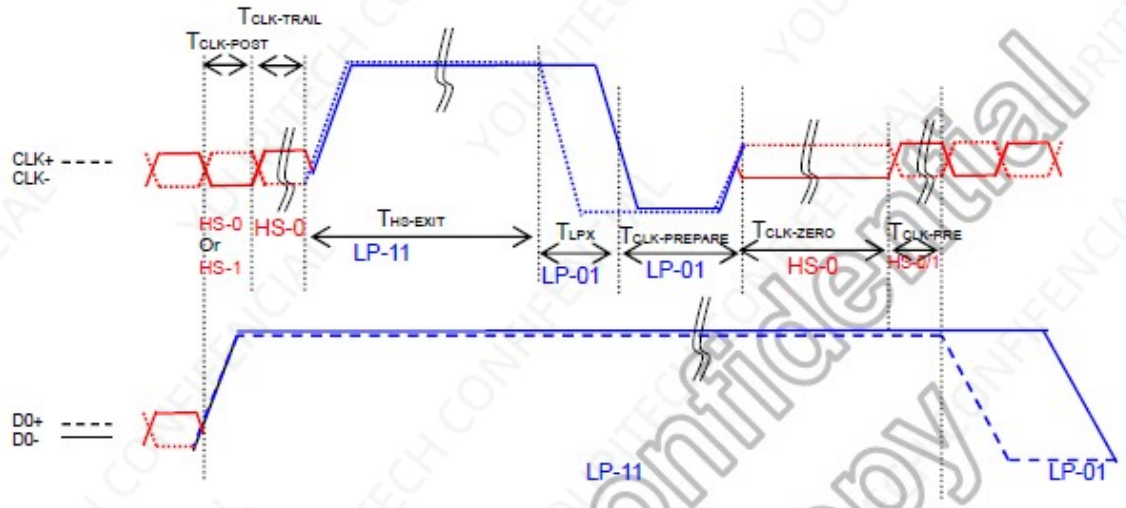
**Table 7.5: DSI Low Power Mode to High Speed Mode Timing**




NOTE:
If the last bit is HS-0, the transmitter changes from HS-0 to HS-1
If the last bit is HS-0, the transmitter changes from HS-1 to HS-0

| Signal | Item | Symbol | Spec. | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| DSI_D0P/ DSI_D0P | Time-Out at Display Module to Ignore Transition Period of EoT | $T_{HS-SKIP}$ | 40 | - | 55+4xUI | ns |
| | Time to Driver LP-11 after HS Burst | $T_{HS-EXIT}$ | 100 | - | - | ns |

**Table 7.6: DSI Low Power Mode to High Speed Mode Timing**




| Signal | Item | Symbol | Spec. | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| DSI_CP/ DSI_CN | Time that the MCU shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode | $T_{CLK-POST}$ | 60+52xUI | - | - | ns |
| | Time to drive HS differential state after last payload clock bit of a HS transmission burst | $T_{CLK-TRAIL}$ | 60 | - | - | ns |
| | Time to drive LP-11 after HS burst | $T_{HS-EXIT}$ | 100 | - | - | ns |
| | Time to drive LP-00 to prepare for HS transmission | $T_{CLK-PREPARE}$ | 38 | - | 95 | ns |
| | Time-out at Clock Lane Display Module to enable HS Termination | $T_{CLK-TERM-EN}$ | - | - | 38 | ns |
| | Minimum lead HS-0 drive period before starting Clock | $T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$ | 300 | - | - | ns |
| | Time that the HS clock shall be driven prior to any associated data Lane beginning the transition from LP to HS mode | $T_{CLK-PRE}$ | 8xUI | | | |

**Table 7.7: Clock Lanes High Speed Mode to/from Low Power Mode Timings**

## Reset input timing

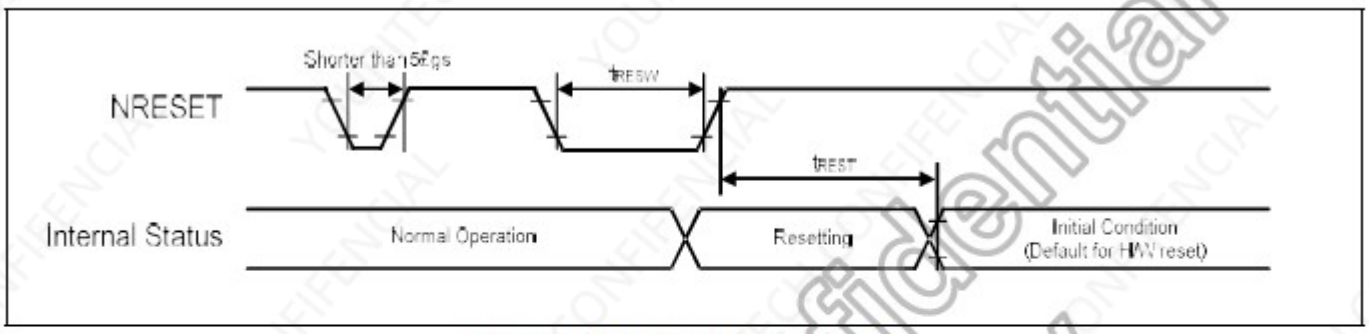



**Figure 7.8: Reset input timing**

| Symbol | Parameter | Related Pins | Spec. | | | Note | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| tRESW | Reset low pulse width(1) | NRESET | 10 | - | - | - | µs |
| tREST | Reset complete time(2) | - | 5 | - | - | When reset applied during SLPIN mode | ms |
| | | - | 120 | - | - | When reset applied during SLPOUT mode | ms |

**Table 7.8: Reset input timing**

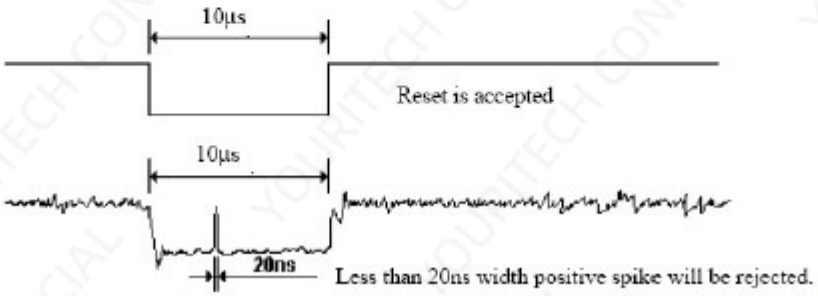
**Note:** (1) Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the following table.

| NRESET Pulse | Action |
|---|---|
| Shorter than 5 µs | Reset Rejected |
| Longer than 10 µs | Reset |
| Between 5 µs and 10 µs | Reset Start |

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which Maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

(3) During Reset Complete Time, ID and VCOM value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of NRESET.

(4) Spike Rejection also applies during a valid reset pulse as shown as below:



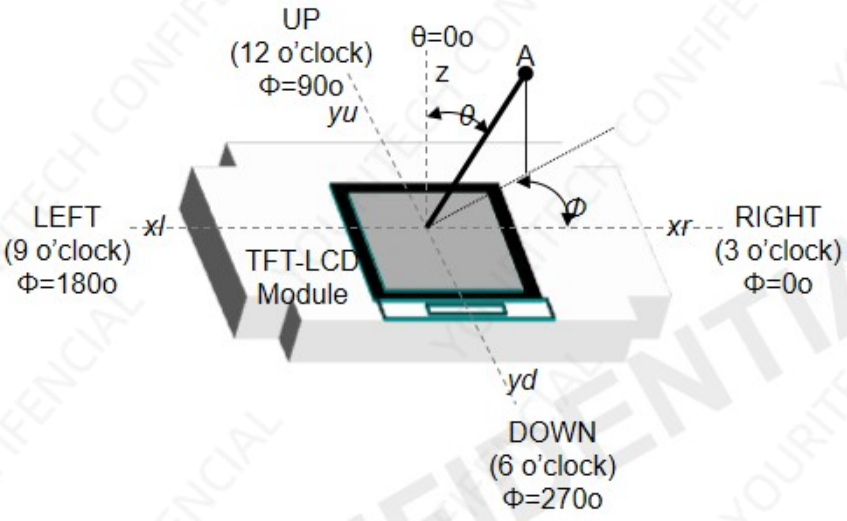

(5) It is necessary to wait 5msec after releasing NRESET before sending commands. Also Sleep Out command cannot be sent for 120msec.

## 7.Optical Characteristics

| Parameter | | Symbol | Condition | Min. | Typ. | Max. | Unit | Remark |
|---|---|---|---|---|---|---|---|---|
| Viewing Angle Range | Horizontal | $\Theta_3$ | CR > 10 | 80 | 85 | - | Deg. | Note 4.1 |
| | | $\Theta_9$ | | 80 | 85 | - | Deg. | |
| | Vertical | $\Theta_{12}$ | | 80 | 85 | - | Deg. | |
| | | $\Theta_6$ | | 80 | 85 | - | Deg. | |
| Contrast Ratio | | CR | Θ = 0° | 800 | 1000 | - | | APF Note 4.2/4.3 |
| Cell Transmittance | | Tr | | 4.7 | 5.65 | - | % | |
| Reproduction of color | | Rx | Θ = 0° | 0.629 | 0.659 | 0.689 | | CF@C Light Note 4.4 |
| | | Ry | | 0.288 | 0318 | 0.348 | | |
| | | Gx | | 0.233 | 0.263 | 0.293 | | |
| | | Gy | | 0.538 | 0.568 | 0.598 | | |
| | | Bx | | 0.107 | 0.137 | 0.167 | | |
| | | By | | 0.054 | 0.084 | 0.114 | | |
| | | Wx | | 0.275 | 0.305 | 0.335 | | |
| | | Wy | | 0.303 | 0.333 | 0.363 | | |
| Color Gamut | | | Θ = 0° | 65 | 70 | - | % | |
| Response Time | | Tr | Ta= 25° C Θ = 0° | - | **30** | **35** | ms | Note 4.5 |
| | | Tf | | - | | | ms | |
| | | Tgray | | - | - | - | ms | |

**Note 4.1:** Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see Figure 8).

**<Figure 6. Viewing Angle Range Is Defined As Follows>**



**Note 4.2:** Contrast measurements shall be made at viewing angle of Θ=0° and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. Luminance Contrast Ratio (CR) is defined mathematically.

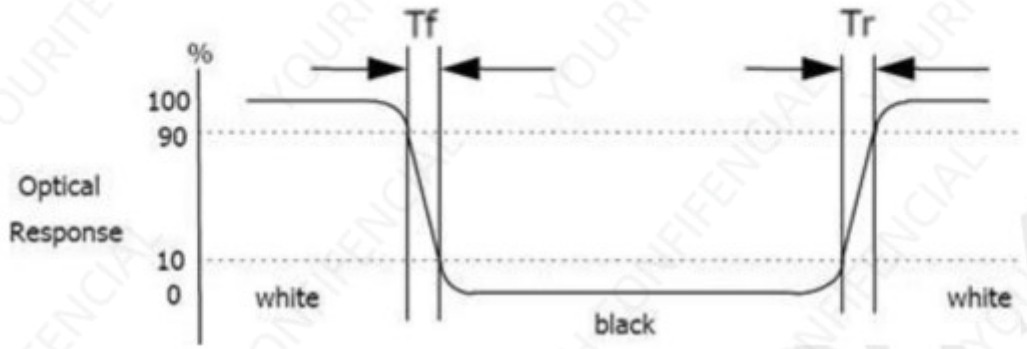
$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

**Note 4.3:** Transmittance is the Value with Polarizer.

**Note 4.4:** The color chromaticity coordinates specified in Table 5 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

**Note 4.5:** The electro-optical response time measurements shall be made as Figure 9 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Tf.

**<Figure 7. Response Time Testing>**



## 8. Reliability Test Item

| No. | Test Item | Test Condition | Notes |
|---|---|---|---|
| 1 | High Temp. Storage | +80°C / 96H | 1. Functional test isOK. Missing Segment,short, unclear segment non-display,display abnormally and liquid crystal leakare un-allowed.<br>2. No low temperature bubbles,end seal loose andfall, frame rainbow. |
| 2 | Low Temp. Storage | -30°C / 96H | |
| 3 | High Tempe. Operating | +70°C / 96H | |
| 4 | Low Tempe. Operating | -20°C / 96H | |
| 5 | High Temperature /Humidity storage | 50°C x 90%RH /96H | |
| 6 | Thermal and cold shock | Static state，-20℃（30min）~70℃（30min），50 cycles | |

## 9. Packing Method----TBD

- END -