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Project No. 项目编号	ET113BA06-T
Customer 客户名称	
Module No. 客户型号	
Product type 产品内容	**Standard LCD Module** **TFT：440*RGBx1920Dots** **10.11”TFT LCD**

客户确认Customer Approval	
项目负责人Project Manager	
品质主管Director of Quality	
采购工程师Purchasing Engineer	

PREPARED BY	CHECKED BY	APPROVED BY

1. Introduction

1.1 Scope of application

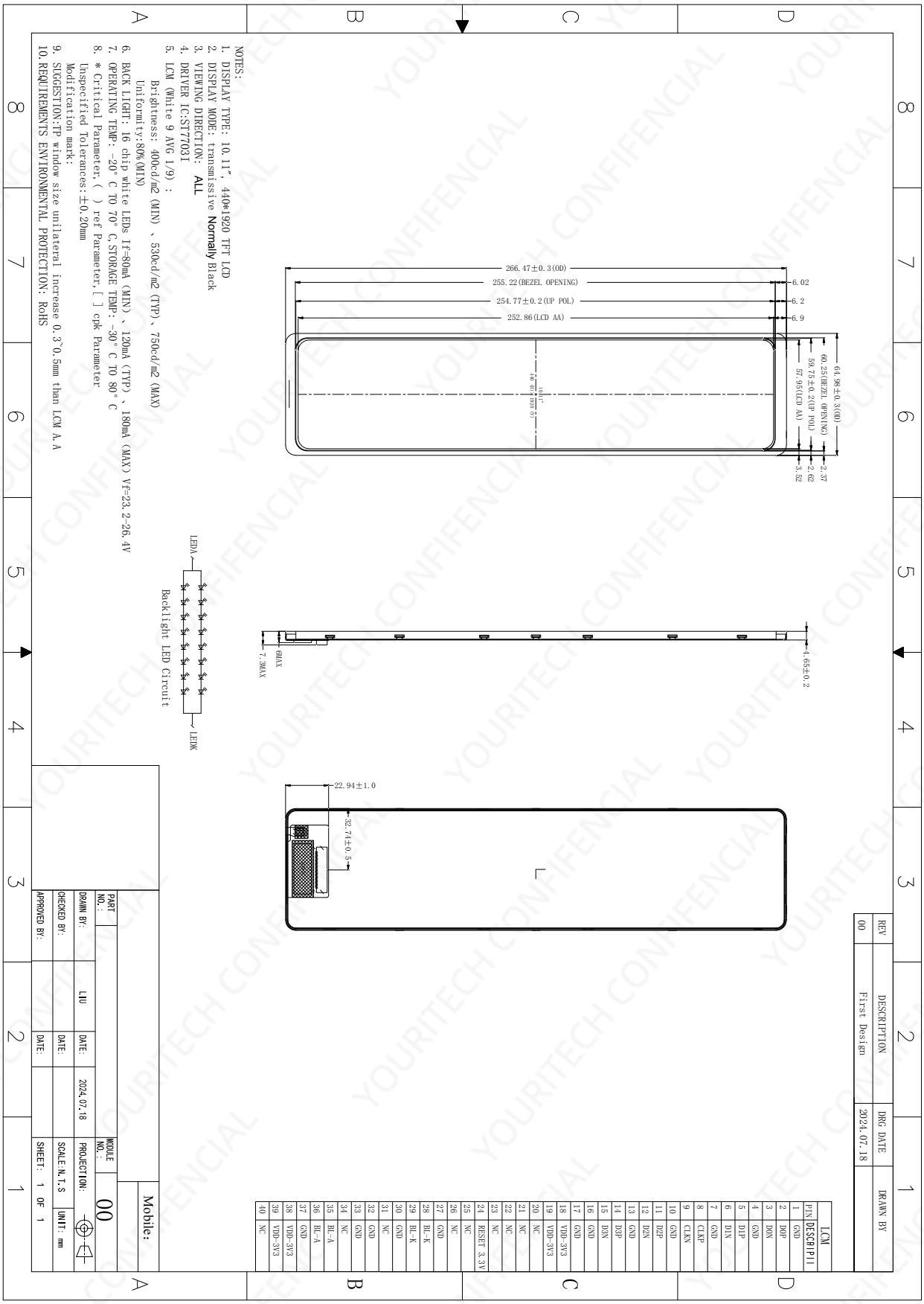
This specification applies to the LCD module that is supplied by YOURITECH Technology CO., LTD.
LCD specification: Dots 440xRGBx1920.
As to basic specification of the driver IC, refer to the IC (ST7703I) specification and data book.
All material & processing of the LCD module should be Lead Free.

1.2 TFT features:

Structure: TFT PANNEL+IC +FPC+BL;
IPS Type LCD
440dot-segment and 1920 dot-common outputs;
16.7M Color can be selected by software;
White LED back light;
4lane MIPI interface

2. LCM General specification

ITEM	Sandard value	Unit
LCD Type	Normally black	--
Drive element	TFT active matrix	--
Number of pixels	440*3RGB(H)X1920(V)	Dots
Pixel arrangement	RGB stripe	--
Pixel Pitch (W*H)	0.1317(W) × 0.1317 (H)	mm
Active area	57.95(W) × 252.86(H)	mm
Viewing direction	ALL O'CLOCK	--
TFT Driver IC	ST7703I	--
TFT interface	4lane MIPI interface	--
Approx. Weight	TBD	g
LCM Size(W*H*T)	64.98(W) ×266.47(H) ×4.65(T)	mm
Touch structure	--	--
Touch Driver IC	--	--
Touch Interface	--	--


NOTES:
1. DISPLAY TYPE: 10.11" 440*1920 TFT LCD
2. DISPLAY MODE: transmissive Normally Black
3. VIEWING DIRECTION: ALL
4. DRIVER IC:ST7703I
5. LCM (White 9 AVG 1/9) :
Brightness: 400cd/m2 (MIN) 、530cd/m2 (TYP)、750cd/m2 (MAX)
Uniformity:80%(MIN)
6. BACK LIGHT: 16 chip white LEDs If=80mA (MIN)、120mA (TYP)、180mA (MAX) Vf=23.2-26.4V
7. OPERATING TEMP: -20° C TO 70° C,STORAGE TEMP: -30° C TO 80° C
8. * Critical Parameter,( ) ref Parameter,[ ] cpk Parameter
Unspecified Tolerances:±0.20mm
Modification mark:
9. SUGGESTION:TP window size unilateral increase 0.3~0.5mm than LCM A.A
10.REQUIREMENTS ENVIRONMENTAL PROTECTION: RoHS
266.47±0.3(OD)
255.22(BEZEL OPENING)
254.77±0.2(UP POL)
252.86(LCD AA)
6.02
6.2
6.9
64.98±0.3(OD)
60.25(BEZEL OPENING)
59.75±0.2(UP POL)
57.95(LCD AA)
2.37
2.62
3.52
LEDA
LEDK
Backlight LED Circuit
6MAX
7.38MAX
4.65±0.2
22.94±1.0
32.74±0.5
L
LCM
PIN DESCRIPTION
1 GND
2 D0P
3 D0N
4 GND
5 D1P
6 D1N
7 GND
8 CLKP
9 CLKN
10 GND
11 D2P
12 D2N
13 GND
14 D3P
15 D3N
16 GND
17 GND
18 VDD-3V3
19 VDD-3V3
20 NC
21 NC
22 NC
23 NC
24 RESET 3.3V
25 NC
26 NC
27 GND
28 BL-K
29 BL-K
30 GND
31 NC
32 GND
33 GND
34 NC
35 BL-A
36 BL-A
37 GND
38 VDD-3V3
39 VDD-3V3
40 NC
REV
00
DESCRIPTION
First Design
DRG DATE
2024.07.18
DRAWN BY
Mobile:
PART NO.:
MODULE NO.:
00
DRAWN BY:
LIU
DATE:
2024.07.18
PROJECTION:
CHECKED BY:
DATE:
SCALE:N.T.S
UNIT: mm
APPROVED BY:
DATE:
SHEET: 1 OF 1

3.Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
LCM Operating Temperature	T_{OPR}	-20	+70	°C
LCM Storage Temperature	T_{STG}	-30	+80	°C
Humidity	RH	--	90	%

4.Electrical Characteristics

4.1 TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage for(DC/DC)	VDD	2.8	3.3	3.3	V

4.2 Back-Light Unit Characeristics

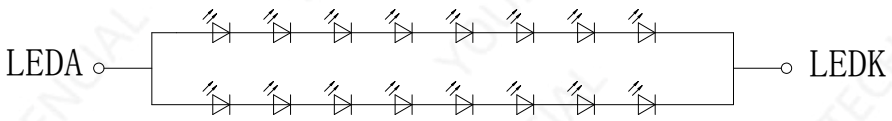
The back-light system is an edge-lighting type with 16 white LEDs. The characteristics of the back-light are shown in the following tables.

Characteristics	Symbol	Min.	Type	Max.	Unit	Notes
Forward Voltage	V_F	23.2	--	26.4	V	--
Forward current	I_F	80	120	180	mA	--
Luminance(With LCD)	Lv	400	530	750	cd/m^2	--
LED life time	N/A	--	20,000	--	Hr	Note 1

Note:

(1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=40mA/LED. The LED life time could be decreased if operating I_L is larger than 45mA/LED.

Backlight circuit diagram shown in below:



5. Module Function Description

Pin No.	Symbol	LCM Description
1	GND	Power Ground
2	D0P	Positive polarity of low voltage differential data 0 signal
3	D0N	Negative polarity of low voltage differential data 0 signal
4	GND	Power Ground
5	D1P	Positive polarity of low voltage differential data 1 signal
6	D1N	Negative polarity of low voltage differential data 1 signal
7	GND	Power Ground
8	CLKP	Positive polarity of low voltage differential clock signal
9	CLKN	Negative polarity of low voltage differential clock signal
10	GND	Power Ground
11	D2P	Positive polarity of low voltage differential data 2 signal
12	D2N	Negative polarity of low voltage differential data 2 signal
13	GND	Power Ground
14	D3P	Positive polarity of low voltage differential data 3 signal
15	D3N	Negative polarity of low voltage differential data 3 signal
16	GND	Power Ground
17	GND	Power Ground
18	VDD 3.3V	Power Supply For LCD.
19	VDD 3.3V	Power Supply For LCD.
20	NC	No Connection.
21	NC	No Connection.
22	NC	No Connection.
23	NC	No Connection.
24	RESET 3.3V	Reset signal input terminal. Active at ‘L’.
25	NC	No Connection.
26	NC	No Connection.
27	GND	Power Ground
28	LEDK	Power supply for backlight cathode input terminal.
29	LEDK	Power supply for backlight cathode input terminal.
30	GND	Power Ground
31	NC	No Connection.
32	GND	Power Ground
33	GND	Power Ground
34	NC	No Connection.
35	LEDA	Power supply for backlight anode input terminal.
36	LEDA	Power supply for backlight anode input terminal.
37	GND	Power Ground
38	VDD 3.3V	Power Supply For LCD.
39	VDD 3.3V	Power Supply For LCD.
40	NC	No Connection.

6. Timing Characteristics

Power on/off Sequence

Power source IOVCC, VCI can be applied and powered down in any order. IOVCC, VCI can be powered down in any order.

During power off, if LCD is in the Sleep Out mode, IOVCC, VCI must be powered down minimum 120msec after NRESET has been released.

During power off, if LCD is in the Sleep In mode, IOVCC, VCI can be powered down minimum 0msec after NRESET has been released.

NCS can be applied at any timing or can be permanently grounded. NRESET has priority over NCS.

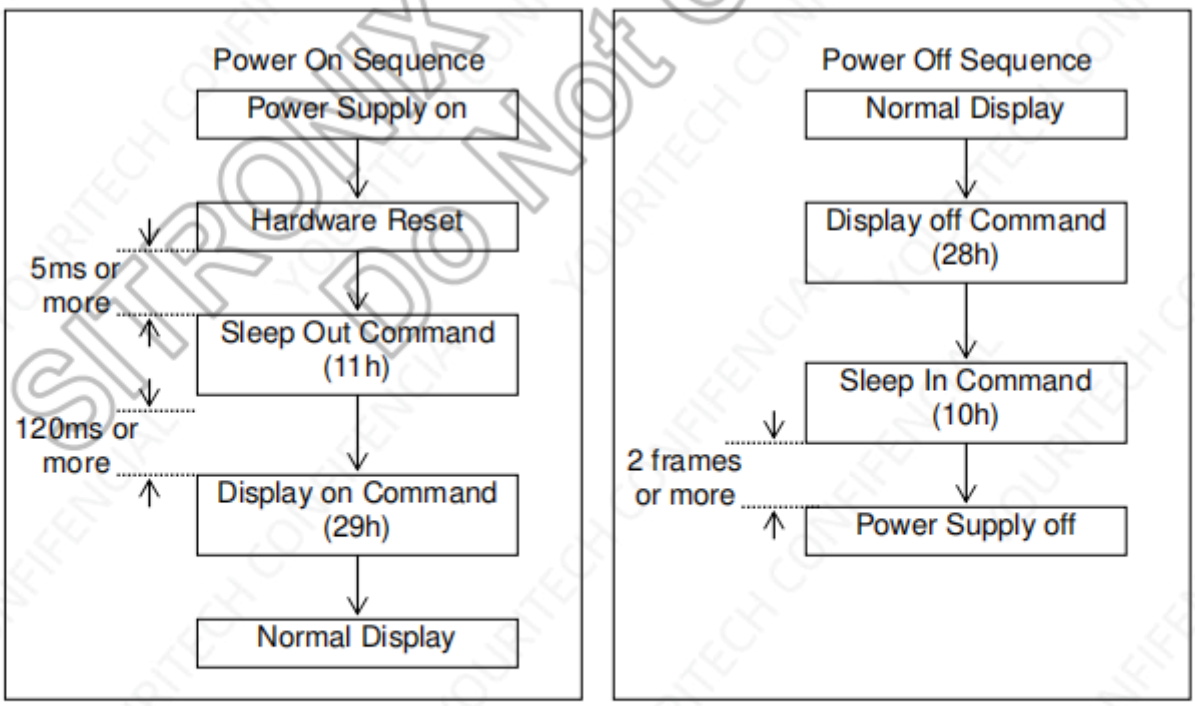


Figure 5.32: The power supply ON/OFF setting for Display ON/OFF and Sleep In/out

Case 1: RESX line is held high or unstable by host at power on

If RESX line is held high or unstable by the host during power on, then a Hardware Reset must be applied after both VDD1, VDD2 and VDD3 have been applied- otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.

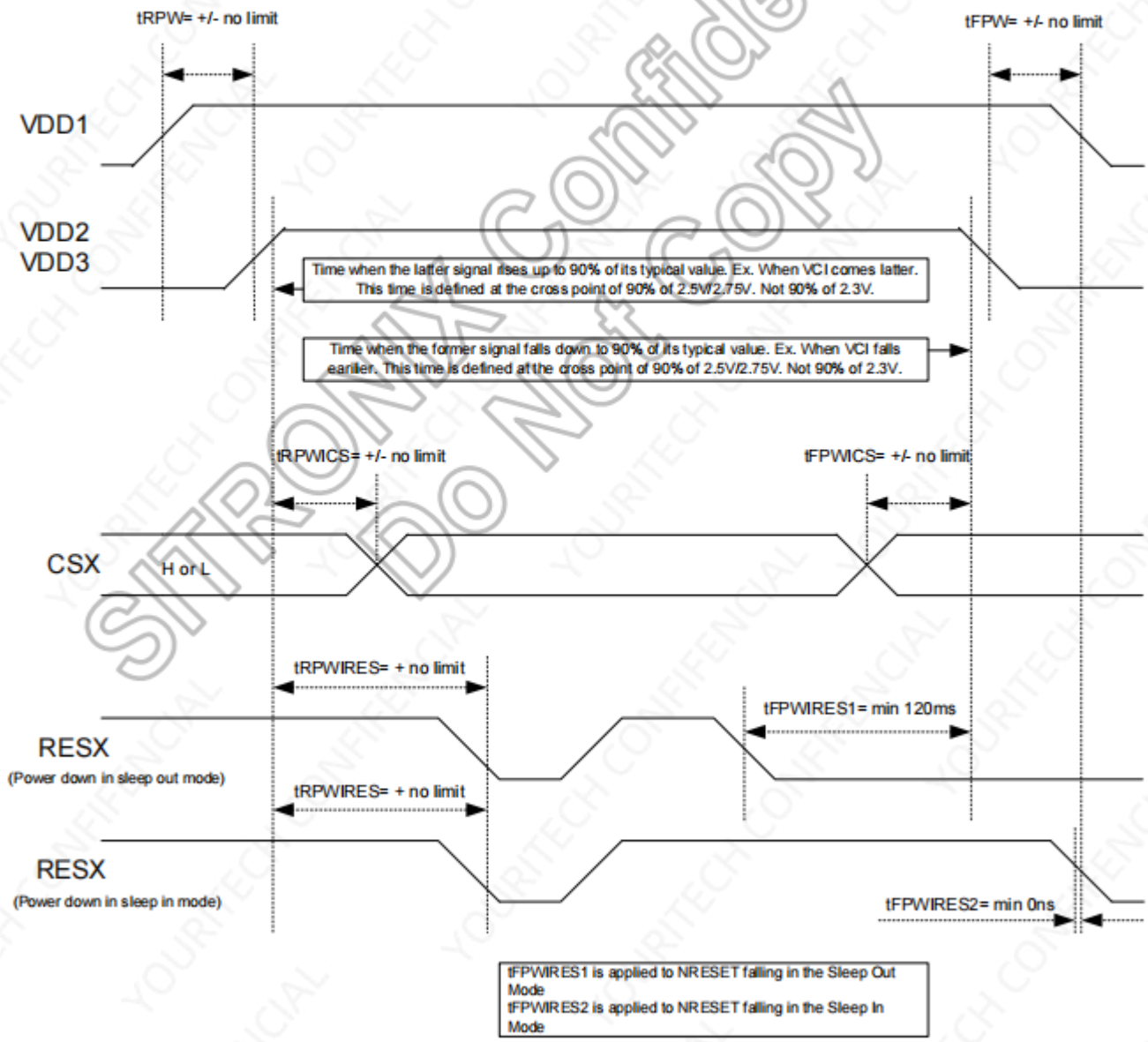
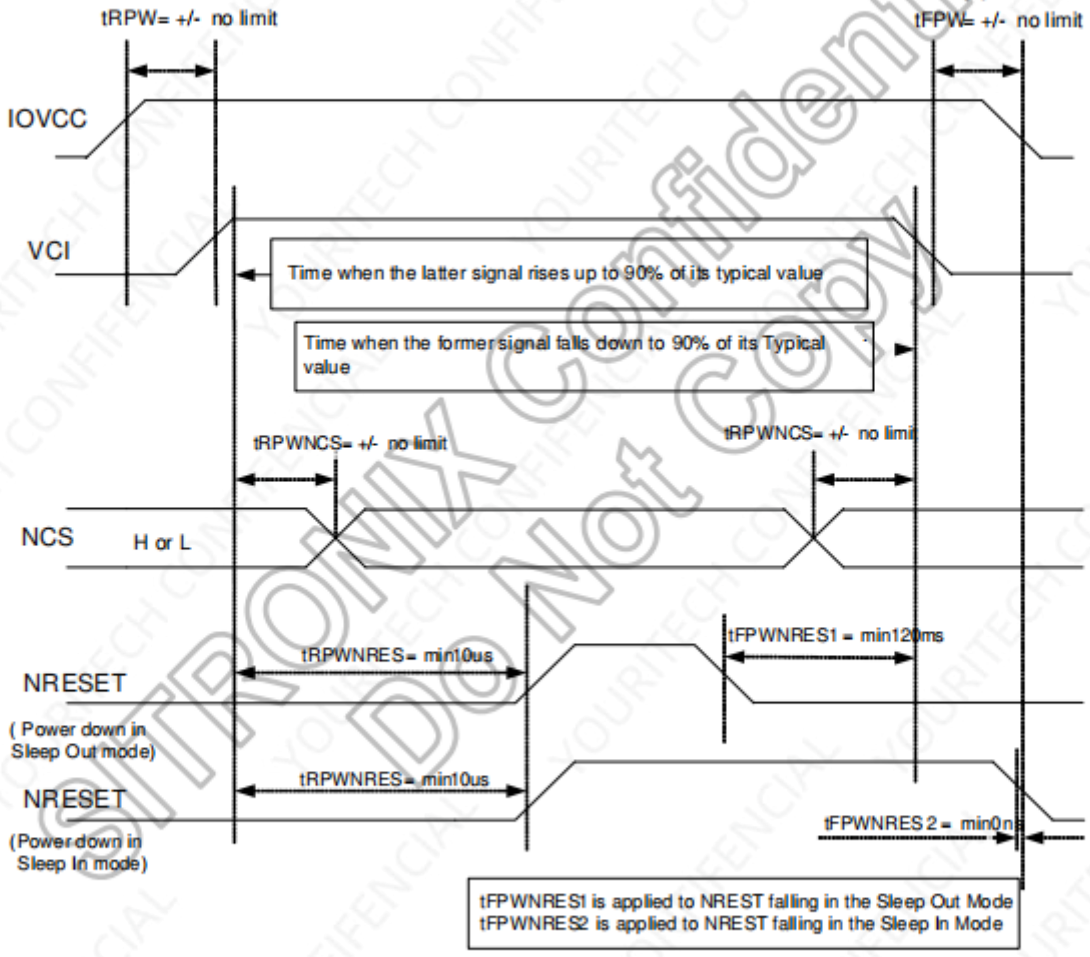


Figure 5.33: Case 1: RESX line is held high or unstable by host at power on

Case 2: RESX line is held low by host at power on

If RESX line is held low (and stable) by the host during power on, then the RESX must be held low for minimum 10µsec after both VDD1, VDD2 and VDD3 have been applied.



Note: Unless otherwise specified timings herein show cross point at 50% of signal/power level

Figure 5.34: Case 2: RESX line is held low by host at power on

DSI-MIPI Interface Timing Characteristics

High Speed Mode

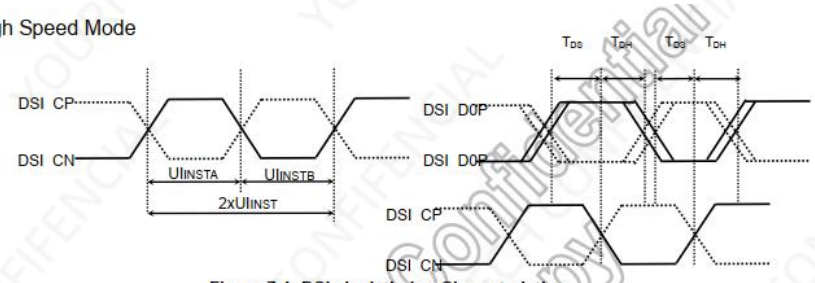


Figure 7.4: DSI clock timing Characteristics

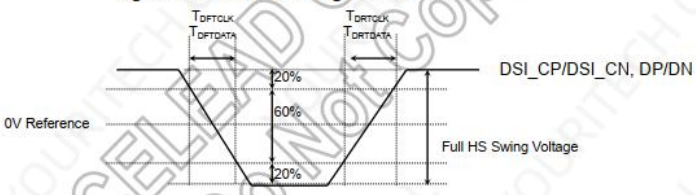


Figure 7.5: Rising and falling time on clock and data channel

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V,T_A = -30 to 70°C)

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Double UI instantaneous	2xUINST	TBD	-	25	ns
	UI instantaneous	UINSTA UINSTB	TBD	-	12.5	ns
DP/DN	Data to clock setup time	TDS	0.15xUI	-	-	ps
	Data to clock hold time	TDH	0.15xUI	-	-	ps
DSI_CP/ DSI_CN	Differential rise time for clock	TDRTCLK	150	-	0.3UI	ps
	Differential fall time for clock	TDFTCLK	150	-	0.3UI	ps
DP/DN	Differential rise time for data	TDRTDATA	150	-	0.3UI	ps
	Differential fall time for data	TDFTDATA	150	-	0.3UI	ps

Table 7.3: DSI High Speed Mode Characteristics

Low Power Mode

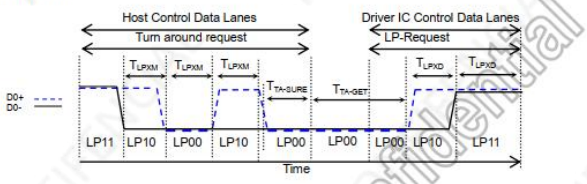


Figure 7.6: BTA from HOST to Display Module Timing

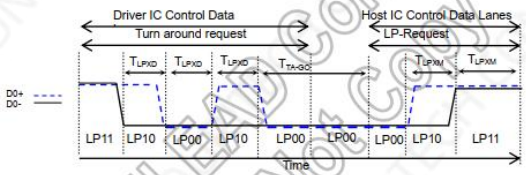


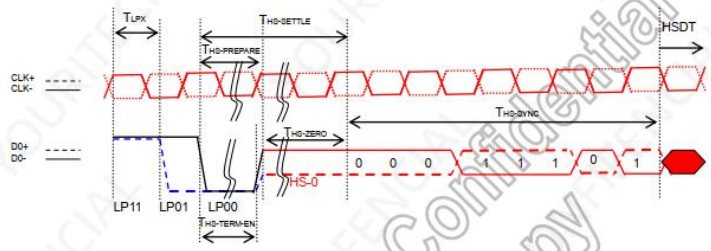
Figure 7.7: BTA from Display Module Timing to HOST

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V,T_A = -30 to 70°C)

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11 Host→ Display module	TLPXM	50	-	-	ns
	Length of LP-00/LP01/LP10/LP11 Display module →Host	TLPXD	50	-	-	ns
	Time-out before the MPU start driver	TTA-SURE	TLPXD	-	2xTLPXD	ns
	Time to drive LP-00 by display module	TTA-GET	5xTLPXD	-	-	ns
	Time to drive LP-00 after turnaround request Host	TTAGO	4xTLPXD	-	-	ns

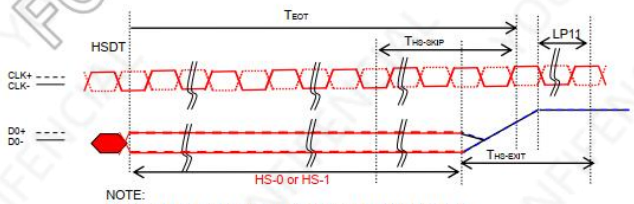
Table 7.4: DSI Low Power Mode Characteristics

DSI BURSTS



Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11	T_{LPX}	50	-	-	ns
	Time to Driver LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI	-	85+6UI	ns
	Time to enable data receiver line termination	$T_{HS-TERM-EN}$	-	-	35+4xUI	ns
	Time to drive LP-00 by display module	T_{TA-GET}	5xT_{LPXD}	-	-	ns
	Time to drive LP-00 after turnaround request Host	T_{TAGO}	4xT_{LPXD}	-	-	ns

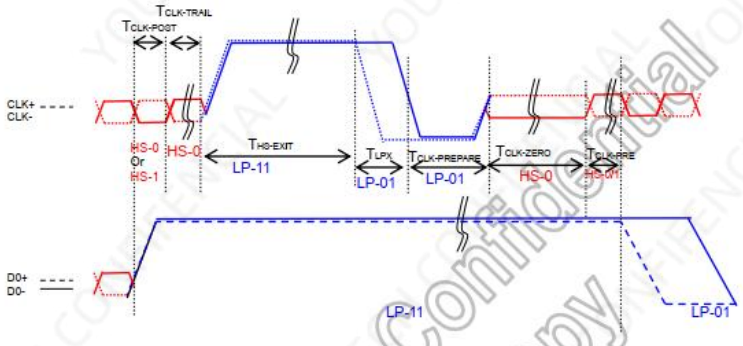
Table 7.5: DSI Low Power Mode to High Speed Mode Timing



NOTE:
If the last bit is HS-0, the transmitter changes from HS-0 to HS-1
If the last bit is HS-0, the transmitter changes from HS-1 to HS-0

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Time-Out at Display Module to Ignore Transition Period of EoT	$T_{HS-SKIP}$	40	-	55+4xUI	ns
	Time to Driver LP-11 after HS Burst	$T_{HS-EXIT}$	100	-	-	ns

Table 7.6: DSI Low Power Mode to High Speed Mode Timing



Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Time that the MCU shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$	60+52xUI	-	-	ns
	Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK-TRAIL}$	60	-	-	ns
	Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100	-	-	ns
	Time to drive LP-00 to prepare for HS transmission	$T_{CLK-PREPARE}$	38	-	95	ns
	Time-out at Clock Lane Display Module to enable HS Termination	$T_{CLK-TERM-EN}$	-	-	38	ns
	Minimum lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	300	-	-	ns
	Time that the HS clock shall be driven prior to any associated data Lane beginning the transition from LP to HS mode	$T_{CLK-PRE}$	8xUI			

Table 7.7: Clock Lanes High Speed Mode to/from Low Power Mode Timing

Reset Description:

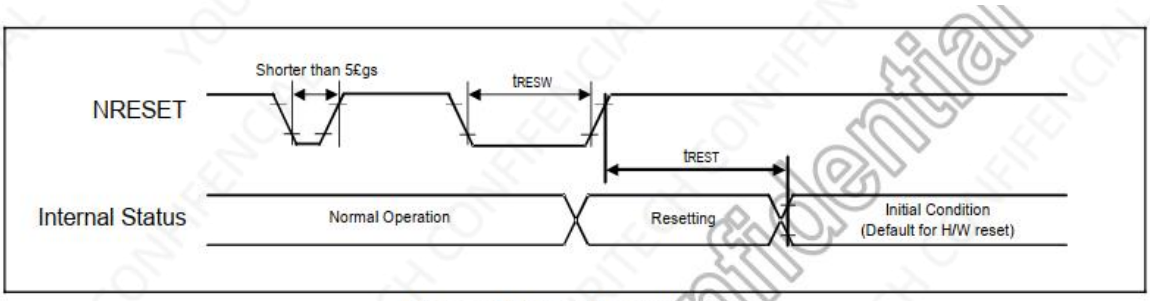


Figure 7.8: Reset input timing

Symbol	Parameter	Related Pins	Spec.			Note	Unit
			Min.	Typ.	Max.		
tRESW	Reset low pulse width(1)	NRESET	10	-	-	-	µs
tREST	Reset complete time(2)	-	15	-	-	When reset applied during SLPIN mode	ms
		-	120	-	-	When reset applied during SLPOUT mode	ms

Table 7.8: Reset Input Timing

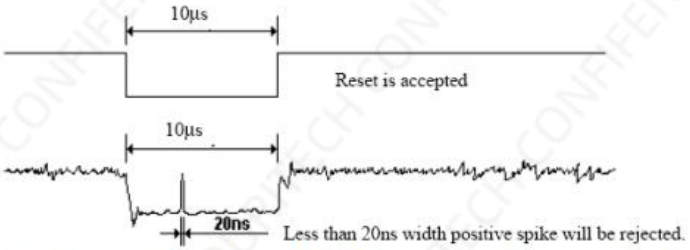
Note: (1) Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the following table.

NRESET Pulse	Action
Shorter than 5 µs	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which Maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

(3) During Reset Complete Time, ID and VCOM value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 15ms after a rising edge of NRESET.

(4) Spike Rejection also applies during a valid reset pulse as shown as below:



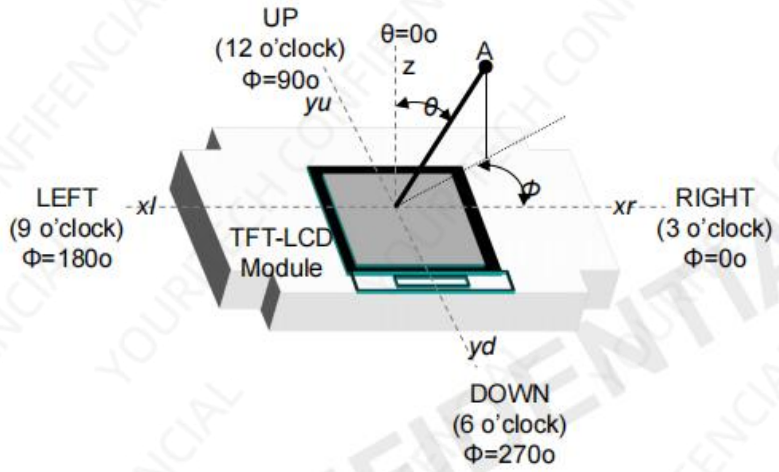
(5) It is necessary to wait 15msec after releasing NRESET before sending commands. Also Sleep Out command cannot be sent for 120msec.

7.Optical Characteristics

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle Range	Horizontal	Θ_3	CR > 10	80	85	-	Deg.	Note 4.1
		Θ_9		80	85	-	Deg.	
	Vertical	Θ_{12}		80	85	-	Deg.	
		Θ_6		80	85	-	Deg.	
Contrast Ratio		CR	Θ = 0°	800	1000	-		APF Note 4.2/4.3
Cell Transmittance		Tr		4.7	5.65	-	%	
Reproduction of color		Rx	Θ = 0°				-	CF@C Light Note 4.4
		Ry					-	
		Gx					-	
		Gy					-	
		Bx					-	
		By					-	
		Wx		0.274	0.304	0.334	-	
		Wy		0.302	0.332	0.362	-	
Color Gamut			Θ = 0°	65	70	-	%	
Response Time		Tr	Ta= 25° C Θ = 0°	-	**30**	**35**	ms	Note 4.5
		Tf		-			ms	

Note 1: Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see Figure 6).

<Figure 6. Viewing Angle Range Is Defined As Follows>



Note 2: Contrast measurements shall be made at viewing angle of Θ=0° and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. Luminance Contrast Ratio (CR) is defined mathematically.

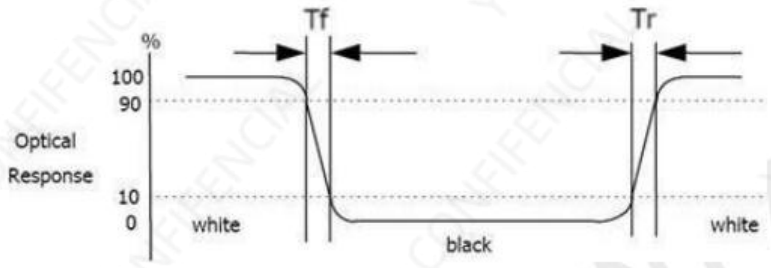
$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

Note 3: Transmittance is the Value with Polarizer.

Note 4: The color chromaticity coordinates specified in Table 5 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

Note 5: The electro-optical response time measurements shall be made as Figure 7 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Tf.

<Figure 7. Response Time Testing>



8. Reliability Test Item

No.	Test Item	Test Condition	Notes
1	High Temp. Storage	+80°C / 96H	1. Functional test isOK. Missing Segment,short, unclear segment non-display,display abnormally and liquid crystal leakare un-allowed. 2. No low temperature bubbles,end seal loose andfall, frame rainbow.
2	Low Temp. Storage	-30°C / 96H	
3	High Tempe. Operating	+70°C / 96H	
4	Low Tempe. Operating	-20°C / 96H	
5	High Temperature /Humidity storage	60°C x 90%RH / 96H	
6	Thermal and cold shock	Static state， -20℃（30min） ~70℃（30min），10 cycles	

9. Packing Method----TBD

- END -