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Product Specifications

Customer	Standard
Description	ePaper Display Signage
Model Name	ET116EP01-J
Date	2025/09/26
Revision	1.0

	Design Engineering		
	Approval	Check	Design

Content

1. Overview

ET116EP01-J is a reflective electrophoretic technology display module on an active matrix TFT substrate. The panel is capable of displaying black, white, yellow, and red images depending on the associated lookup table used. The circuitry on the panel includes an integrated gate and source driver, timing controller, oscillator, DC-DC boost circuit, and memory to store the frame buffer and lookup tables, and additional circuitry to control VCOM and BORDER settings.

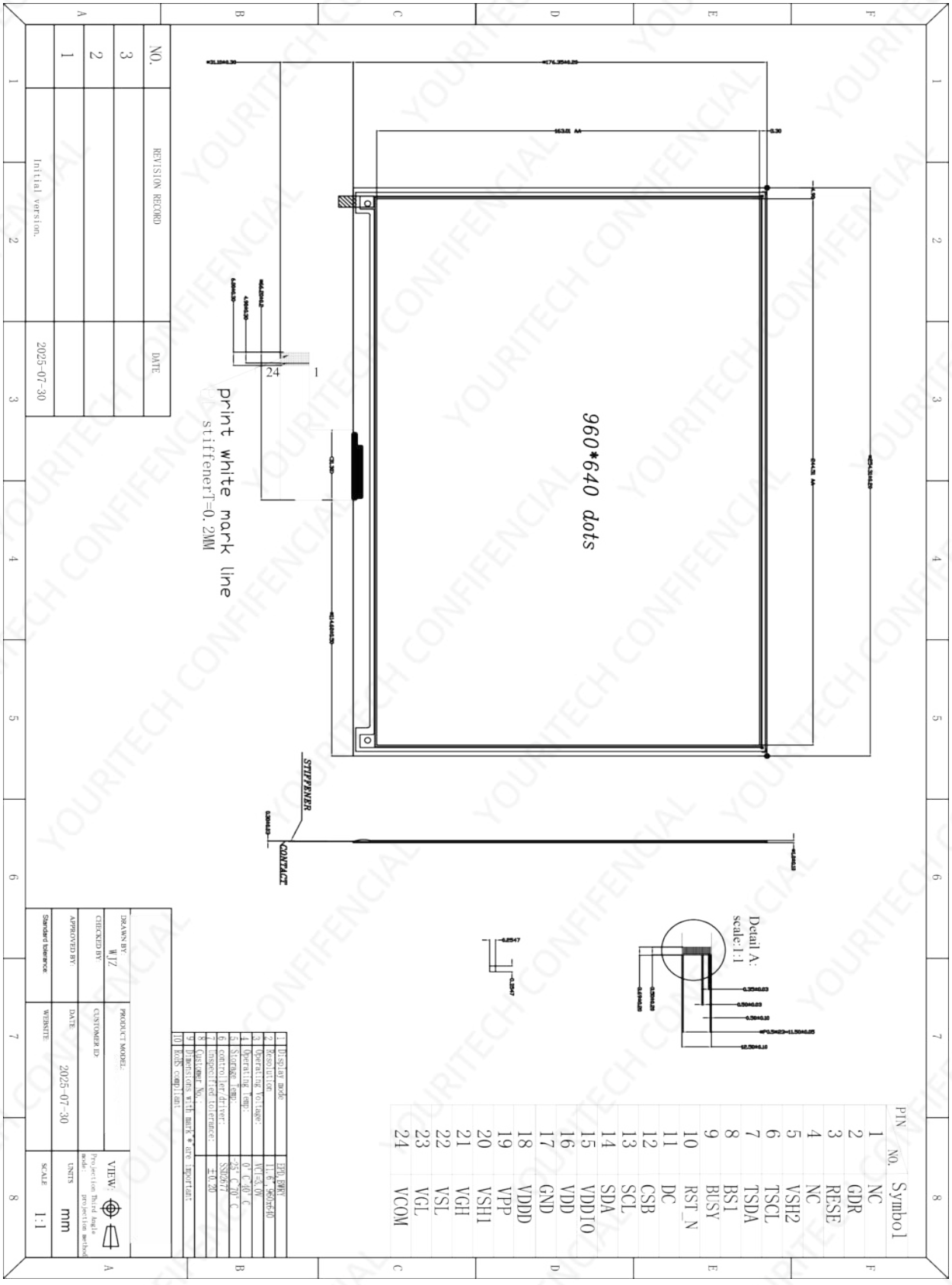
2. Features

- Highlight Red and Yellow color
- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Antiglare hard-coated front-surface
- Low current deep sleep mode
- On chip display RAM
- Waveform stored in On-chip OTP
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I²C signal master interface to read external temperature sensor
- Available in COG package

3. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	11.6	Inch	
Display Resolution	960(H)×640(V)	Pixel	Dpi:99
Active Area	244.51×163.01	mm	
Pixel Pitch	0. 2547×0.2547	mm	
Pixel Configuration	Rectangle		
Outline Dimension	254.31(H)×176.35(V) ×1.0(D)	mm	
Weight	82.9±0.5	g	

4. Mechanical Drawing of EPD module



5. Input/Output Pin Assignment

5.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	Keep Open
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC		Do not connect with other NC pins	Keep Open
5	VSH2	C	Positive Source driving voltage	
6	TSCL	O	This pin is I^2C Interface to digital temperature sensor Clock pin. External pull up resistor is required when connecting to I^2C slave. When not in use: VSS	
7	TSDA	I/O	This pin is I^2C Interface to digital temperature sensor Data pin. External pull up resistor is required when connecting to I^2C slave. When not in use: VSS	
8	BS1	I	Interface Selection Pin	
9	BUSY	O	This pin indicates the driver status.	
10	RST_N	I	This pin is reset signal input.Active Low.	
11	DC	I	This pin is Data/Command control pin connecting to the MCU	
12	CSB	I	This pin is the chip select input connecting to the MCU.	
13	SCL	I	Serial clock pin for interface	
14	SDA	I/O	Serial data pin for interface	
15	VDDIO	P	Power for interface logic pins	
16	VDD	P	Power Supply for the chip	
17	GND	P	Ground	
18	VDDD	C	Core logic power pin	
19	VPP	P	Reserved	
20	VSH1	C	Positive Source driving voltage	
21	VGH	C	Positive Gate driving voltage	
22	VSL	C	Negative Source driving voltage	
23	VGL	C	Negative Gate driving voltage	
24	VCOM	C	VCOM driving voltage	

Key: I = Input, O =Output, I/O = Bi-directional (input/output), P = Power pin, C = Capacitor PinNC = Not Connected, Pull L =connect to GND, Pull H = connect to VDDIO

6. Electrical Characteristics

6.1 Absolute Maximum Rating

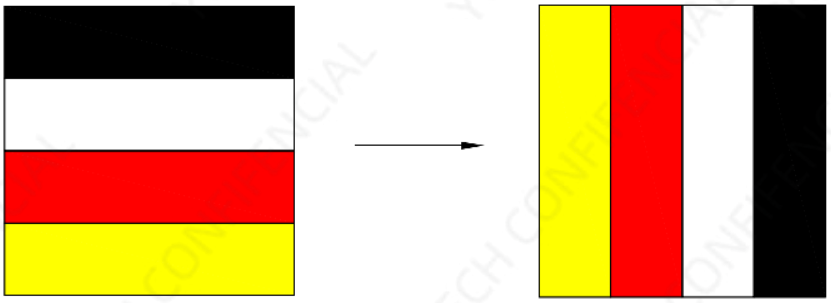
Parameter	Symbol	Rating	Unit
Logic supply voltage	VDD	-0.5 to +4.0	V
Logic Input voltage	VIN	-0.5 to V_{DDIO} +0.5	V
Logic Output voltage	VOUT	-0.5 to V_{DDIO} +0.5	V
Operating Temp range	TOPR	0 to +40	°C
Storage Temp range	TSTG	-25 to +70	°C
Optimal Storage Temp	TSTGo	23±2	°C
Optimal Storage Humidity	HSTGo	55±10	%RH

Note: Maximum ratings are the limits beyond which damage to the device may occur. Functional operation should be restricted to the conditions specified in the Electrical Characteristics tables or the Pin Description section.

6.2 Panel DC Characteristics

Parameter	Symbol	Conditions	Applicable pin	Min.	Typ.	Max	Units
Single ground	V_{SS}	-		-	0	-	V
VDD supply operation voltage	V_{DD}	-	VDD	2.3	3.0	3.6	V
High level input voltage	V_{IH}	-	-	0.8 V_{DDIO}	-	-	V
Low level input voltage	V_{IL}	-	-	-	-	0.2 V_{DDIO}	V
High level output voltage	V_{OH}	IOH = -100uA	-	0.8V_{DDIO}	-	-	V
Low level output voltage	V_{OL}	IOL = 100uA	-	-	-	0.2V_{DDIO}	V
Typical power	P_{TYP}	V_{DD} =3.0V	-	-	135	-	mW
Deep sleep mode	P_{STPY}	V_{DD} =3.0V	-	-	0.003	-	mW
Typical operating current	Iopr_V_{DD}	V_{DD} =3.0V	-	-	45	-	mA
Image update time	-	25 ºC	-	-	26	-	sec
Sleep mode current	Islp_V_{DD}	DC/DC off No clock No input load Ram data retain	-	-	20	35	uA
Deep sleep mode current	Idslp_V_{DD}	DC/DC off No clock No input load Ram data not retain	-	-	1	-	uA

Notes:1. Typical power is measured under a transition from a horizontal 4-scale pattern to a vertical 4-scale pattern.



2. Deep sleep power is defined as the power consumed when the panel controller operates in deep sleep mode.

3. All specified electrical and optical characteristics are guaranteed exclusively with the controller and waveform provided by YOURITECH.

4. Electrical measurements are to be performed using a multimeter.

6.3 Panel AC Characteristics

6.3.1 MCU Interface selection

The IC can support 3-wire/4-wire serial peripheral. In the IC, the MCU interface is pin selectableby BS1 shown in Table 6-1.

Note

(1) L is connected to GND

(2) H is connected to VDDIO

Table 6-1 : Interface pins assignment under different MCU interface

MCU Interface	BS1	RST_N	CSB	DC	SCL	SDA
4-wire serial peripheral interface (SPI)	L	Required	CSB	D/C	SCL	SDA
3-wire serial peripheral interface (SPI) – 9 bits SPI	H	Required	CSB	L	SCL	SDA

6.3.2 MCU Serial Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCL, serial data SDA, D/C and CSB. The control pins status in 4-wire SPI in reading/writing command/data is shown in Table 6-2. The read/writeprocedure of 4-wire SPI is shown in Figure 6-1.

Table 6-2 : Control pins status of 4-wire SPI

Function	SCL pin	SDA pin	D/C pin	CSB pin
Write command	↑	Command bit	L	L
Read/Write data	↑	Data bit	H	L

Note:

(1) L is connected to GND and H is connected to VDDIO

(2) ↑ stands for rising edge of signal

(3) SDA (Write Mode) is shifted into an 8-bit shift register on every rising edge of SCL in theorder of D7, D6, ... D0. The level of D/C should be kept over the whole byte. The data bytein the shift register is written to the Graphic Display Data RAM (RAM)/Data Byte

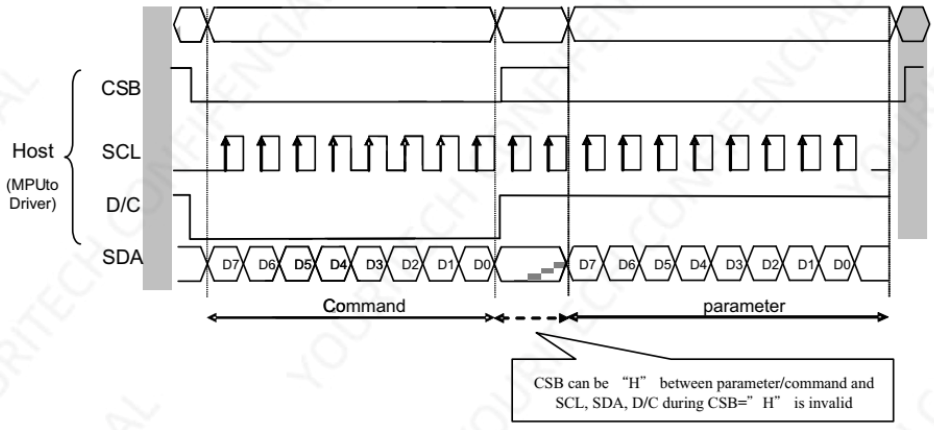


Figure 6-1 : Read/Write procedure in 4-wire SPI mode

6.3.3 MCU Serial Interface (3-wire SPI)

The 3-wire SPI interface consists of Serial Clock (SCL), Serial Data (SDA), and Chip Select (CSB). Its operation is similar to 4-wire SPI, but the D/C pin is not used and must be tied to a low level (LOW). The control pin states for 3-wire SPI are detailed in Table 6-3, and the read/write procedure is illustrated in Figure 6-3.

During read/write operations, a 9-bit data frame is shifted into the register on each clock's rising edge. The bit sequence is: D/C bit, followed by D7, D6, down to D0. The first bit (D/C) determines the type of the subsequent byte: a value of '0' indicates a command, and a value of '1' indicates data.

Function	SCL pin	SDA pin	D/C pin	CSB pin
Write command	↑	Command bit	Tie LOW	L
Read/Write data	↑	Data bit	Tie LOW	L

Note:

(1) L is connected to GND and H is connected to VDDIO

(2) ↑ stands for rising edge of signal

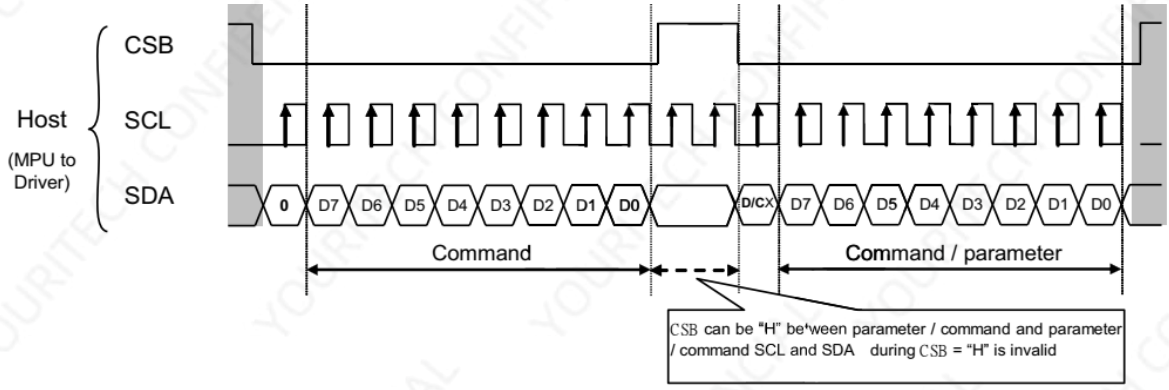
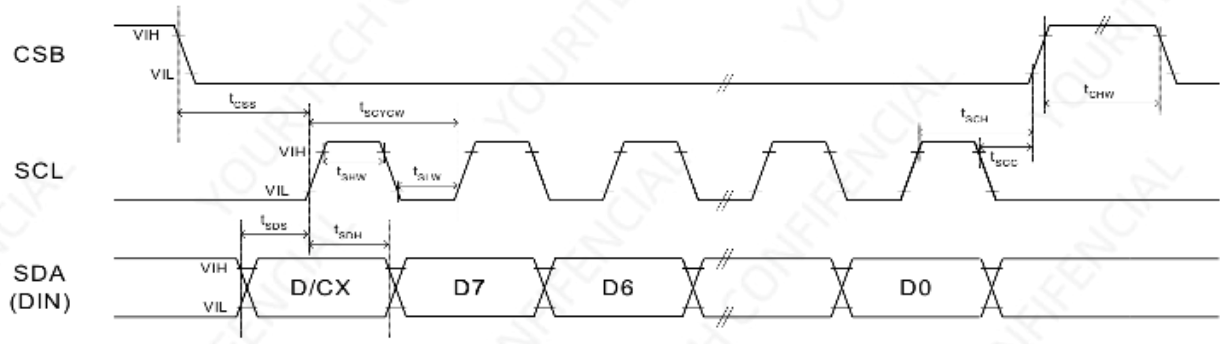


Figure 6-2: Read/Write procedure in 3-wire SPI mode

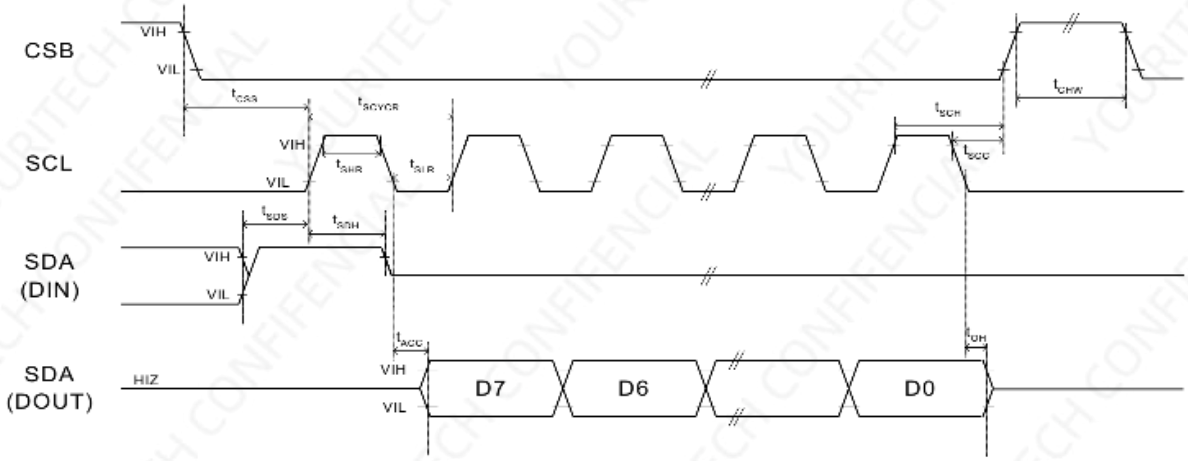
6.3.4 Interface Timing

Symbol	Parameter	Min	Typ	Max	Unit
t_{CSS}	CSB select setup time	60			ns
t_{SCH}	CSB select hold time	65			ns
t_{SCC}	CSB deselect setup time	25			ns
t_{CHW}	CSB deselect hold time	100			ns
t_{SCYCW}	Serial clock cycle (Write)	50			ns
t_{SHW}	SCL "H" pulse width (Write)	25			ns
t_{SLW}	SCL "L" pulse width (Write)	25			ns
t_{SCYCL}	Serial clock cycle (Read)	400			ns
t_{SHR}	SCL "H" pulse width (Read)	180			ns
t_{SLR}	SCL "L" pulse width (Read)	180			ns
t_{SDS}	Data setup time	30			ns
t_{SDH}	Data hold time	30			ns
t_{DCS}	DC setup time	40			ns
t_{DCH}	DC hold time	40			ns
t_{ACC}	Access time			100	ns
t_{OH}	Output disable time	15			ns

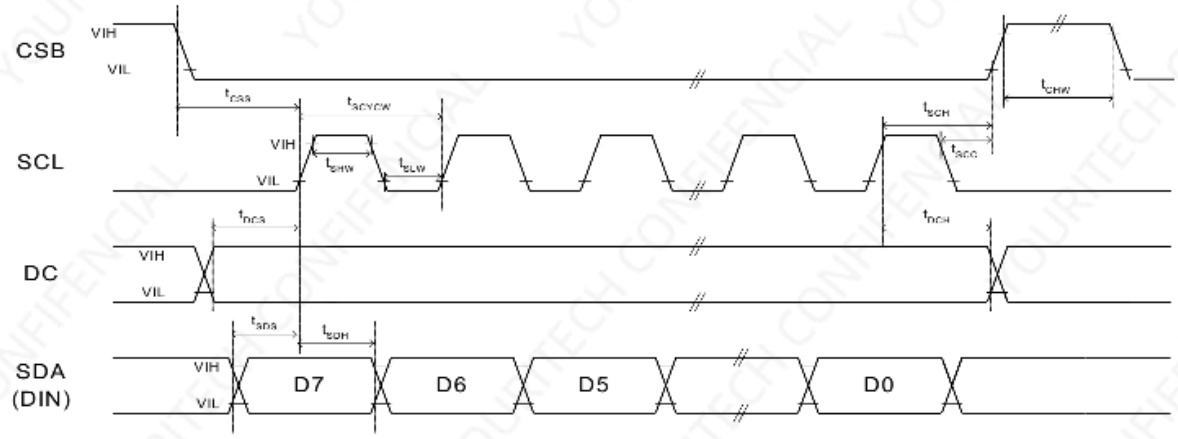
Note: All timings are based on 20% to 80% of VDDIO-GND



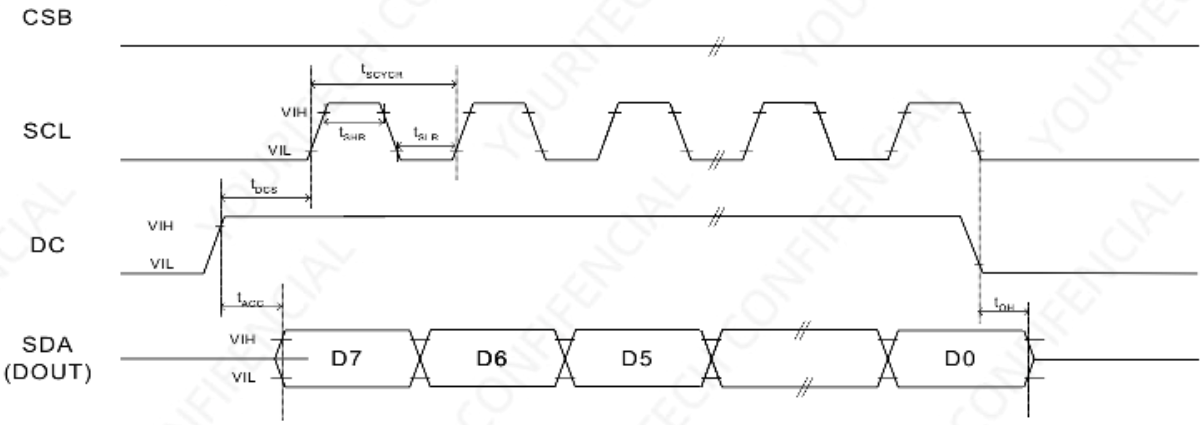
3 pin serial interface characteristics (write mode)



3 pin serial interface characteristics (read mode)



4 pin serial interface characteristics (write mode)



4 pin serial interface characteristics (read mode)

7. Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	00	0	0	0	0	0	0	0	0	PSR	Panel Setting Register A[7:0] = 2Fh [POR] B[7:0] = 09h [POR]
0	1		A_7	A_6	A_5	0	A_3	A_2	A_1	A_0		A[7:6] ~ RES[1:0] Display Resolution setting (source x gate) 00b: 960 x 680 (Default) 01b: 960 x 672 10b: 960 x 640 11b: 880 x 528 *Remark: Inactive Gate outputs will be VGL for DRF and AMV. Inactive Source outputs will follow VCOM LUT output for DRF A[5] ~ B_mode Blanking Mode for voltage switching, the duration setting follow CDI. 0: Mode A Blanking time only for ACVCOM. 1: Mode B (Default) Blanking time for ACVCOM or switch mode of source power. A[3] ~ UD Gate Scan Direction: 0: Scan down. First line to Last line: Gn-1 … G0 1: Scan up. (Default) First line to Last line: G0 … Gn-1 A[2] ~ SHL Source Shift Direction: 0: Shift left. First data to Last data: Sn-1 … S0 1: Shift right. (Default) First data to Last data: S0 … Sn-1 A[1] ~ SHD_N Booster and Regulator Switch: 0: PON / POF command will not execute 1: PON / POF command will execute (Default) A[0] ~ RST_N Soft Reset: 0: The controller is reset. Reset all registers to their default value. Driver all function will be disabled. 1: Normal operation (Default). BUSY_N signal will become “0” until Soft reset is finished.
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		B[7] ~ LUT_EN

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
												0: During reset, auto load LUT from OTP if it is valid. When PON/DRF, analog setting will follow the content of OTP. (Default) 1: During reset, no action to load LUT from OTP. When PON/DRF, analog setting will follow the content of MCU B[6:5] ~ FOPT[1:0] FOPT function 00b: NO effect. Scan 1 frame after waveform finished (Default) 01b: Will scan 1 frame same as last output (of LUT) after waveform finished. 10b: Will scan 1 frame with Floating output after waveform finished. 11b: No Scan after waveform finished (Power off floating) B[4] ~ VCMZ VCOM Hi-Z option 0: NO effect. (default) 1: VCOM is always floating. B[3] ~ TS_AUTO Temperature Sensor auto option 0: NO effect. 1: Before loading OTP, Temperature Sensor will be activated automatically one time. (default) B[2] ~ TIEG VGL power off option 0: NO effect. (default) 1: After power off booster, VGL will be tied to GND. B[1] ~ NORG VCOM display end GND option 0: NO effect. (default) 1: After refreshing display, VCOM is tied to GND before power off B[0] ~ VC_LUTZ VCOM display end floating option 0: NO effect. 1: After refreshing display, the output of VCOM is set to floating automatically (default)

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	01	0	0	0	0	0	0	0	1	PWR	Power setting Register A[5:0] = 07h [POR] B[7:0] = F0h [POR] C[6:0] = 00h [POR] D[6:0] = 00h [POR] E[6:0] = 00h [POR] F[6:0] = 00h [POR]
0	1		0	0	0	0	0	A_2	A_1	A_0		A[2] ~ VSC_EN Source LV power selection: 0: External source power for VSH2 pin. 1: Internal DCDC function for generate source power. (default) A[1] ~ VS_EN Source LV power selection; 0: External source power for VSH1 and VSL pin. 1: Internal DCDC function for generate source power. (default) A[0] ~ VG_EN Gate power selection: 0: External gate power for VGH and VGL pin. 1: Internal DCDC function for generate gate power. (default)

0	1		1	1	1	1	0	0	B_1	B_0		B[1:0] ~ VGPN [1:0] Internal VGH / VGL Voltage Level Selection:
0	1		0	C_6	C_5	C_4	C_3	C_2	C_1	C_0		C[6:0] ~ VSPL [6:0] Internal Source Voltage Level Selection for VSH2@Mode0:
0	1		0	D_6	D_5	D_4	D_3	D_2	D_1	D_0		D[6:0] ~ VSNL[6:0] Internal Source Voltage Level Selection for VSL@Mode1:

VGPN [1:0]	Gate Voltage Level
00	VGH=20V,VGL=-20V (Default) VSH1=15V, VSL=-15V
01	VGH=17V ,VGL=-17V VSH1=15V, VSL=-15V
10	VGH=15V,VGL=-15V VSH1=13V, VSL=-13V
11	Reserved.

VSPL[6:0]	Voltage Level
00h	3.0V (default)
02h	3.2V
04h	3.4V
06h	3.6V
:	:
76h	14.8V
78h	15.0V
Other	Reserved

VSNL[6:0]	Voltage Level
00h	-3.0V (default)
02h	-3.2V
04h	-3.4V
06h	-3.6V
:	:
76h	-14.8V
78h	-15.0V
Other	Reserved

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	1		0	E_6	E_5	E_4	E_3	E_2	E_1	E_0		E[6:0] ~ VSPL2[6:0] Internal Source Voltage Level Selection for VSH1@Mode1:
0	1		0	F_6	F_5	F_4	F_3	F_2	F_1	F_0		F[6:0] ~ VSNL2[6:0] Internal Source Voltage Level Selection for VSH2@Mode1:

VSPL2[6:0]	Voltage Level
00h	3.0V (default)
02h	3.2V
04h	3.4V
06h	3.6V
:	:
76h	14.8V
78h	15.0V
Other	Reserved

VSNL2[6:0]	Voltage Level
00h	3.0V (default)
02h	3.2V
04h	3.4V
06h	3.6V
:	:
76h	14.8V
78h	15.0V
Other	Reserved

0	0	02	0	0	0	0	0	0	1	0	POF	Power OFF Command Register
0	1		0	0	0	0	0	0	0	0		After power off command, driver will power off based on the Power OFF Sequence. BUSY_N will output low during operation. The Power OFF command will turn off DCDC, source driver, gate driver, VCOM driver, temperature sensor, but register and SRAM data will keep until VDD off. SD output will base on previous condition. *Remark: POF works at PON only
0	0	03	0	0	0	0	0	0	1	1	POFS	Power on/off Sequence Setting Register A[7:0] = 00h [POR]
0	1		0	0	A_5	A_4	0	0	A_1	A_0		A[5:4] ~ T_VDPG_OFF[1:0] Power off delay from VGL to VGH 00b: 20ms (default) 01b: 40ms 10b: 60ms 11b: 80ms A[1:0] ~ T_VDS_OFF[1:0] Power off delay from VSHX/VSL to VGH 00b: 20ms (default) 01b: 40ms 10b: 60ms 11b : 80ms

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	04	0	0	0	0	0	1	0	0	PON	Power ON Command Register After the Power ON command, driver will power on based on the Power ON Sequence. BUSY_N will output low during operation. * Remark: PON Include booster on, VSH1/VSH2/VSL regulator on With default BTST, timing is >80ms
0	0	06	0	0	0	0	0	1	1	0	BTST	VGH Booster Soft Start Setting Register (for VGH) A[6:0] = 0Fh [POR] B[6:0] = 8Bh [POR] C[6:0] = 93h [POR] D[6:0] = A3h [POR]
0	1		0	A_6	A_5	A_4	A_3	A_2	A_1	A_0		A[6:4] ~ VGHSSC_ONT [2:0] VGH booster maximum MOSFET ON time (reserved) A[6:4] = 000 (Default) A[3:2] ~ T_VGHSSA [1:0] = 11 (Default) VGH booster soft start Phase A duration A[1:0] ~ T_VGHSSB [1:0] = 11 (Default) VGH booster soft start Phase B duration
0	1		1	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		1	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	1		1	D_6	D_5	D_4	D_3	D_2	D_1	D_0		

	Soft Start Phase Period (ms)
00	10
01	20
10	30
11	40

B[6:4] ~ VGHSSA_DRV [2:0], = 000 (Default)
VGH Phase A Driving Strength
C[6:4] ~ VGHSSB_DRV [2:0], = 001 (Default)
VGH Phase B Driving Strength
D[6:4] ~ VGHSSC_DRV [2:0] = 010 (Default)
VGH Phase C Driving Strength

Driving Strength			
000	0	100	(reserved)
001	1	101	(reserved)
010	2	110	(reserved)
011	3(strongest)	111	(reserved)

B[3:0] ~ VGHSSA_OFFT[[3:0], = 1011 (Default)
VGH Phase A Minimum OFF Time
C[3:0] ~ VGHSSB_OFFT[[3:0], = 0011 (Default)
VGH Phase B Minimum OFF Time
D[3:0] ~ VGHSSC_OFFT[[3:0], = 0011 (Default)
VGH Phase C Minimum OFF Time

Minimum OFF Time (setting)			
0000	OFFH0	1000	OFFH8
0001	OFFH1	1001	OFFH9
0010	OFFH2	1010	OFFHA
0011	OFFH3	1011	OFFHB
0100	OFFH4	1100	OFFHC
0101	OFFH5	1101	OFFHD
0110	OFFH6	1110	OFFHE
0111	OFFH7	1111	OFFHF

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	07	0	0	0	0	0	1	1	1	DSLP	Deep Sleep Register
0	1		1	0	1	0	0	1	0	1		This command makes the chip enter the deep-sleep mode. The deep sleep mode could return to stand-by mode by hardware reset assertion. The only one parameter is a check code, the command would be executed if check code is A5h.
0	0	10	0	0	0	1	0	0	0	0	DTM	Data Start transmission Register
2 bit per pixel												This command indicates that user starts to transmit data. Then write to SRAM. While complete data transmission, user must send a Data Refresh command (R12H). Then the chip will start to send data/VCOM for panel.
0	1		KPixel1 [1:0]		KPixel2 [1:0]		KPixel3 [1:0]		KPixel4 [1:0]			
:			...									
0	1		KPixel (4M-3) [1:0]		KPixel (4M-2) [1:0]		KPixel (4M-1) [1:0]		KPixel (4M) [1:0]			

KPixel[1:0] Source Driver Output

	DDX=1 (Default)	DDX=0
00b	Gray 0	Gray 3
01b	Gray 1	Gray 2
10b	Gray 2	Gray 1
11b	Gray 3	Gray 0

After issue this command, the host must send at least 1 byte data to the device.

0	0	12	0	0	0	1	0	0	1	0	DRF	Display Refresh Command Register
0	1		0	0	0	0	0	0	0	0		After this command is issued, driver will refresh display (data/VCOM) according to SRAM data and LUT. BUSY_N will output low during operation.
0	0	17	0	0	0	1	0	1	1	1	AUTO	Auto Sequence Register
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		This command makes the chip enter the auto sequence Single-chip application ONLY. Auto Sequence Option 0xA5: Start Auto Sequence (PON > DRF > POF) 0xA7: Start Auto Sequence (PON > DRF > POF > DSLP). Others: No effect BUSY_N signal will become "0" until Auto Sequence is finished.

0	0	30	0	0	1	1	0	0	0	0	PLL	Frame Rate Control register The command controls the clock frequency. A[3:0] = 2h [POR]
0	1		0	0	0	0	0	A_2	A_1	A_0		A[3]: Dynamic Frame Rate 0: Disable (Default) 1: Enable A[2:0] ~ FR[2:0] It supports the following frame rates. Frame Rate Selection, Frame rate for Gate/Source switching that exclude the blanking time defined in CDI.

FR[2:0]	Frame Rate Selection
000	12.5Hz
001	25Hz
010	50Hz (Default)
011	65Hz
100	75Hz
101	85Hz

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	40	0	1	0	0	0	0	0	0	TSC	Temperature Sensor Command Register
1	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		This command enables internal temperature sensor. BUSY_N will output low during operation. Then the temperature value can be read in 1degC step A[7:0] ~ TS [7:0]

TS [7:0]	Return Value(degC)
E7h	-25
...	...
FFh	-1
00h	0
01h	1
...	...
19h	25
...	...
31h	49
32h	50

0	0	41	0	1	0	0	0	0	0	1	TSE	Temperature Sensor Enable Register This command selects Temperature offset A[7:0] = 00h [POR]
0	1		0	0	0	0	A_3	A_2	A_1	0		A[3:0] ~ TO[3:1] , Temperature offset:

TO[3:1]	Calculation	TO[3:1]	Calculation
000	+0	100	-4
001	+1	101	-3
010	+2	110	-2
011	+3	111	-1

0	0	50	0	1	0	1	0	0	0	0	CDI	VCOM and DATA interval setting Register This command indicates the Border Output Selection and the interval between Vcom and data output A[7:0] = 97h [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		A[7:5]~VBD [2:0] Border Output Selection:

	DDX=1	DDX=0
VBD[2:0]	LUT (Default)	LUT
000	Gray 0	HIZ
001	Gray 1	Gray 3
010	Gray 2	Gray 2
011	Gray 3	Gray 1
100	HIZ(Default)	Gray 0

A[4]: DDX
Data Polarity for Pixel Data (See DTM command)
0: Invert
1: Non-invert (Default)
A[3:0] ~ CDI[3:0]
Gate and source blanking time (No gate source scanning)

CDI [3:0]	Interval (ms)	CDI [3:0]	Interval (ms)
0h	2	8h	40
1h	4	9h	60
2h	8	Ah	80
3h	12	Bh	100
4h	14	Ch	120
5h	16	Dh	140
6h	18	Eh	160
7h	20 (Default)	Fh	Reserved

User needs to review CDI setting to have stable VCOM in application

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	51	0	1	0	1	0	0	0	1	LPD	Lower Power Detection Register
1	1		0	0	0	0	0	0	0	A_0		BUSY_N will output low during operation. Then the LPD status can be read. A[0] ~ LPD status 0: Low power input (VDD<2.5V, selected by LVD_SEL[1:0] in command LVSEL) 1: Normal (default)
0	0	61	0	1	1	0	0	0	0	1	TRES	Resolution setting Register A[9:0] = 3C0h [POR] B[9:0] = 2A8h [POR]
0	1		0	0	0	0	0	0	A_9	A_8		This command defines alternative resolution. A[9:0] ~ HRES[9:0] Horizontal Display Resolution Remark: Horizontal resolution should be 4-multiple. B[9:0] ~ VRES[9:0] Vertical Display Resolution e.g. HRES= 3C0h, VRES= 2A8h
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	B_9	B_8		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	0	65	0	1	1	0	0	1	0	1	GSST	Gate/Source Start Setting Register A[9:0] = 0x000h [POR] B[9:0] = 0x000h [POR]
0	1								A_9	A_8		A[9:0] ~ S_start[9:0] First valid source output channel setting
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1								B_9	B_8		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		

UD,SHL	Source and gate sequence
00	S959,G679 to S0,G0
01	S0, G679 to S959,G0
10	S959,G0 to S0, G679
11	S0,G0 to S959, G679

Remark:
1) Both PSR.RES & TRES command can set panel resolution. Priority will be given to the last received PSR or TRES command.
2) VRES[9:0] >= 420

S_start [9:0]	First valid source output
000h	S0 (Default)
004h	S4
008h	S8
…	…
3B8h	S952
3BCh	S956
Other	Reserved

											B[9:0] ~ G_start[9:0] First valid gate output channel setting GSST and TRES can define the display window from target source and gate start and end line. GD: First G active = G16, G_start[9:0]=16. Last G active = G543, VRES[9:0]=528. SD: First S active = S8, S_start[9:0]=8. Last S active = S887, HRES[9:0]=880. Remark: G_start+VRES< 680, S_start+HRES< 960.

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	70	0	1	1	1	0	0	0	0	REV	Chip Revision Register The command is to read the ID A[7:0] = 07h [POR] B[7:0] = 01h [POR] C[7:0] = 01h [POR]
1	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	0	80	1	0	0	0	0	0	0	0	AMV	Auto Measurement VCOM Register This command implements related VCOM sensing setting. A[7:0] = 00h [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	0	A_0		A[7:6] ~ P[1:0] Number of sensing Points 00: 2 (Default) 01: 4 10: 8 11: 16 A[5:4] ~AMVT[1:0] Auto Measure Vcom Time: Sensing Time 00: 5 sec. (Default) 01: 10 sec. 10: 15 sec. 11: 20 sec. A[3] ~ AMVX VCOM measurement Gate settings 0: Gate scan normally during VCOM measurement (Default) 1: All Gates ON during VCOM measurement A[2] ~ AMVS Source output of AMV: 0: Set Source output to 0V during Auto Measure VCOM period. (Default) 1: Set Source output to VSH_LV during Auto Measure VCOM period. A[0] ~ AMVE Auto Measure Vcom Enable (/Disable): 0: Disabled (Default) 1: Enabled BUSY_N will output low during operation. Note: AMV only can work while PON only

0	0	81	1	0	0	0	0	0	0	1	VV	Auto Measurement VCOM Register This command gets the Vcom value after AMV.
1	1		1	0	A_5	A_4	A_3	A_2	A_1	A_0		A[5:0] ~ VV[5:0]: Vcom read Value , valid range from -0.2V to -4.0V.

VV[5:0]	Vcom read value
00h	Reserved
04h	-0.2V
08h	-0.4V
0Ch	-0.6V
10h	-0.8V
…	…
3Ch	-3.0V
…	…
50h	-4.0V
others	Reserved

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	82	1	0	0	0	0	0	1	0	VDCS	VCM_DC Setting Register This command sets VCOM_DC value. A[7:0] = 00h [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	0	0		A[7] ~ OTP_VCM Vcom follow VDCS after RESET. 0: Disable (Default), auto load from OTP if it is valid. 1: Enable, VCOM value from the VDCS[6:0] A[6:0] ~ VDCS[6:0]: VCOM_DC Setting, 0.2V step from -0.2V to -4.0V.

VDCS [6:0]	VCOM_DC Setting
00h	Reserved
04h	-0.2V
08h	-0.4V
0Ch	-0.6V
10h	-0.8V
…	…
3Ch	-3.0V
…	…
50h	-4.0V
others	Reserved

0	0	83	1	0	0	0	0	0	1	1	PTLW	Partial Window This command sets partial window address. A[9:0] = 000h [POR] B[9:0] = 3BFh [POR] C[9:0] = 000h [POR] D[9:0] = 2A7h [POR] E[7:0] = 00h [POR]
0			0	0	0	0	0	0	A_9	A_8		
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	B_9	B_8		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		0	0	0	0	0	0	C_9	C_8		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		A[9:0] ~ HRST [9:0] Horizontal start address B[9:0] ~ HRED [9:0] Horizontal end address C[9:0] ~ VRST [9:0] Vertical start address D[9:0] ~ VRED [9:0] Vertical end address E[0] ~ PMODE 0: disable partial mode (Default) 1: enable partial mode Gate scan both inside and outside of the partial window Note: 1) HRST [9:0]<= HRED [9:0] 2) VRST [9:0]<= VRED [9:0]
0	1		0	0	0	0	0	0	D_9	D_8		
0	1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
0	1		0	0	0	0	0	0	0	E_0		

<table>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>90</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>PGM</td><td>Program Mode
This command is to set OTP program mode
After this command is issued, the chip would enter the program mode.
After the programming procedure completed, a hardware reset is necessary for leave the program mode

BUSY_N will output low when PGM mode is ready.</td></tr>
<tr><td>0</td><td>0</td><td>91</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>APG</td><td>Active Program
This command is to execute OTP program
After this command is issued, the chip would program the OTP.
BUSY_N will output low during operation.

Note: In PON mode with internal programming power.</td></tr>
<tr><td>0</td><td>0</td><td>92</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>ROTP</td><td>Read OTP Data</td></tr>
<tr><td>1</td><td>1</td><td colspan="9">1st ~ dummy
2nd ~ N+1th Parameter</td><td>This command is to read the OTP content from SRAM.

The 1st byte read is dummy byte.
The 2nd byte read is the content of Address 0 in OTP
The N+1th byte read is the content of Address n in OTP
After issue this command, the host must read at least 1 byte data from the device.</td></tr>
<tr><td>0</td><td>0</td><td>E0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>CCSET</td><td>Cascade & External temperature input
A[7:0] = 00h [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A1</td><td>A0</td><td></td><td>A[1] ~ TSFIX
0: Use Internal Temperature Sensor (Default)
1: Use command 0xE6 TS_SET [7:0] value
A[0] ~ CSEIN, cascade mode enable
0: Disable
1: Enable</td></tr>
<tr><td>0</td><td>0</td><td>E3</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>PWS</td><td>Power Saving Register
This command is sets for saving power VCOM/Source power saving during display refresh period.
A[7:0] = 65h [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td></td><td>If the output voltage of VCOM/Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.

A[7:4] = VCOM_W [3:0]
<table>
<tr><th>VCOM_W [3:0]</th><th>VCOM_power saving width. (time unit)</th><th>VCOM_W [3:0]</th><th>VCOM_power saving width. (time unit)</th></tr>
<tr><td>0</td><td>Reserved</td><td>8</td><td>8</td></tr>
<tr><td>1</td><td>1</td><td>9</td><td>9</td></tr>
<tr><td>2</td><td>2</td><td>10</td><td>10</td></tr>
<tr><td>3</td><td>3</td><td>11</td><td>11</td></tr>
<tr><td>4</td><td>4</td><td>12</td><td>12</td></tr>
<tr><td>5</td><td>5</td><td>13</td><td>13</td></tr>
<tr><td>6</td><td>6[Default]</td><td>14</td><td>14</td></tr>
<tr><td>7</td><td>7</td><td>15</td><td>15</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>A[3:0] = SD_W [3:0]
<table>
<tr><th>SD_W [3:0]</th><th>Source power saving width[us]</th><th>SD_W [3:0]</th><th>Source power saving width [us]</th></tr>
<tr><td>0</td><td>Reserved</td><td>8</td><td>4</td></tr>
<tr><td>1</td><td>0.5</td><td>9</td><td>4.5</td></tr>
<tr><td>2</td><td>1</td><td>10</td><td>5</td></tr>
<tr><td>3</td><td>1.5</td><td>11</td><td>5.5</td></tr>
<tr><td>4</td><td>2</td><td>12</td><td>6</td></tr>
<tr><td>5</td><td>2.5[Default]</td><td>13</td><td>6.5</td></tr>
<tr><td>6</td><td>3</td><td>14</td><td>7</td></tr>
<tr><td>7</td><td>3.5</td><td>15</td><td>7.5</td></tr>
</table>
Remark:
VCOM_W setting < CDI setting
SD_W setting < S2G setting</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>E4</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>LVSEL</td><td>LVD Voltage Select Register
This command is sets for low power detect level power
A[1:0] = 03h [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_1</td><td>A_0</td><td></td><td>A[1:0] ~ LVD_SEL[1:0]
Low power detection threshold
00: 2.2V
01: 2.3V
10: 2.4V
11 : 2.5V (Default)</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>E6</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>TS_SET</td><td>Manual input temperature value
This command is to force the TS value
A[7:0] = 00h [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td>A[7:0] ~ TS_SET[7:0]
When TSFIX=1, Temperature value will be set by TS_SET[7:0].
Format of the temperature value is 8-bit binary value and it is 1degC per step.
<table>
<tr><th>TS_SET[7:0]</th><th>Force the TS Value(degC)</th></tr>
<tr><td>E7h</td><td>-25</td></tr>
<tr><td>…</td><td>…</td></tr>
<tr><td>FFh</td><td>-1</td></tr>
<tr><td>00h</td><td>0</td></tr>
<tr><td>01h</td><td>1</td></tr>
<tr><td>…</td><td>…</td></tr>
<tr><td>19h</td><td>25</td></tr>
<tr><td>…</td><td>…</td></tr>
<tr><td>31h</td><td>49</td></tr>
<tr><td>32h</td><td>50</td></tr>
</table></td></tr>
</table>

8. Optical Specifications

Measurements are made with that the illumination is under an angle of 45 degree, the detectionis perpendicular unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ.	Max	Units	Notes
R	White Reflectivity	White	30	35	-	%	8-1
CR	Contrast Ratio	Indoor	8:1		-		8-2
T update	Image update time	at 25 °C		26	-	sec	
Life		Topr		1000000times or 5years			

Notes: 8-1. Luminance meter: Eye-One Pro Spectrophotometer.
8-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

9. Matched Development Kit

Our Development Kit designed for SPI E-paper Display aims to help users to learn how to use E-paper Display more easily. It can refresh black-white E-paper Display, three-color (black, white and red/Yellow) E-paper Display and four-color(black, white, red and yellow) YOURITECH 's E-pa p er Display. And it is also added the functions of USB serial port, FLASH c hip, font chip, current detection ect.
Development Kit consists of the development board and the pinboard.

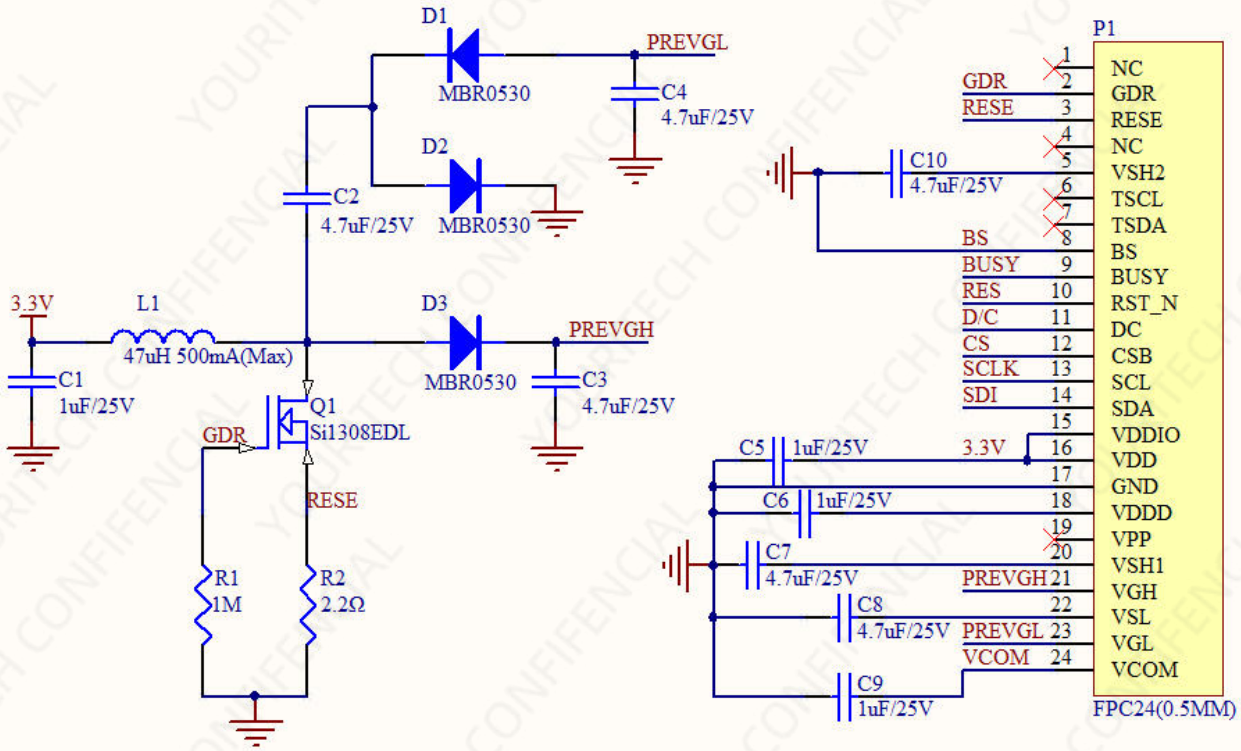
Supported development platforms include STM32, ESP32, ESP8266, Arduino UNO, etc.

10. Reliability test

NO	Test items	Test condition
1	Low-Temperature Storage	T = -25°C, 240 h Test in white pattern
2	High-Temperature Storage	T=60° C， RH=35%， 240h Test in white pattern
3	High-Temperature Operation	T=40° C， RH=35%， 240h
4	Low-Temperature Operation	T=0° C， 240h
5	High-Temperature, High-Humidity Operation	T=40° C， RH=80%， 240h
6	High Temperature, High Humidity Storage	T=50° C， RH=90%, 240h Test in white pattern
7	Temperature Cycle	1 cycle:[-25℃ 30min]→[+60℃ 30 min] : 50 cycles Test in white pattern
8	UV exposure Resistance	765W/m² for 168hrs,40 °C Test in white pattern
9	ESD Gun	Air+/-15KV;Contact+/-8KV (Test finished product shell, not display only) Air+/-8KV;Contact+/-6KV (Naked EPD display, no including IC and FPC area) Air+/-4KV;Contact+/-2KV (Naked EPD display, including IC and FPC area)

Note: Put in normal temperature for 1hour after test finished, display performance is ok.

11. Typical Application Circuit

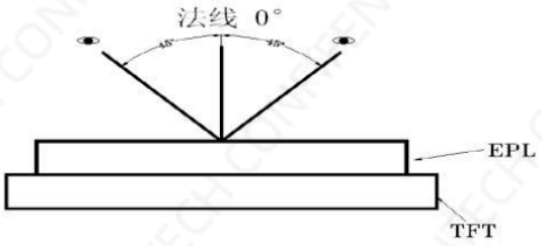


Part Name	Requirements for spare part
C1—C10	0603/0805; X5R/X7R;Voltage Rating:≥25V
R1、R2	0603/0805;1% variation,≥0.05W
D1—D3	MBR0530: 1)Reverse DC Voltage≥30V 2)Io≥500mA 3)Forward voltage ≤430mV
Q1	Si1308EDL:1)Drain-Source breakdown voltage≥30V 2)Vgs(th)≤1.5V 3)Rds(on)≤400mΩ
L1	refer to NR3015: Io=500mA(max)
P1	24pins,0.5mm pitch

12. Inspection method and condition

12.1Inspection Condition

Item	Condition
Illuminance	800~1500 lux
Temperature	22℃±3℃
Humidity	55±10 %RH
Distance	≥30cm
Angle	Vertical fore and aft 45
Inspection method	By eyes

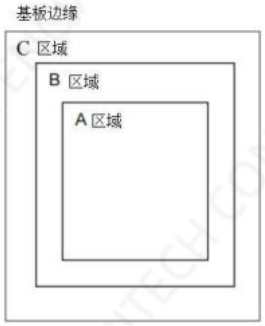


12. 2 Zone definition

A Zone： Active area

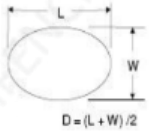
B Zone： Border zone

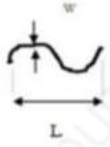
C Zone： From B zone edge to panel edge

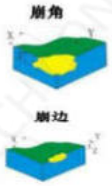
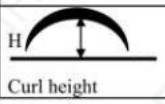


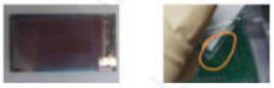
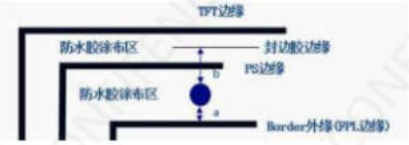
12.3 General inspection standards for products

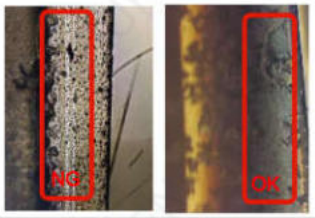
12.3.1Appearance inspection standard

Inspection item		Figure		A zone inspection standard	B/C zone	Inspection method	MAJ/ MIN
Spot defects	Spot defects such as dot, foreign matter, air bubble, and dent etc.	Diameter D=(L+W)/2 (L-length、W-width) Measuring method shown in the figure below 	The distance between the two spots should not be less than 10mm	7.5"-13.3"Module（Not include 7.5"）： D＞1mm N=0 0.5＜D≤0.8 N≤4 D≤0.5 Ignore 0.8＜D≤1 N≤2 4.2"-7.5"Module（Not include 4.2"）： D＞0.5 N=0 0.4＜D≤0.5 N≤2 D≤0.25 Ignore 0.25＜D≤0.4 N≤4 Module below 4.2"： D＞0.5 N=0 0.4＜D≤0.5 N≤1 D≤0.25 Ignore 0.25＜D≤0.4 N≤4 0.1mm＜D≤0.25 N≤3/cm²	Foreign matter D≤1mm Pass	Check by eyes Film gauge	MIN

Inspection item		Figure		A zone inspection standard	B/C zone	Inspection method	MAJ/ MIN
Line defects	Line defects such as scratch, hair etc.	L-Length，W-Width，(W/L)＜1/4 Judged by line， (W/L)≥1/4 Judged by dot 	The distance between the two lines should not be less than 5mm	7.5"-13.3"Module（Not include 7.5"）： L＞10mm,N=0 W＞0.8mm，N=0 5mm≤L≤10mm，0.5mm≤W≤0.8mm N≤2 L≤5mm，W≤0.5mm Ignore 4.2"-7.5"Module（Not include 4.2"）： L＞8mm,N=0 W＞0.2mm，N=0 2mm≤L≤8mm，0.1mm≤W≤0.2mm N≤4 L≤2mm，W≤0.1mm Ignore Module below 4.2"： L＞5mm,N=0 W＞0.2mm，N=0 2mm≤L≤5mm，0.1mm≤W≤0.2mm N≤4 L≤2mm，W≤0.1mm Ignore	Ignore	Check by eyes Film gauge	MIN

Inspection item		Figure	Inspection standard	Inspection method	MAJ/ MIN
Panel chipping and crack defects	TFT panel chipping	X the length, Y the width, Z the chipping height, T the thickness of the panel 	Chipping at the edge： Module over 7.5"（Include 7.5"）： X≤ 6mm,Y≤1mm Z≤T N=3 Allowed Module below 7.5"(Not include 7.5")： X≤ 3mm,Y≤1mm Z≤T N=3 Allowed Chipping on the corner： IC sideX≤2mm Y≤2mm, Non-IC sideX≤1mm Y≤1mm . Allowed Note： Chipping should not damage the edge wiring. If it does not affect the display, allowed	Check by eyes、 Film gauge	MIN
	Crack		Crack at any zone of glass , Not allowed	Check by eyes、Film gauge	MIN
	Burr edge		No exceed the positive and negative deviation of the outline dimensions X+Y≤0.2mm Allowed	Calliper	MIN
	Curl of panel		Curl height H≤Total panel length 1% Allowed	Check by eyes	MIN

Inspection item		Figure	Inspection standard	Inspection method	MAJ / MIN
PS defect	Water proof film		1 .Waterproof film damage, wrinkled, open edge, not allowed 2. Exceeding the edge of module(according to the lamination drawing) Not allowed 3. Edge warped exceeds height of technical file, not allowed	Check by eyes	MIN
RTV defect	Adhesive effect		Adhesive height exceeds the display surface, not allowed	Check by eyes	MIN
			1 .Overflow, exceeds the panel side edge, affecting the size, not allowed 2 .No adhesive at panel edge≤1mm, mo exposure of wiring, allowed 3. No adhesive at edge and corner1*1mm, no exposure of wiring, allowed		
			Protection adhesive, coverage width within W≤1.5mm, no break of adhesive, allowed		
	Adhesive re-fill		Dispensing is uniform, without obvious concave and breaking, bubbling and swell, not higher than the upper surface of the PS, and the diameter of the adhesive re-filling is not more than 8mm, allowed	Check by eyes	MIN
EC defect	Adhesive bubble		1、 Effective edge sealing area of hot melt products ≥1/2 edge sealing area; 2、Bubble a+b≥1/2 effective width, N≤3, spacing≥5mm , allowed No exposure of wiring, allowed	Check by eyes	MIN

Inspection item		Figure	Inspection standard	Inspection method	MAJ/ MIN
EC defect	Adhesive effect		1 .Overflow, exceeds the panel side edge, affecting the size, not allowed 2.No adhesive at panel edge≤1mm, mo exposure of wiring, allowed 3.No adhesive at edge and corner 1*1mm, no exposure of wiring, allowed 4. Adhesive height exceeds the display surface, not allowed	Visual, caliper	MIN
Silver dot adhesive defect	Silver dot adhesive		1、Single silver dot dispensing amount ≥1mm, allowed 2、One of the double silver dot dispensing amount is ≥1mm and the other has adhesive (no reference to 1mm) Allowed	Visual	MIN
			Silver dot dispensing residue on the panel ≤0.2mm, allowed	Film gauge	MIN
FPC defect	FPC wiring FPC golden finger		FPC, TCP damage / gold finger peroxidation, adhesive residue, not allowed	Visual	MIJ
			The height of burr edge of TCP punching surface ≅ 0.4mm, not allowed	Caliper	MIN
	FPC damage/crease		Damage and breaking, not allowed Crease does not affect the electrical performance display, allowed	Check by eyes	MIN

Inspection item		Figure	Inspection standard	Inspection method	MAJ/ MIN
Protective film defect	Protective film	Scratch and crease on the surface but no affect to protection function, allowed		Check by eyes	MIN
		Adhesive at edge L≤5mm，W≤0.5mm，N=2, no entering into viewing area		Check by eyes	MIN
Stain defect	Stain	If stain can be normally wiped clean by > 99% alcohol, allowed		Visual	MIN
Pull tab defect	Pull tab	The position and direction meet the document requirements, and ensure that the protective film can be pulled off.		Check by eyes/ Manual pulling	MIN
Shading tape defect	Shading tape	Tilt≤10°, flat without warping, completely covering the IC.		Check by eyes/ Film gauge	MIN
Stiffener	Stiffener	Flat without warping, Exceeding the left and right edges of the FPC is not allowed. Left and right can be less than 0.5mm from FPC edge		Check by eyes	MIN
Label	Label/ Spraying code	The content meets the requirements of the work sheet. The attaching position meets the requirements of the technical documents.		Check by eyes	MIN

13. Handling, Safety and Environmental Requirements

WARNING
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

Data sheet status	
Product specification	The data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and dose not form part of the specification.	

Product Environmental certification
RoHS

14. Precautions

(1) Do not apply pressure to the EPD panel in order to prevent damaging it.

(2) Do not connect or disconnect the interface connector while the EPD panel is in operation.

(3) Do not touch IC bonding area. It may scratch TFT lead or damage IC function.

(4) Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.

(5) If the EPD Panel / Module is not refreshed every 24 hours, a phenomena known as "Ghosting" or "Image Sticking" may occur. It is recommended to refreshed the ESL / EPD Tag every 24 hours in use case. It is recommended that customer ships or stores the ESL / EPD Tag with a completely white image to avoid this issue

(6) High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel's performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time.