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MODEL NO.:ET167BA01-YF

SUFFIX: B

Approved by	Checked by	Prepaerd by	Customer Approved
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1.0 GENERAL DESCRIPTION

1.1 Introduction

This specification applies to the Color TFT-LCD Module ET167BA01-YF. OC uses BOE · This LCD module has a TFT active matrix type liquid crystal panel 1920x540 pixels, and diagonal size of 16.7 inch.

1.2 Features

Model		YFHD167BSM01-A	Unit	Note
LCD	Type	16.7	inch	
	Display Area	408.96(H) x115.02(V)	mm	
	Driver Element	a-Si TFT		
	Display Colors	16.7M	Colors	
	Number of Pixels	1920x540	Pixel	
	Pixel Pitch	213X213	um	
	Viewing Angle	89/89/89/89		
	Contrast Ratio	1000:1		
	Response Time	14	ms	
	Backlight	LED		
	Brightness	500	nits	
	Aspect Ratio	32;9		
	Surface Treatment	Haze 25%,		
Power	Consumption	≤30	W	
Operation Conditions	OperatingTemperature	-20 ~ 70	°C	
	Storage Temperature	-20 ~ 70	°C	
	Humidity	20% ~ 60%		
Dimensions (mm)		436(H) x 135(V) x12(D)	mm	
Pixel arrangement		RGB Vertical stripe		
8-bit color depth, display 16.7M colors				



2.0 ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 2.

< Table 2. Open Cell Electrical Specifications >

[VSS=GND=0V]

Parameter	Symbol	Min.	Max.	Unit	Remark
Power Supply Voltage	VDD	-0.3	6.0	V	Ta = 25 °C
Logic Supply Voltage	VIN	VSS-0.3	VDD+0.3	V	
Operating Temperature	T _{OP}	-20	+70	°C	Note 1
Storage Temperature	T _{SUR}	-20	+70	°C	
	T _{ST}	-20	+70	°C	
Operating Ambient Humidity	Hop	10	80	%RH	
Storage Humidity	Hst	10	80	%RH	



3.0 ELECTRICAL SPECIFICATIONS

3.1 TFT LCD Open Cell

< Table 3. Open Cell Electrical Specifications >

[Ta =25±2 °C]

Parameter		Symbol	Values			Unit	Remark
			Min	Typ	Max		
Power Supply Input Voltage		VDD	4.5	5.0	5.5	Vdc	
Power Supply Ripple Voltage		VRP	-	-	200	mV	
Power Supply Current		IDD	-	400	1000	mA	Note 1
Power Consumption		PDD	-	2	5	Watt	
Rush current		IRUSH	-		3.0	A	Note 2
LVDS Interface	Differential Input High Threshold Voltage	VLVTH	+100	-	+300	mV	
	Differential Input Low Threshold Voltage	VLVTL	-300	-	-100	mV	
	Input Differential Voltage	VID	200	-	600	mV	
	Differential input common mode voltage	VCM	1.0	1.2	1.5	V	

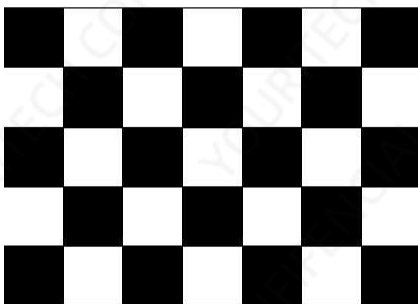
Note 1 : The supply voltage is measured and specified at the interface connector of LCM.

The current draw and power consumption specified is for VDD=5.0V,

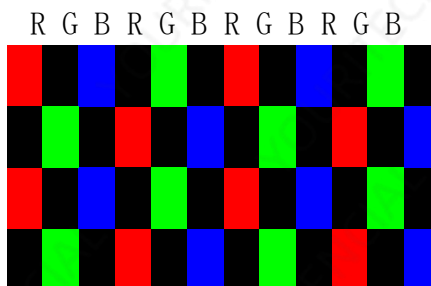
Frame rate $f_v=60\text{Hz}$ and Clock frequency = 74.25MHz.

Test Pattern of power supply current

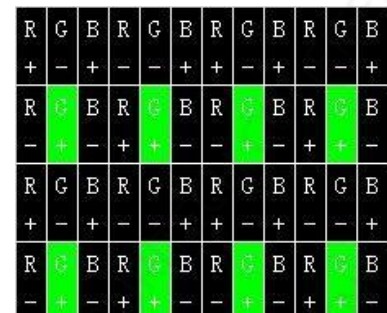
a) Typ : Mosaic 7X5 (L0/L255)



b) Max : Skip 1 dot Pattern



c) Flicker Pattern



Note 2 : The duration of rush current is about 2ms and rising time of Power Input is 1ms(min)



4.0 INTERFACE CONNECTION

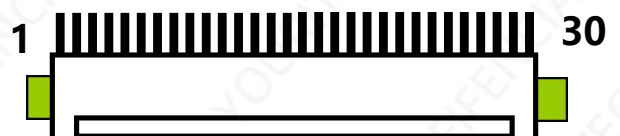
4.1 Open Cell Input Signal & Power (CN101)

- LVDS Connector : IS100-L300-C23(UJU), MSBKT2407P30HC(STM) or Equivalent.

< Table 4. Open Cell Input Connector Pin Configuration >

Pin No	Symbol	Description	Pin No	Symbol	Description
1	RXO0-	Negative Transmission data of Pixel 0 (ODD)	16	RXE1+	Positive Transmission data of Pixel 1 (EVEN)
2	RXO0+	Positive Transmission data of Pixel 0 (ODD)	17	GNG	Power Ground
3	RXO1-	Negative Transmission data of Pixel 1 (ODD)	18	RXE2-	Negative Transmission data of Pixel 2 (EVEN)
4	RXO1+	Positive Transmission data of Pixel 1 (ODD)	19	RXE2+	Positive Transmission data of Pixel 2 (EVEN)
5	RXO2-	Negative Transmission data of Pixel 2 (ODD)	20	RXEC-	Negative Transmission Clock (EVEN)
6	RXO2+	Positive Transmission data of Pixel 2 (ODD)	21	RXEC+	Positive Transmission Clock (EVEN)
7	GND	Power Ground	22	RXE3-	Negative Transmission data of Pixel 3 (EVEN)
8	RXOC-	Negative Transmission Clock (ODD)	23	RXE3+	Positive Transmission data of Pixel 3 (EVEN)
9	RXOC+	Positive Transmission Clock (ODD)	24	GND	Power Ground
10	RXO3-	Negative Transmission data of Pixel 3 (ODD)	25	NC	No. Connection
11	RXO3+	Positive Transmission data of Pixel 3 (ODD)	26	NC	No. Connection
12	RXE0-	Negative Transmission data of Pixel 0 (EVEN)	27	NC	No. Connection
13	RXE0+	Positive Transmission data of Pixel 0 (EVEN)	28	VDD	Power Supply: +5V
14	GND	Power Ground	29	VDD	
15	RXE1-	Negative Transmission data of Pixel 1 (EVEN)	30	VDD	

Note : Pin 24 should be connected with GND.

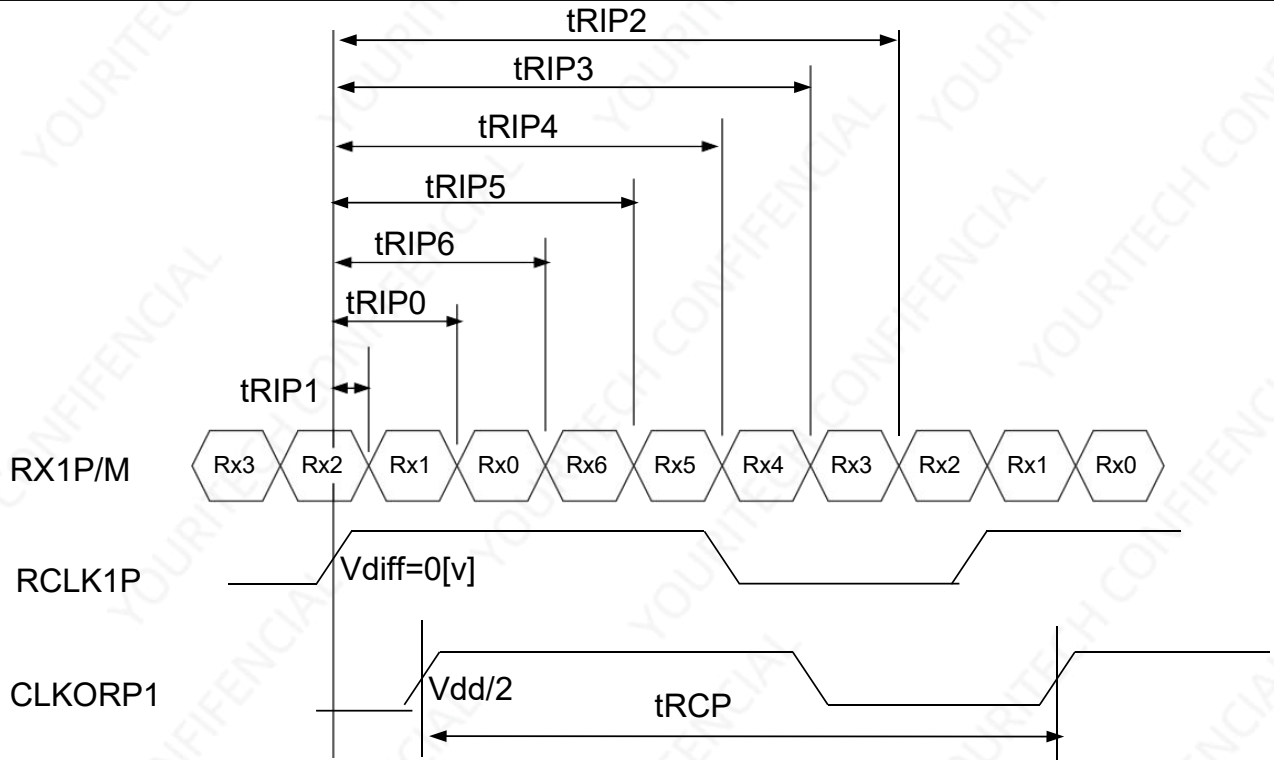


4.2 LVDS Rx Interface Timing Parameter

The specification of the LVDS Rx interface timing parameter is shown in Table 6.

<Table 6. LVDS Rx Interface Timing Specification>

Item	Symbol	Min	Typ	Max	Unit	Remark
CLKIN Period	tRCP	14.8	18.5	22.2	nsec	
Receiver Data Input Margin	tRMG	-0.35	-	0.35	nsec	fCLKIN=110MHz
		-0.40	-	0.40	nsec	fCLKIN=95MHz
		-0.45	-	0.45	nsec	fCLKIN=85MHz
		-0.60	-	0.60	nsec	fCLKIN=65MHz
Input Data 0	tRIP1	- tRMG	0.0	tRMG	Clock	
Input Data 1	tRIP0	T/7- tRMG	T/7	T/7+ tRMG	Clock	
Input Data 2	tRIP6	2 T/7- tRMG	2T/7	2T/7+ tRMG	Clock	
Input Data 3	tRIP5	3T/7- tRMG	3T/7	3T/7+ tRMG	Clock	
Input Data 4	tRIP4	4T/7- tRMG	4T/7	4T/7+ tRMG	Clock	
Input Data 5	tRIP3	5T/7- tRMG	5T/7	5T/7+ tRMG	Clock	
Input Data 6	tRIP2	6T/7- tRMG	6T/7	6T/7+ tRMG	Clock	



* $V_{diff} = (RXz+) - (RXz-), \dots, (RXCLK+) - (RXCLK-)$



5.0 SIGNAL TIMING SPECIFICATION

5.1 Timing Parameters (DE only mode)

< Table 8. Timing Table >

Item		Symbols	Min	Typ	Max	Unit
Clock	Frequency	1/Tc	60	74.25	78	MHz
	High Time	Tch	-	4/7Tc	-	
	Low Time	Tcl	-	3/7Tc	-	
Frame Period		Tv	1100	1125	1149	lines
			48.5	60	63	Hz
Horizontal Active Display Term	Valid	t _{HV}	-	960	-	t _{CLK}
	Total	t _{HP}	1060	1100	1200	t _{CLK}
Vertical Active Display Term	Valid	t _{VV}	-	1080	-	t _{HP}
	Total	t _{VP}	1100	1125	1149	t _{HP}

Notes: This product is DE only mode. The input of Hsync & Vsync signal does not have an effect on normal operation.

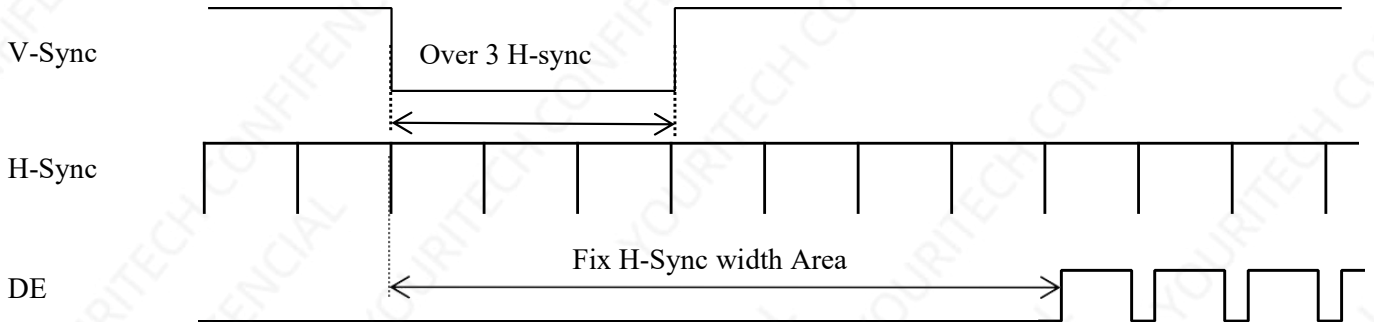
< Table 9. LVDS Input SSCG>

Symbol	Parameter	Condition	Min	Typ	Max	Unit
F	LVDS Input frequency	-	60	74.25	78	MHz
T _{LVSK}	LVDS channel to channel skew	F=100MHz V _{IC} =1.2V V _{ID} =±400mV	-380	-	+380	ps
F _{LVMOD}	Modulating frequency of input clock during SSC		60	-	85	KHz
F _{LVDEV}	Maximum deviation of input clock frequency during SSC		-3	-	+3	%
T _{CY-CY}	Cycle to Cycle jitter		-	-	100	ps



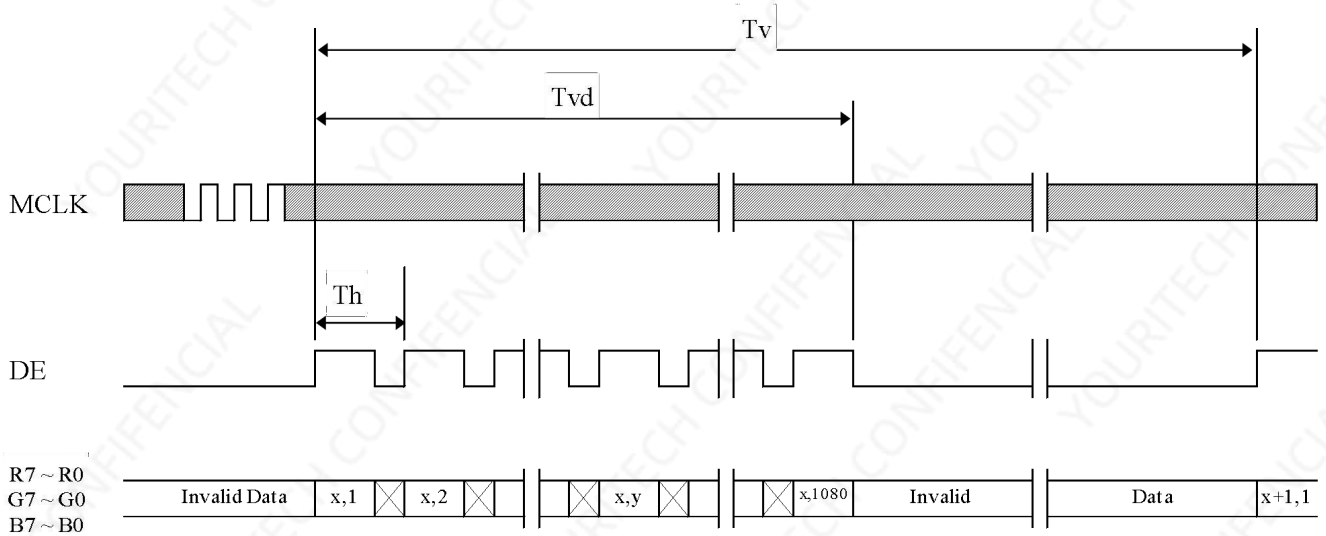
5.2 Signal Timing Waveform

5.2.1 Sync Timing Waveforms

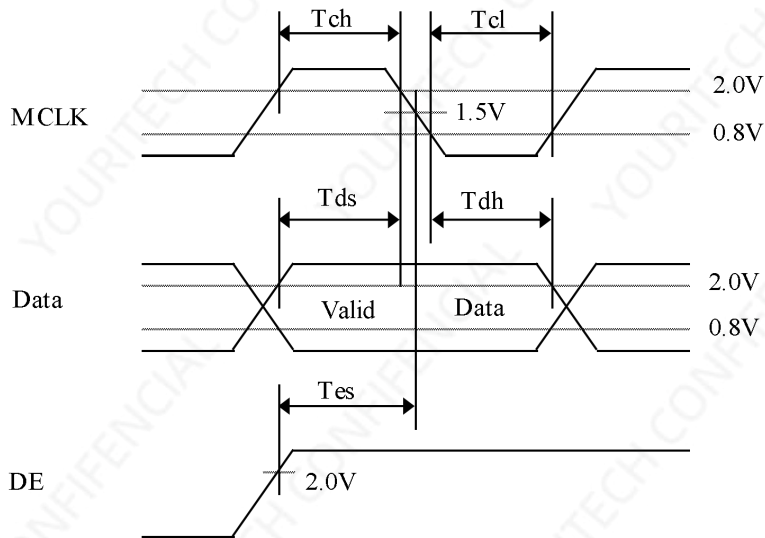
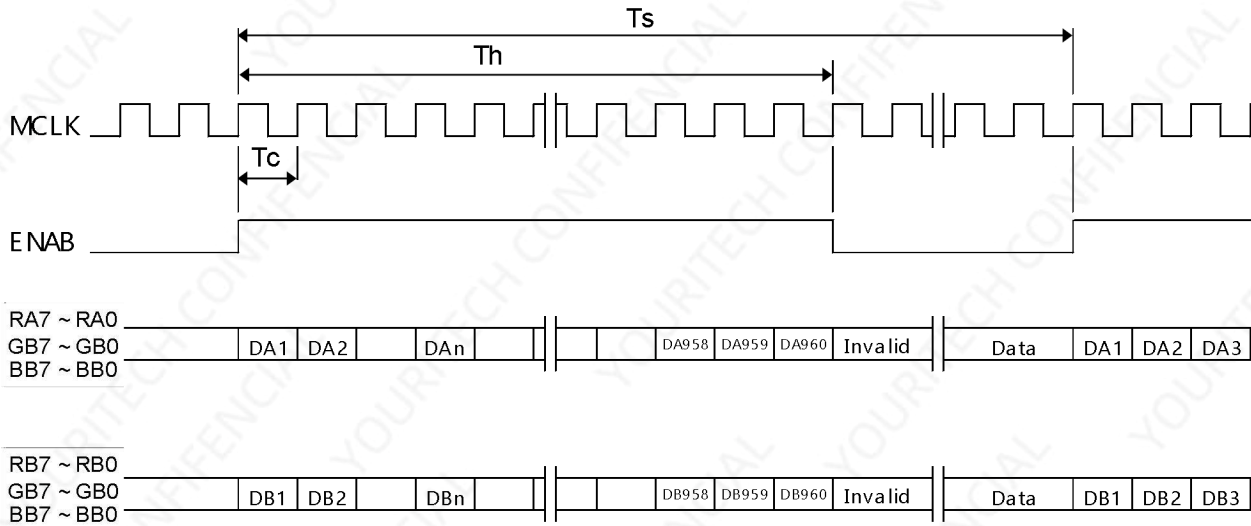


- 1) Need over 3 H-sync during V-Sync Low
- 2) Fix H-Sync width from V-Sync falling edge to first rising edge

5.2.2 Vertical Timing Waveforms

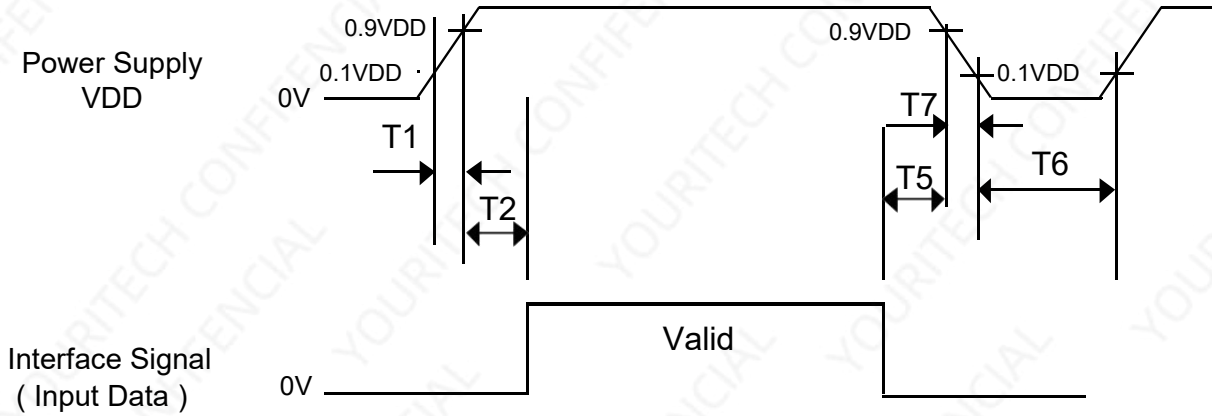


5.2.3 Horizontal Timing Waveforms



5.3 Power Sequence

To prevent a latch-up or DC operation of the Open Cell, the power on/off sequence shall be as shown in below



< Table 11. Sequence Table >

Parameter	Values			Units
	Min	Typ	Max	
T1	0.5	-	20	ms
T2	10	-	100	ms
T3	200	-	-	ms
T4	200	-	-	ms
T5	0	-	-	ms
T6	1	-	-	s

- Notes:
1. Back Light must be turn on after power for logic and interface signal are valid.
 2. Even though T1 is out of SPEC, it is still ok if the inrush current of VDD is below the limit.
 3. When $VDD < 0.9VDD(Typ.)$, Power off.
 4. T7 decreases smoothly, if there were rebounding voltage, it must smaller than 5 volts.



6.0 OPTICAL SPECIFICATIONS

The test of optical specifications shall be measured in a dark room (ambient luminance 1 lx and temperature=25±2°C) with the equipment of Luminance meter system (Goniometer system and PR730) and test unit shall be located at an approximate distance 180cm from the LCD surface at a viewing angle of θ and Φ equal to 0°. We refer to $\theta_{\Phi=0}$ ($=\theta_3$) as the 3 o'clock direction (the "right"), $\theta_{\Phi=90}$ ($=\theta_{12}$) as the 12 o'clock direction ("upward"), $\theta_{\Phi=180}$ ($=\theta_9$) as the 9 o'clock direction ("left") and $\theta_{\Phi=270}$ ($=\theta_6$) as the 6 o'clock direction ("bottom"). While scanning θ and/or Φ , the center of the measuring spot on the Display surface shall stay fixed. The measurement shall be executed after 30 minutes warm-up period. VDD shall be 12.0V at 25°C. Optimum viewing angle direction is 6 o'clock.

< Table 12. Optical Table >

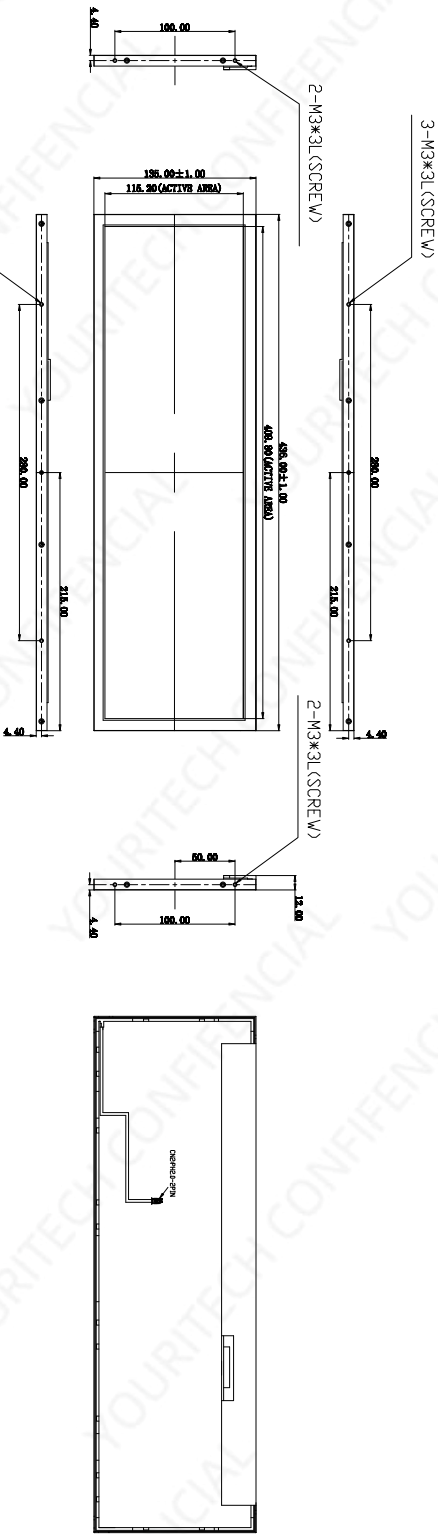
[VDD = 12.0V, Frame rate = 60Hz, Ta =25±2 °C]

Parameter		Symbol	Condition	Min	Typ	Max	Unit	Remark
Viewing Angle	Horizontal	Θ_3	CR > 10	80	89	-	Deg.	Note 1
		Θ_9		80	89	-	Deg.	
	Vertical	Θ_{12}		80	89	-	Deg.	
		Θ_6		80	89	-	Deg.	
Brightness		Lv	$\Theta = 0$ (Center) Normal Viewing Angle			-	nit	
Contrast ratio		CR		700:1	1000:1	-		Note 2
White luminance uniformity		ΔY		75	80	-	%	Note 3
Reproduction of color	White	W_x		TYP. - 0.03	TBD	TYP. + 0.03		Note 4
		W_y			TBD			
	Red	R_x			TBD			
		R_y			TBD			
	Green	G_x			TBD			
		G_y			TBD			
	Blue	B_x			TBD			
		B_y			TBD			
Color Gamut				68	72	-	%	
Cell Transmittance				TBD	TBD			
Response Time	G to G	T_g		-	14	20	ms	Note 5



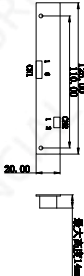
7、2D Drawing

标记	内容	日期	签名



恒流板

CN1: P22, 0-8PIN		CN2: P22, 0-8PIN	
NO.	Definition	NO.	Definition
1	VCC	1	V+
2	VCC	2	V-
3	N/F		
4	ADJ		
5	GND		
6	GND		



整机技术要求:

1. 整机表面整洁光滑, 不应有凹凸变形、粗糙不平、划伤、间隙、裂纹、毛刺、边缘棱角突出、霉斑、脏污、指纹、色差、螺丝孔堵塞、金属斑点、黑点、纹理等任何缺陷;
2. 所有五金件切口及螺丝沉头位置做防锈处理;
3. 所有装配螺丝孔牙长4.0±0.5mm;
4. 未注尺寸公差参照尺寸公差对应表;

设计			整机名称:	16.7吋液晶显示屏	型号	FD016711B00
审核			整机规格:	16.7吋	图号	
批准			单位	mm	比例	1:1
公差	0 ~ 30 ±0.50 30~100 ±0.80 >100 ±1.0 ANGLARE ± 0.3°					
A4	1/4 ANGLE PROJECTION					