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☑ **Tentative Specification**

☐ **Preliminary Specification**

☐ **Approval Specification**

MODEL NO.: ET240BA01-YU

SUFFIX: A

Approved by	Checked by	Prepaerd by	Customer Approved

Revise History

Version	Date	Description	Note
V0.1	2026/01/30	Draft	Initial version, not certified yet.

1. General Description

1.1 Overview

This specification applies to the Color TFT-LCD Module ET240BA01-YU. OC uses BOE, This LCD module has a TFT active matrix type liquid crystal panel 3840x720 pixels, and diagonal size of 24 inch.

1.2 Features

Model		ET240BA01-YU	Unit	Note
LCD	Type	24	inch	
	Display Area	596.74(H) x 111.87(V)	mm	
	Driver Element	a-Si TFT		
	Display Colors	16.7M	Colors	
	Number of Pixels	3840x720	Pixel	
	Pixel Pitch	-	mm	
	Viewing Angle	89/89/89/89		
	Contrast Ratio	1200:1		
	Response Time	14	ms	
	Backlight	LED		
	Brightness	700	nits	
	Aspect Ratio	16：3		
	Surface Treatment	Hard coating (3H)		Haze 25%
Power	Consumption	≤50	W	
Operation Conditions	OperatingTemperature	0 ~ 50	°C	
	Storage Temperature	-20 ~ 60	°C	
	Humidity	5% ~ 90%		
Dimensions (mm)		620(H) x138(V) x15.2(D)	mm	
Weight	Net	-	Kg	
	Gross	-	Kg	

2.0 ABSOLUTE MAXIMUM RATINGS

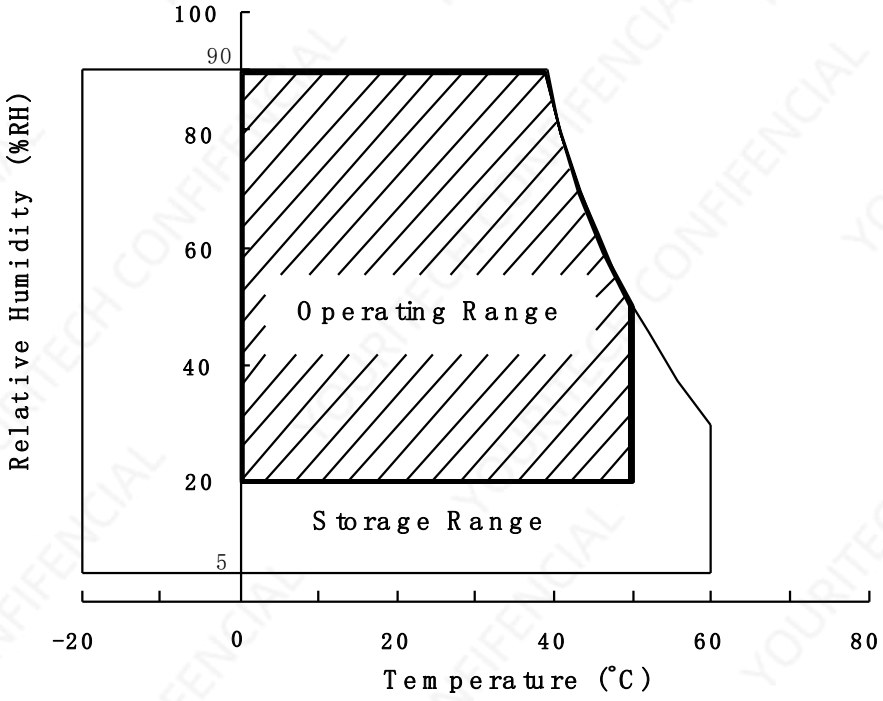
The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 2.

< Table 2. Absolute Maximum Ratings> [VSS=GND=0V]

Parameter	Symbol	Min.	Max.	Unit	Remarks
Power Supply Voltage	V_{DD}	GND-0.3	12	V	Ta = 25 ℃
Logic Supply Voltage	V_{IN}	VSS-0.3	V_{DD}+0.3	V	
Operating Temperature	T_{OP}	0	+50	℃	1)
Storage Temperature	T_{ST}	-20	+60	℃	1)
LCM Surface Temperature (Operation)	$T_{Surface}$	0	+65	℃	2)

Note : 1) Temperature and relative humidity range are shown in the figure below.
Wet bulb temperature should be 39 ^{O}C max. and no condensation of water.

2) Panel Surface Temperature should be Min. 0^{O}C and Max. +65^{O}C under the VDD = 10.0V, Frame rate = 60Hz,25^{O}C ambient Temp. no humidity control and LED string current is typical value.



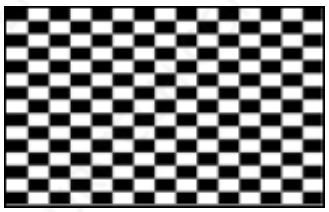
3.0 ELECTRICAL SPECIFICATIONS

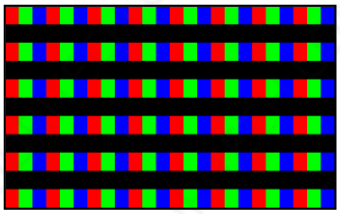
3.1Electrical Specifications

< Table 3. Open Cell Electrical specifications > [Ta =25±2 ℃]

Parameter		Min.	Typ.	Max.	Unit	Remarks
Power Supply Voltage	V_{DD}	9	10.0	11	V	Note1
Power Supply Current	I_{DD}	-	460	950	mA	
In-Rush Current	I_{RUSH}	-	2.0	3.0	A	Note 2
Permissible Input Ripple Voltage	V_{RF}	-	-	400	mV	Note1,3
High Level Differential Input Threshold Voltage	V_{IH}	-	-	+100	mV	
Low Level Differential Input Threshold Voltage	V_{IL}	-100	-	-	mV	
Differential input voltage	$\|V_{ID}\|$	100	-	600	mV	
Differential input common mode voltage	Vcm	0	-	2	V	V_{IH}=100mV, V_{IL}=-100mV
Power Consumption	P_D	-	4.6	9.5	W	

Notes : 1. The supply voltage is measured and specified at the interface connector of LCM.
The current draw and power consumption specified is for VDD=10.0V, Frame rate=60Hz
Test Pattern of power supply curren
a) Typ : Mosaic Pattern
b) Max : 1 line Inversion





2. Duration of rush current is about 2 ms and rising time of VDD is 520 μs ± 20 %
3. Ripple Voltage should be covered by Input voltage Spec.
4. Calculated value for reference (Input pins*VPIN ×IPIN) excluding inverter loss.

4.0 OPTICAL SPECIFICATION

4.1 Overview

The test of Optical specifications shall be measured in a dark room (ambient luminance ≤ 1 lux and temperature = 25±2℃) with the equipment of Luminance meter system (Goniometer system and TOPCONE PR730) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and Φ equal to 0°. We refer to $\theta_{Ø=0}$ (=θ_3) as the 3 o'clock direction (the "right"), $\theta_{Ø=90}$ (= θ_{12}) as the 12 o'clock direction ("upward"), $\theta_{Ø=180}$ (= θ_9) as the 9 o'clock direction ("left") and $\theta_{Ø=270}$(= θ_6) as the 6 o'clock direction ("bottom"). While scanning θ and/or Ø, the center of the measuring spot on the Display surface shall stay fixed. The measurement shall be executed after 30 minutes warm-up period. VDD shall be 5.0V +/-10% at 25°C. Optimum viewing angle direction is 6 'clock.

4.2 Optical Specifications

[VDD = 10.0V, Frame rate = 60Hz, Clock = 74.25MHz, I_{BL} = 360mA, Ta =25±2 ℃]

< Table 4. Module Optical >

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle range	Horizontal	Θ_3	CR > 10	85	89	-	Deg.	Note 1
		Θ_9		85	89	-	Deg.	
	Vertical	Θ_{12}		85	89	-	Deg.	
		Θ_6		85	89	-	Deg.	
Luminance Contrast ratio		CR	Θ = 0° (Center) Normal Viewing Angle	700	1000			Note 2
Transmittance		Tr		3.4	3.7	-	%	Note 3
White luminance uniformity		ΔY		75	80		%	Note 4
Reproduction of color	White	W_x		0.283	0.313	0.343	-	Note 5 (With BOE BLU)
		W_y		0.299	0.329	0.359	-	
	Red	R_x		0.622	0.652	0.682	-	
		R_y		0.303	0.333	0.363	-	
	Green	G_x		0.258	0.288	0.318	-	
		G_y		0.603	0.633	0.663	-	
	Blue	B_x		0.120	0.150	0.180	-	
		B_y		0.030	0.060	0.090	-	
Response Time	GTG	T_g			14	20	ms	Note 6
Cross Talk		CT		-	-	2.0	%	Note 7

Note :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface.
2. Contrast measurements shall be made at viewing angle of θ= 0° and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (See FIGURE 1 shown in Appendix) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Definition of Transmittance (T%) @BOE BLU:
   Module is with white(L255) signal input

$$\text{Transmittance} = \frac{\text{Luminance of LCD Module}}{\text{Luminance of BLU}} \times 100\ \%$$

3. The White luminance uniformity on LCD surface is then expressed as :
   ΔY = (Minimum Luminance of 9points / Maximum Luminance of 9points) * 100
   (See FIGURE 2 shown in Appendix).
5. The color chromaticity coordinates specified in Table 4. shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.
6. Response time Tg is the average time required for display transition by switching the input signal as below table and is based on Frame rate fV =60Hz to optimize.
   Each time in below table is defined as appendix Figure 3 and shall be measured by switching the input signal for "any level of gray(bright)"and "any level of gray(dark)"
7. Cross-Talk of one area of the LCD surface by another shall be measured by comparing the luminance (Y_A) of a 25mm diameter area, with all display pixels set to a gray level, to the luminance (Y_B) of that same area when any adjacent area is driven dark. (See FIGURE 4 shown in Appendix).

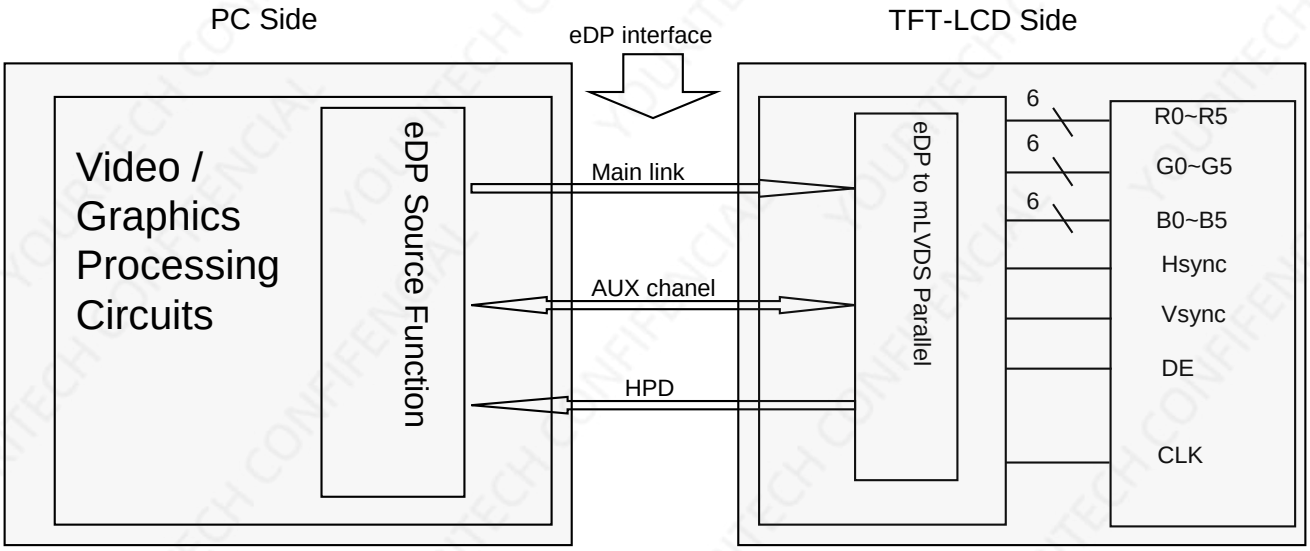
5.0 INTERFACE CONNECTION.

5.2 Electrical Interface Connection

- CN1 Module Side Connector : STM MSAK24025P30.

Pin No	Symbol	Function	Remark
1	VDD	Power Supply (10.0V)	
2	VDD	Power Supply (10.0V)	
3	VDD	Power Supply (10.0V)	
4	VDD	Power Supply (10.0V)	
5	VDD	Power Supply (10.0V)	
6	NC	No connection	
7	GND	Ground	
8	NC	No connection	
9	NC	No connection	
10	GND	Ground	
11	HPD	Hot Plug Detection Signal	
12	GND	Ground	
13	DAUXN	Negative Signal for Auxiliary Chanel	
14	DAUXP	Positive Signal for Auxiliary Chanel	
15	GND	Ground	
16	DRX0P	Positive Signal For eDP Lane0	
17	DRX0N	Negative Signal For eDP Lane0	
18	GND	Ground	
19	DRX1P	Positive Signal For eDP Lane1	
20	DRX1N	Negative Signal For eDP Lane1	
21	GND	Ground	
22	DRX2P	Positive Signal For eDP Lane2	
23	DRX2N	Negative Signal For eDP Lane2	
24	GND	Ground	
25	DRX3P	Positive Signal For eDP Lane3	
26	DRX3N	Negative Signal For eDP Lane3	
27	GND	Ground	
28	GND	Ground	
29	NC	No connection	
30	GND	Ground	BIST

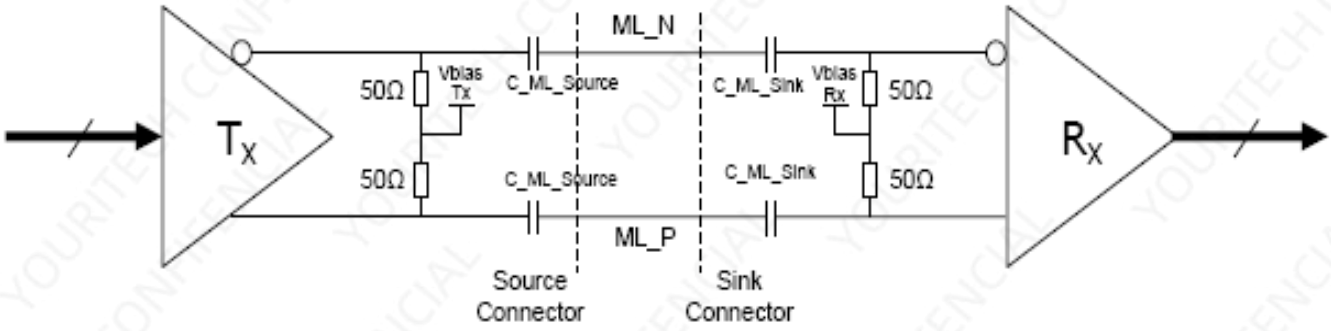
5.3.eDP Interface



Note. Transmitter : Parade DP501or equivalent.

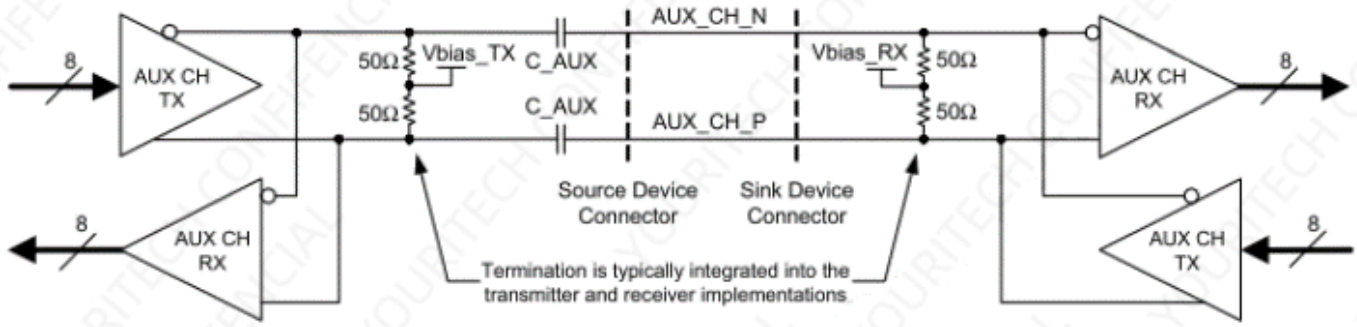
Transmitter is not contained in Module.

5.3.1 eDP Main Link Signal



Parameter	Symbol	Min	Typ	Max	Uint	Notes
Unit Interval for high bit rate (5.4Gbps/lane)	UI_HBR2	-	185	-	ps	
Link Clock Down Spreading	Amplitude	0	-	0.5	%	
	Frequency	30		33	kHz	
Differential peak-to-peak voltage at Sink side connector	$V_{RX-DIFFP-P}$	-	-	1.38	V	
EYE width at Sink side connector	$T_{RX-EYE-CONN}$	0.38	-	-	UI	
Lane-to-Lane skew	$L_{Rx-SKEW-INTER\_PAIR}$	-	-	4UI+ 500ps		
Lane intra-pair skew	$L_{Rx-SKEW-INTER\_PAIR}$	-	-	50	ps	
AC Coupling Capacitor	C_{SOURCE_ML}	75		200	nF	Source side

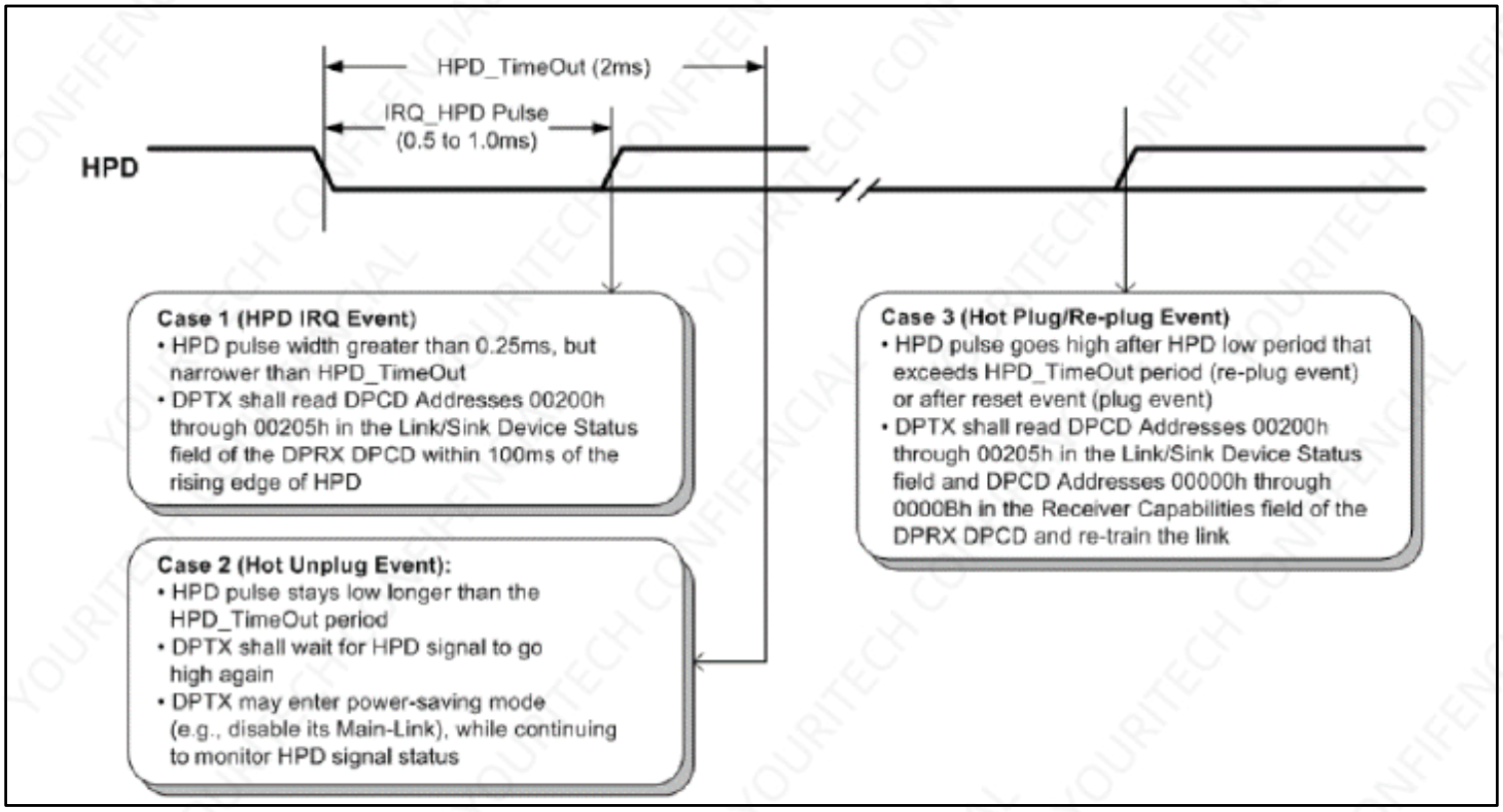
5.4 eDP AUX Channel Signal



Recommended eDP AUX Channel Differential Pair

Parameter	Symbol	Min	Typ	Max	Unit	Notes
AUX Unit Interval	UI	0.4	-	0.6	us	
AUX Jitter at Tx IC Package Pins	T_{jitter}	-	-	0.04	UI	
AUX Jitter at Rx IC Package Pins		-	-	0.05	UI	
AUX Peak-to-peak voltage at Connector Pins of Receiving	$V_{AUX-DIFFP-P}$	0.27	-	1.36	V	
AUX Peak-to-peak voltage at Connector Pins of Transmitting		0.29	-	1.38	V	
AUX EYE Width at Connector Pins of Tx and Rx		0.98	-	-	UI	
AUX DC common mode voltage	V_{AUX-CM_RX}	0	-	1.2	V	
	V_{AUX-CM_TX}	0	-	1.2	V	
AUX AC Coupling Capacitor	$C_{SOURCE-AUX}$	75	-	200	nF	

5.5 eDP HPD Signal



Parameter	Symbol	Min	Typ	Max	Unit	Notes
HPD Voltage	HPD	2.25	-	3.6	V	Sink side Driving
HOT Plug Detection Threshold		2.0	-	-	V	Source side Detecting
HOT Unplug Detection Threshold		-	-	0.8	V	
HPD_IRQ Pulse Width	HPD_IRQ	0.5	-	1.0	ms	
HPD_TimeOut		2.0	-	-	ms	HPD Unplug Event

6.0 SIGNAL TIMING SPECIFICATION

6.1 The MV270QUB-N50 is operated by the DE only.

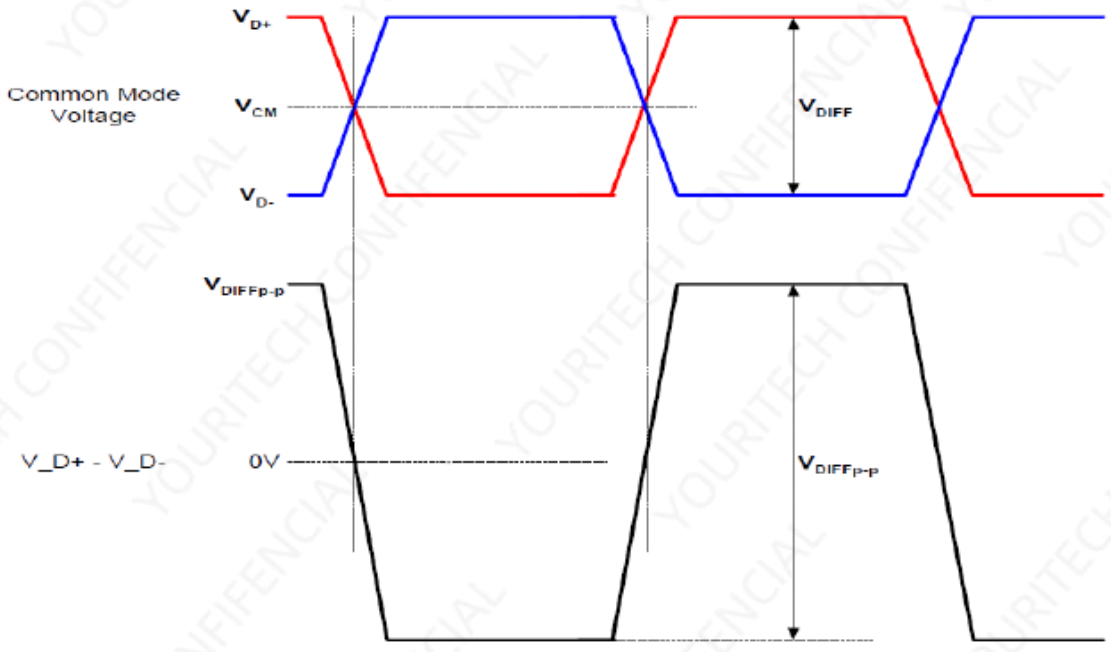
Item		Symbol	Min	Typ	Max	Unit	Note
DCLK	Period	tCLK	1.8	1.9	2.2	ns	
	Frequency	fCLK	444	533	551	MHz	
Hsync	Period	tHP	3950	4000	4088	tCLK	
	Width-Active	tWH	18	28	36		
Vsync	Period	tVP	2213	2222	2290	tHP	
	Frequency	fv	50	60	62	HZ	Adaptive Sync :40~60Hz
	Width-Active	tWV	6	8	12	tHP	
Data Eenlabe	Horizontal valld	tHV	3840	3840	3840	tCLK	
	Horizontal Back Porch	tHBP	32	54	112		
	Horizontal Front Porch	tHFP	60	78	100		
	Horizontal Blank	-	110	160	248		tWH+tHBP+tHFP
	Vertial valld	tVV	2160	2160	2160	tHP	
	Vertial Back Porch	tVBP	5	7	18		
	Vertial Front Porch	t_{VFP}	42	47	100		
	Vertial Blank	-	53	62	130		$t_{WV}+t_{VBP}+t_{VFP}$

6.2 eDP Rx Interface Timing Parameter

The specification of the eDP Rx interface timing parameter is shown in Table 5.

<Table 5. eDP Rx Interface Timing Specification>

Item	Symbol	Min	Typ	Max	Unit	Remark
Spread spectrum clock	ssc	0	-	0.5	%	
Differential peak-to-peak input voltage at package pins	$V_{RX-DIFFp-p}$	-	-	1.38	V	
Rx input DC common mode voltage	$V_{RX\_DC\_CM}$	-	GND	-	V	
Differential termination resistance	$R_{RX-DIFF}$	80	-	100	Ω	
Single-ended termination resistance	R_{RX-SE}	40	-	60	Ω	
Rx short circuit current limit	I_{RX_SHORT}	-	-	20	mA	
Intra-pair skew at Rx package pins (HBR) RX intra-pair skew tolerance at HBR	$L_{RX\_SKEW\_INTRA\_PAIR}$	-	-	150	ps	



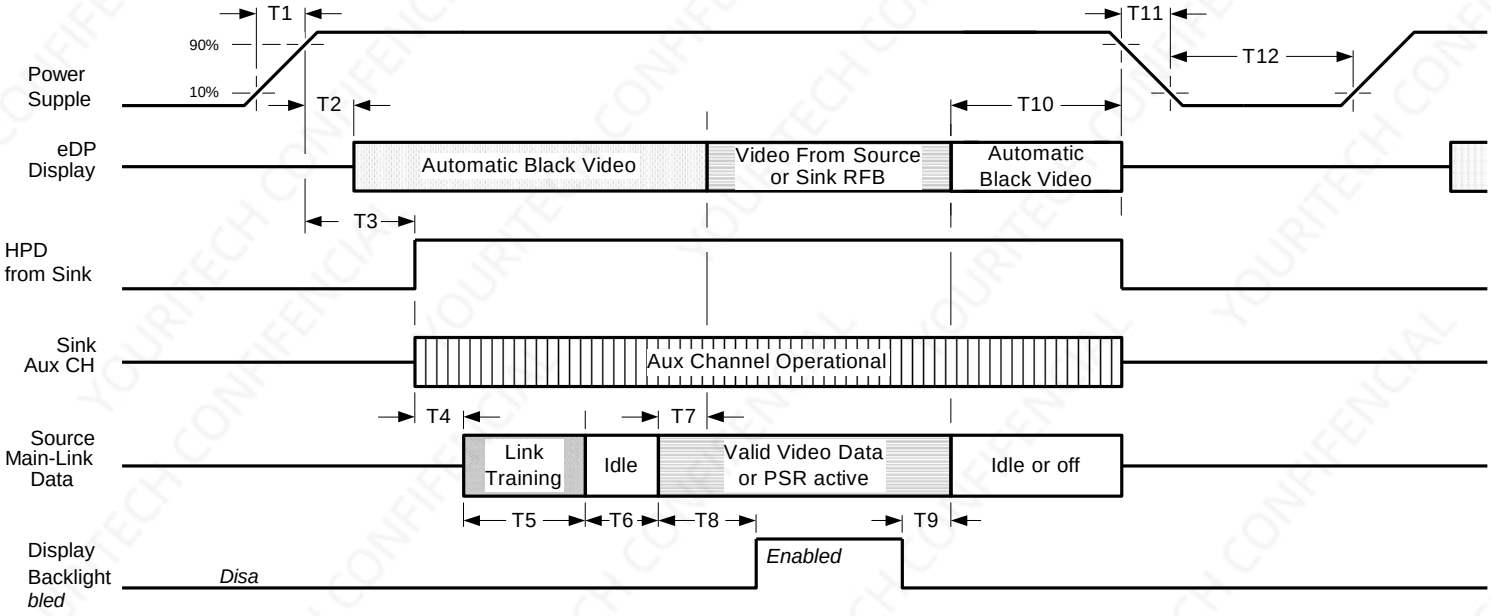
* Vdiff = (RXz+)-(RXz-),…. ,(RXCLK+)-(RXCLK-)

7.0 INPUT SIGNALS, BASIC DISPLAY COLORS & GRAY SCALE OF COLORS

Color & Gray Scale		RED DATA								GREEN DATA								BLUE DATA							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale of RED	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	↑								↑								↑							
	▽	↓								↓								↓							
	Brighter	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	▽	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of GREEN	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	△	↑								↑								↑							
	▽	↓								↓								↓							
	Brighter	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	▽	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale of BLUE	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	△	↑								↑								↑							
	▽	↓								↓								↓							
	Brighter	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	▽	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Gray Scale of WHITE	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
	Darker	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
	△	↑								↑								↑							
	▽	↓								↓								↓							
	Brighter	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1
	▽	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

8.0 POWER SEQUENCE

To prevent a latch-up or DC operation of the LCD module, the power on/off sequence shall be as shown in below



Timing Parameter	Description	Required By	Limits		Notes
			Min	Max	
T1	Power rail rise time, 10% to 90%	Source	0.5ms	10ms	
T2	Delay from Power Supple to automatic Black Video generation	Sink	0ms	200ms	Automatic Black Video generation prevents display noise until valid video data is received from the Source
T3	Delay from Power Supple to HPD high	Sink	0ms	200ms	Sink AUX Channel must be operational upon HPD high
T4	Delay from HPD high to link training initialization	Source	-	-	Allows for the Source to read Link capability and initialize
T5	Link training duration	Source	-	-	Dependant on the Source link training protocol
T6	Link idle	Source	-	-	Min accounts for required BS-Idle Pattern. Max allows for Source frame synchronization.

8.0 POWER SEQUENCE

T7	Delay from valid video data from Source to video on display	Sink	0ms	50ms	Max value allows for the Sink to validate video data and timing. At the end of T7, the Sink will indicate the detection of valid video data by setting the SINK_STATUS bit to logic 1 (DPCD 00205h, bit 0), and the Sink will no longer generate automatic Black Video.
T8	Delay from valid video data from Source to backlight enable	Source	-	-	The Source must assure display video is stable
T9	Delay from backlight disable to end of valid video data	Source	-	-	The Source must assure backlight is no longer illuminated. At the end of T9, the Sink will indicate the detection of no valid video data by setting the SINK_STATUS bit to logic 0 (DPCD 00205h, bit 0), and the Sink will automatically display Black Video.
T10	Delay from end of valid video data from Source to power off	Source	0ms	500ms	
T12	Power off time	Source	500ms	-	

Notes:

1. When the power supply VDD is 0V, keep the level of input signals on the low or keep high impedance.
2. Do not keep the interface signal high impedance when power is on.
3. Back Light must be turn on after power for logic and interface signal are valid.

9.0 MECHANICAL CHARACTERISTICS

9.1 Dimensional Requirements

FIGURE 5 (located in Appendix) shows mechanical outlines for the MV270QUB-N50.
Other parameters are shown in Table 6.

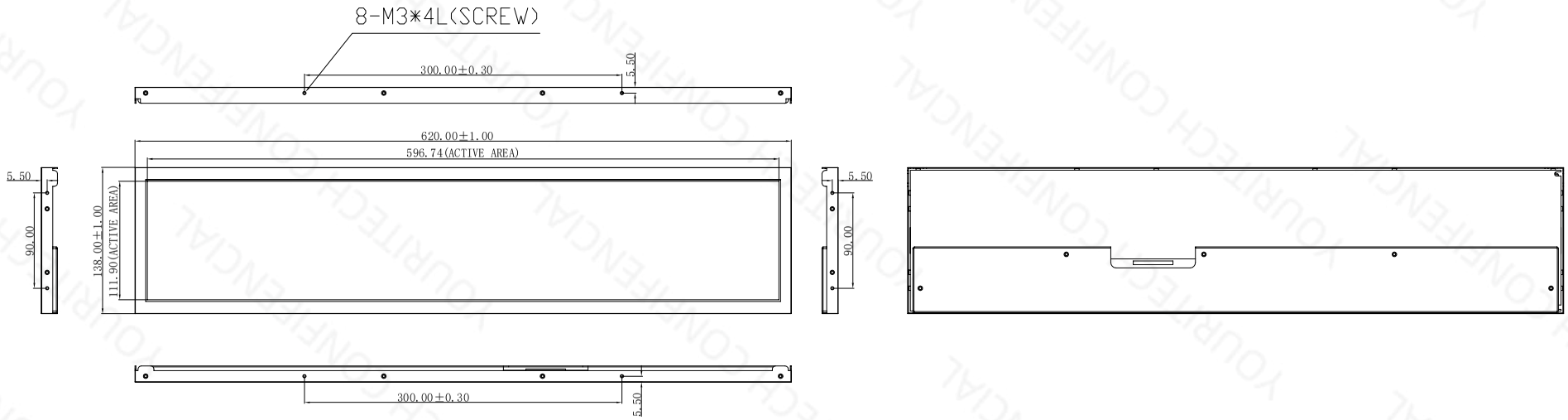
<Table 6. Dimensional Parameters>

Parameter	Specification	Unit
Dimensional outline	620(H) × 138(V) × 15.2(Depth) (typ.)	mm
Weight	TBD	gram
Active area	596.74(H) × 111.87 (V)	mm
Pixel pitch	0.1554 (H) × 0.1554(V)	mm
Number of pixels	3840(H)×720 (V) (1 pixel = R + G + B dots)	pixels

9.2 Anti-Glare and Polarizer Hardness.

The surface of the LCD has an anti-glare coating to minimize reflection and a coating to reduce scratching.

标记	内容	日期	签名



整机技术要求：

1. 整机表面整洁光滑，不应有凹凸变形、粗糙不平、划伤、间隙、裂纹、毛刺、边缘棱角突出、霉斑、脏污、指纹、色差、螺丝孔堵塞、金属斑点、黑点、纹理等任何缺陷；
2. 所有五金件切口及螺丝沉头位置做防锈处理；
3. 所有装配螺丝孔牙长4.0±0.5mm；
4. 未注尺寸公差参照尺寸公差对应表；

设 计			整机名称:	24吋条形液晶显示屏	型号	ET240BA01-YU
审 核			整机规格:	24吋	图号	LCDF24002
核 准			单位	mm	比 例	1:1
公 差	0 ~ 30 ±0.50 >30~100 ±0.80					
	>100 ±1.0 ANGULAR± 0.3°					
A4	1rd ANGLE PROJECTION					