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Project No. 项目编号	**ET320FH02-T**
Customer 客户名称	
Module No. 客户型号	
Product type 产品内容	**Standard LCD Module** **TFT：1920*RGBx1080Dots** **32.0"TFT LCD**

客户确认Customer Approval	
项目负责人Project Manager	
品质主管Director of Quality	
采购工程师Purchasing Engineer	

PREPARED BY	CHECKED BY	APPROVED BY

REVISION HISTORY

Version	Date	Page	Description
1.0	2023/08/25	All	First release

1. GENERAL DESCRIPTION

1.1 OVERVIEW

This specification applies to the 32 inch Color TFT-LCD Module 32011. This LCD module has a TFT active matrix type liquid crystal panel 1920x1080 pixels, and diagonal size of 32 inch. This module supports 1920x1080 mode.

Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the brightness of the sub-pixel color is determined with a 8-bit gray scale signal for each dot. The 32011 has been designed to apply the 8-bit 2 channel LVDS interface method. It is intended to support displays where high brightness, wide viewing angle, high color saturation, and high color depth are very important.

1.2 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Screen Size	32	Inch	-
Driver Element	a-Si TFT active matrix	-	-
Pixel Number	1920 x 1080	Pixel	
Pixel pitch	0.36375(H) x 0.36375 (W)	mm	
Active Area	698.4(H) x 392.85(V)	mm	
Display Colors	8bit / 16.7 millions	Color	
Transmissive Mode	Normally Black	-	
Surface Treatment	Anti-Glare, 3H	-	
Luminance, White	1000	cd/m2	
Color Gamut	/	-	
Power Consumption	Total 45.76W @ cell 4W , BL 41.76W		

2. MECHANICAL SPECIFICATIONS

Item		Min	Typ.	Max	Unit	Note
Module Size	Horizontal(H)		725.2		mm	(1)
	Vertical (V)		422.7		mm	
	Thickness (T)		14.4		mm	
Bezel Area	Horizontal		701.71		mm	
	Vertical		396.63		mm	
Active Area	Horizontal	-	698.4	-	mm	
	Vertical	-	392.85	-	mm	
Weight		-	/		Kg	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

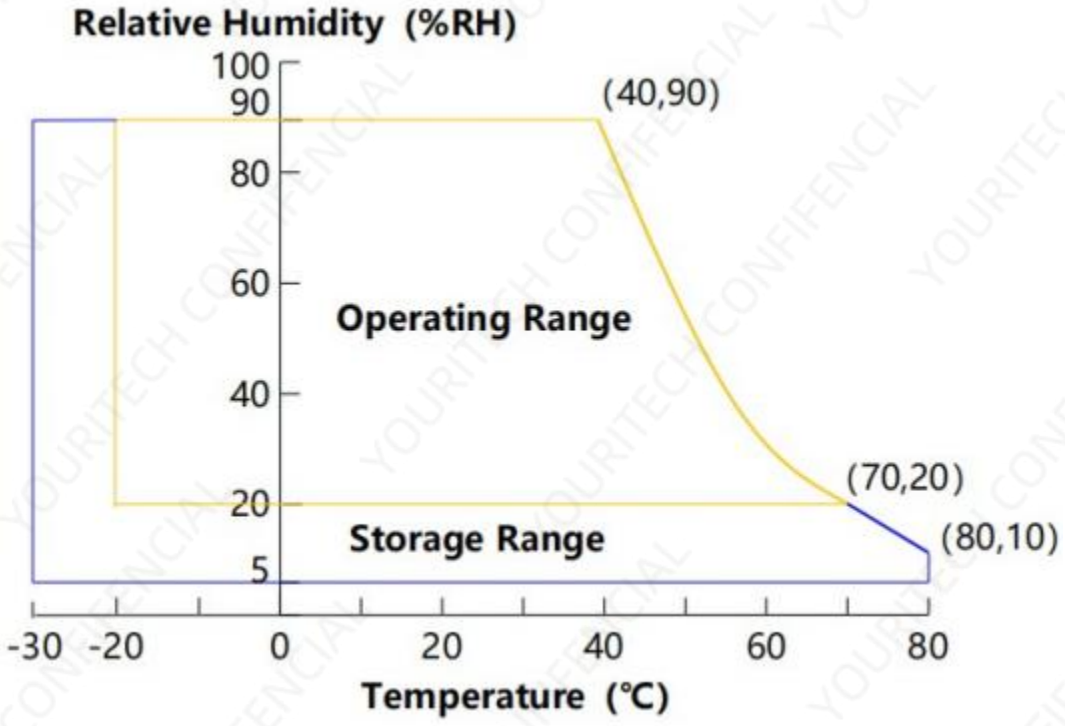
3. ABSOLUTE MAXIMUM RATINGS

3.1 ABSOLUTE RATINGS OF ENVIRONMENT

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in.

Parameter	Symbol	Min.	Max.	Unit	Remark
Power Supply Voltage	VDD	VSS-0.3	13.5	V	Ta = 25 ℃
Operating Temperature	T_{OP}	-20	+70	℃	Note 1
Storage Temperature	T_{SUR}	-20	+70	℃	
	T_{ST}	-20	+70	℃	
Operating Ambient Humidity	Hop	10	80	%RH	
Storage Humidity	Hst	10	80	%RH	

Note 1 : Temperature and relative humidity range are shown in the figure below.
Wet bulb temperature should be 39 ℃ max. and no condensation of water.



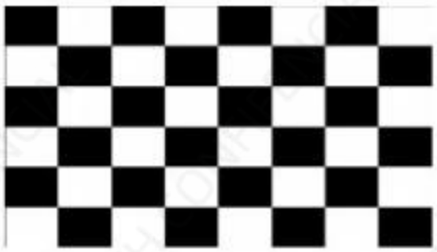
4. ELECTRICAL SPECIFICATIONS

4.1 TFT LCD Open Cell

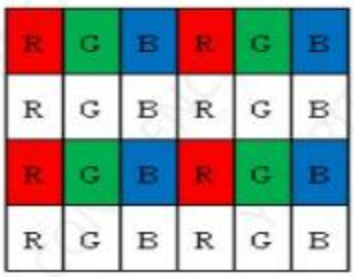
Parameter		Symbol	Values			Unit	Remark
			Min	Typ	Max		
Power Supply Input Voltage		VDD	10.8	12	14	Vdc	
Power Supply Ripple Voltage		VRP			300	mV	
Power Supply Current		IDD	-	333	630	mA	Note 1
Power Consumption		PDD		4.0	7.6	Watt	
Rush current		IRUSH	-	-	3.3	A	Note 2
LVDS Interface	LVDS Swing Voltage	VID	±100		±300	mV	Note 3
	Common Input Voltage	VLVC	1.0	1.2	1.4	V	
CMOS Interface	Input High Threshold Voltage	VIH	2.7	-	3.3	V	
	Input Low Threshold Voltage	VIL	0	-	0.6	V	

Note 1 : The supply voltage is measured and specified at the interface connector of LCM.
The current draw and power consumption specified is for VDD=12.0V,
Frame rate f_V=60Hz and Clock frequency = 75.4MHz.
Test Pattern of power supply current

a) Typ : Mosaic 8 x 6 Pattern(L0/L255)
Pattern(L0/L255)



b) Max : H- Stripe



Note 2 : The duration of rush current is about 2ms and rising time of Power Input is 1ms(min)
Note 3 : The LVDS test point is at each terminal resistor

4.2 PIN ASSIGNMENT

Pin No	Symbol	Description	Pin No	Symbol	Description
1	NC	No Connection	21	GND	Ground
2	SDA	I²C Data	22	CH1[3]-	First pixel negative LVDS differential data input. Pair3
3	SCL	I²C Clock	23	CH1[3]+	First pixel positive LVDS differential data input. Pair3
4	NC	Not Connected	24	NC	Not Connected
5	NC	Not Connected	25	NC	Not Connected
6	NC	Not Connected	26	NC or GND	Not Connected
7	SELLVDS	High: JEIDA Low or Open: VESA	27	NC	Not Connected
8	NC	Not Connected	28	CH2[0]-	Second pixel negative LVDS differential data input. Pair0
9	NC	Not Connected	29	CH2[0]+	Second pixel positive LVDS differential data input. Pair0
10	NC	Not Connected	30	CH2[1]-	Second pixel negative LVDS differential data input. Pair1
11	GND	Ground	31	CH2[1]+	Second pixel positive LVDS differential data input. Pair1
12	CH1[0]-	First pixel negative LVDS differential data input. Pair0	32	CH2[2]-	Second pixel negative LVDS differential data input. Pair2
13	CH1[0]+	First pixel positive LVDS differential data input. Pair0	33	CH2[2]+	Second pixel positive LVDS differential data input. Pair2
14	CH1[1]-	First pixel negative LVDS differential data input. Pair1	34	GND	Ground
15	CH1[1]+	First pixel positive LVDS differential data input. Pair1	35	CH2CLK-	Second pixel negative LVDS clock
16	CH1[2]-	First pixel negative LVDS differential data input. Pair2	36	CH2CLK+	Second pixel positive LVDS clock
17	CH1[2]+	First pixel positive LVDS differential data input. Pair2	37	GND	Ground
18	GND	Ground	38	CH2[3]-	Second pixel negative LVDS differential data input. Pair3
19	CH1CLK-	First pixel negative LVDS clock	39	CH2[3]+	Second pixel positive LVDS differential data input. Pair3
20	CH1CLK+	First pixel positive LVDS clock			

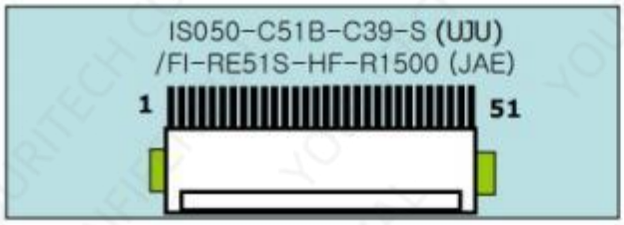
Pin No	Symbol	Description	Pin No	Symbol	Description
40	NC	Not Connected	46	GND	Ground
41	NC	Not Connected	47	NC	Not Connected
42	NC or GND	Not Connected	48	VCC	Input Voltage +12V
43	NC or GND	Not Connected	49	VCC	Input Voltage +12V
44	NC or GND	Ground	50	VCC	Input Voltage +12V
45	GND	Ground	51	VCC	Input Voltage +12V

Module Panel Connector Information

Item	Description
Manufacturer	/
Type part number	/
Mating housing part number	FI-RE51S-HF-R1500 (JAE)

Notes : 1. NC(Not Connected) : This pins are only used for BOE internal operations.
2. Input Level of LVDS signal is based on the IEA 664 Standard.
3. LVDS_SEL : This pin is used for selecting LVDS signal data format.
If this Pin : High (3.3V) →JEIDA LVDS format
Otherwise : Low (GND) or Open (NC) → Normal NS LVDS format

Rear view of LCM



BIST Pattern

4.3 LVDS Interface

LVDS Receiver : Timing Controller (LVDS Rx merged) / LVDS Data : Pixel Data

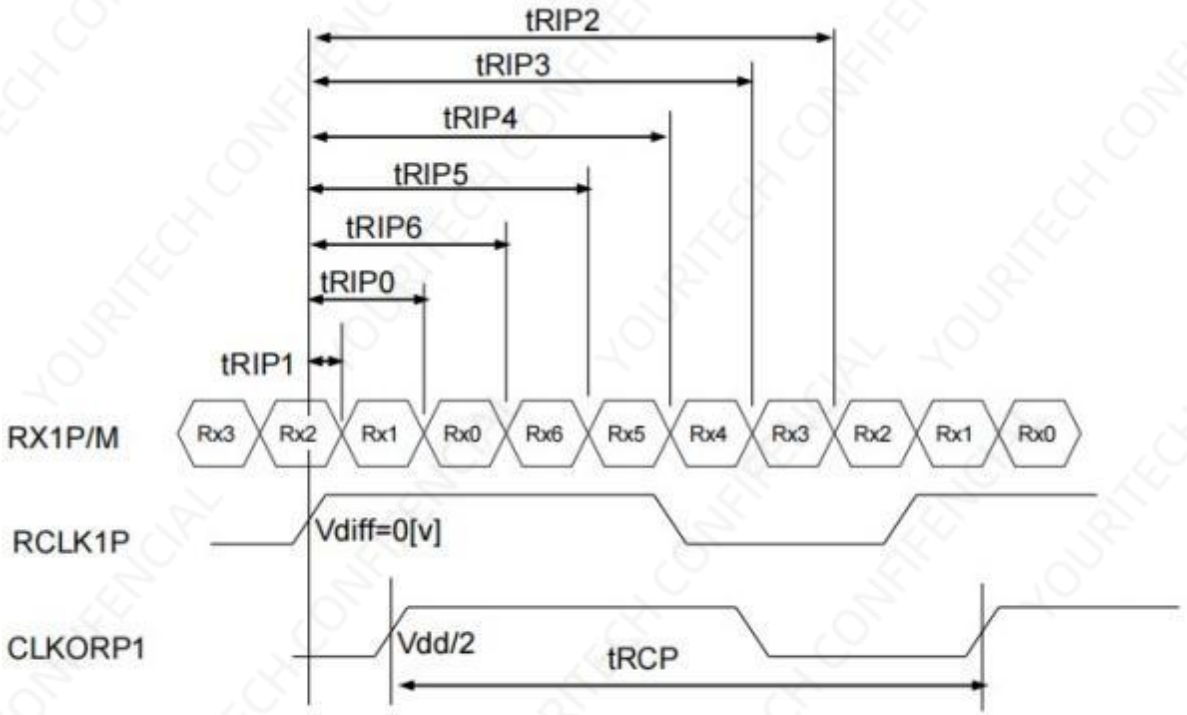
< Open Cell Input Connector Pin Configuration >

Channel No.	Data No.	8-bit LVDS Type	
		NS	JEIDA
0	Bit-0	R0	R2
	Bit-1	R1	R3
	Bit-2	R2	R4
	Bit-3	R3	R5
	Bit-4	R4	R6
	Bit-5	R5	R7
	Bit-6	G0	G2
1	Bit-0	G1	G3
	Bit-1	G2	G4
	Bit-2	G3	G5
	Bit-3	G4	G6
	Bit-4	G5	G7
	Bit-5	B0	B2
	Bit-6	B1	B3
2	Bit-0	B2	B4
	Bit-1	B3	B5
	Bit-2	B4	B6
	Bit-3	B5	B7
	Bit-4	HS	HS
	Bit-5	VS	VS
	Bit-6	DE	DE
3	Bit-0	R6	R0
	Bit-1	R7	R1
	Bit-2	G6	G0
	Bit-3	G7	G1
	Bit-4	B6	B0
	Bit-5	B7	B1
	Bit-6	-	

4.4 LVDS Rx Interface Timing Parameter

The specification of the LVDS Rx interface timing parameter is shown in < LVDS Rx Interface Timing Specification>

Item	Symbol	Min	Typ	Max	Unit	Remark
CLKIN Period	tRCP	9.09	T	25	nsec	
Receiver Data Input Margin	tRMG	-0.40	-	0.40	nsec	fCLKIN=65MHz
Input Data 0	tRIP1	- | tRMG |	0.0	| tRMG |	Clock	
Input Data 1	tRIP0	T/7- | tRMG |	T/7	T/7+ | tRMG |	Clock	
Input Data 2	tRIP6	2 T/7- | tRMG |	2T/7	2T/7+ | tRMG |	Clock	
Input Data 3	tRIP5	3T/7- | tRMG |	3T/7	3T/7+ | tRMG |	Clock	
Input Data 4	tRIP4	4T/7- | tRMG |	4T/7	4T/7+ | tRMG |	Clock	
Input Data 5	tRIP3	5T/7- | tRMG |	5T/7	5T/7+ | tRMG |	Clock	
Input Data 6	tRIP2	6T/7- | tRMG |	6T/7	6T/7+ | tRMG |	Clock	

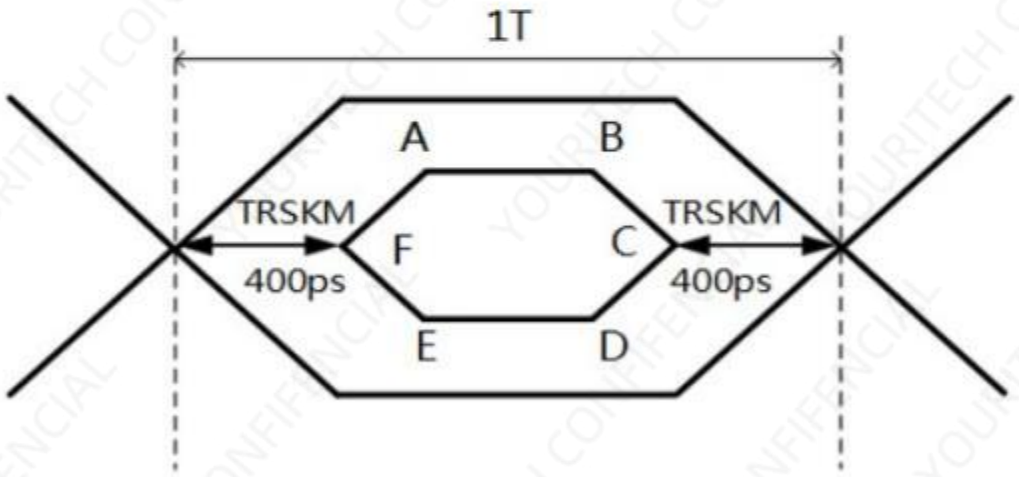


* Vdiff = (RXz+)-(RXz-),.... ,(RXCLK+)-(RXCLK-)

4.5 LVDS Rx Interface Eye Diagram

< LVDS Rx Interface Eye Diagram>

Symbol	Min	Typ	Max	Unit	Note
A	—	150	—	mV	
B	—	150	—	mV	
C	—	0	—	mV	
D	—	-150	—	mV	
E	—	-150	—	mV	
F	—	0	—	mV	

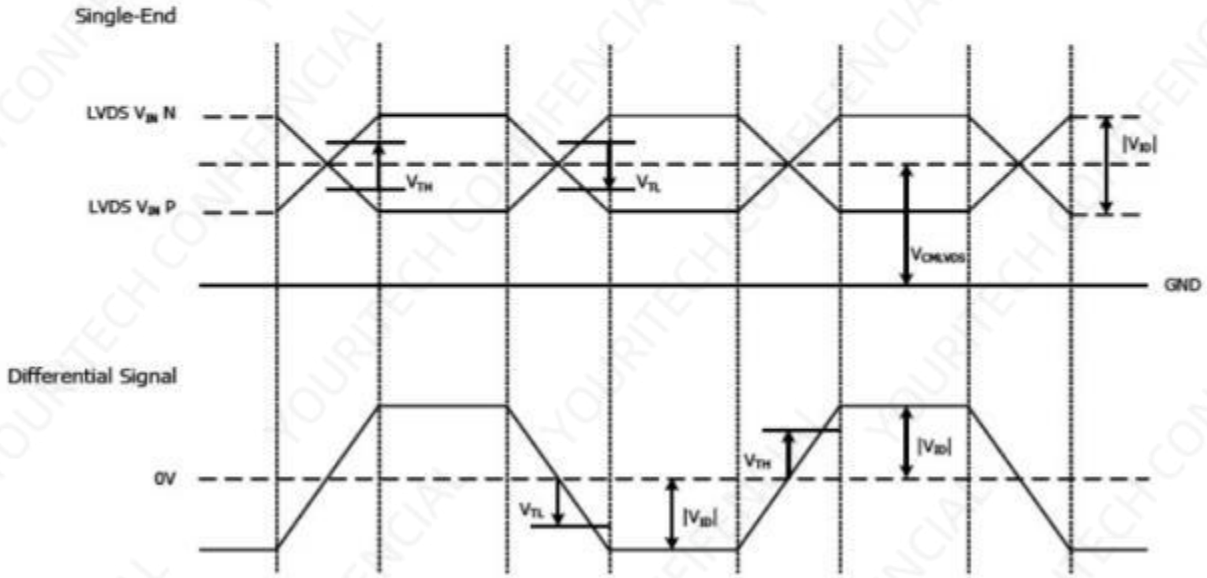


Notes: 1. Time F to A,B to C,C to D,E to F is 150p second.
2. LVDS clock=85Mhz.
3. The time A to B=1T-2*TRSKM-2*150ps.

4.6 LVDS Receiver Differential Input

< LVDS Receiver Differential Input>

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
LVDS Input High Threshold	V_{TH}	V_{CMLVDS} = 1.2V			+100	mV
LVDS Input Low Threshold	V_{TL}	V_{CMLVDS} = 1.2V	-100			mV
Single-End Input Voltage Range	V_{IN}		0		VCC_LVDS	V
LVDS Input Common Mode Voltage	V_{CMLVDS}			1.2	VCC_LVDS-0.4-|VID|/2	V
Differential Input Voltage	$\|V_{ID}\|$		100		600	mV
Input Leakage Current	IN		-10		+10	μA



5. SIGNAL TIMING SPECIFICATION

5.1 Timing Parameters (DE only mode)

< Timing Table >

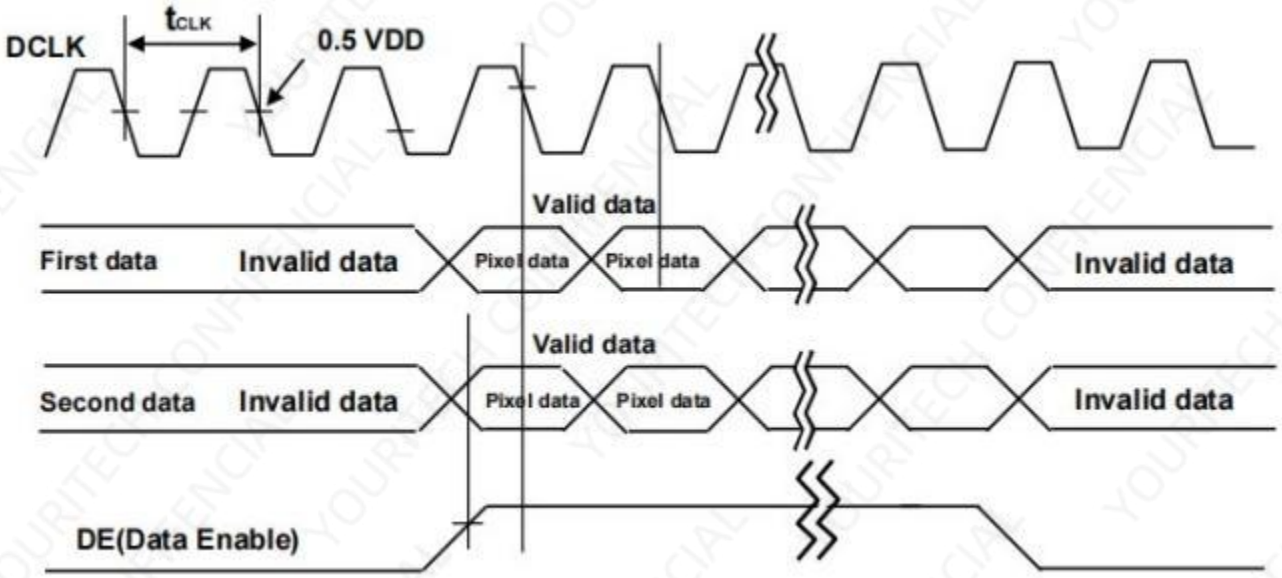
Item		Symbols		Min	Typ	Max	Unit
Clock	Frequency	1/Tc		60	74.25	78	MHz
	High Time	Tch		-	4/7Tc	-	
	Low Time	Tcl		-	3/7Tc	-	
Frame Period		Tv		1100	1125	1149	lines
				48.5	60	63	Hz
Horizontal Active Display Term		Valid	t_{HV}	-	960	-	t_{CLK}
		Total	t_{HP}	1060	1100	1200	t_{CLK}
Vertical Active Display Term		Valid	t_{VV}	-	1080	-	t_{HP}
		Total	t_{VP}	1100	1125	1149	t_{HP}

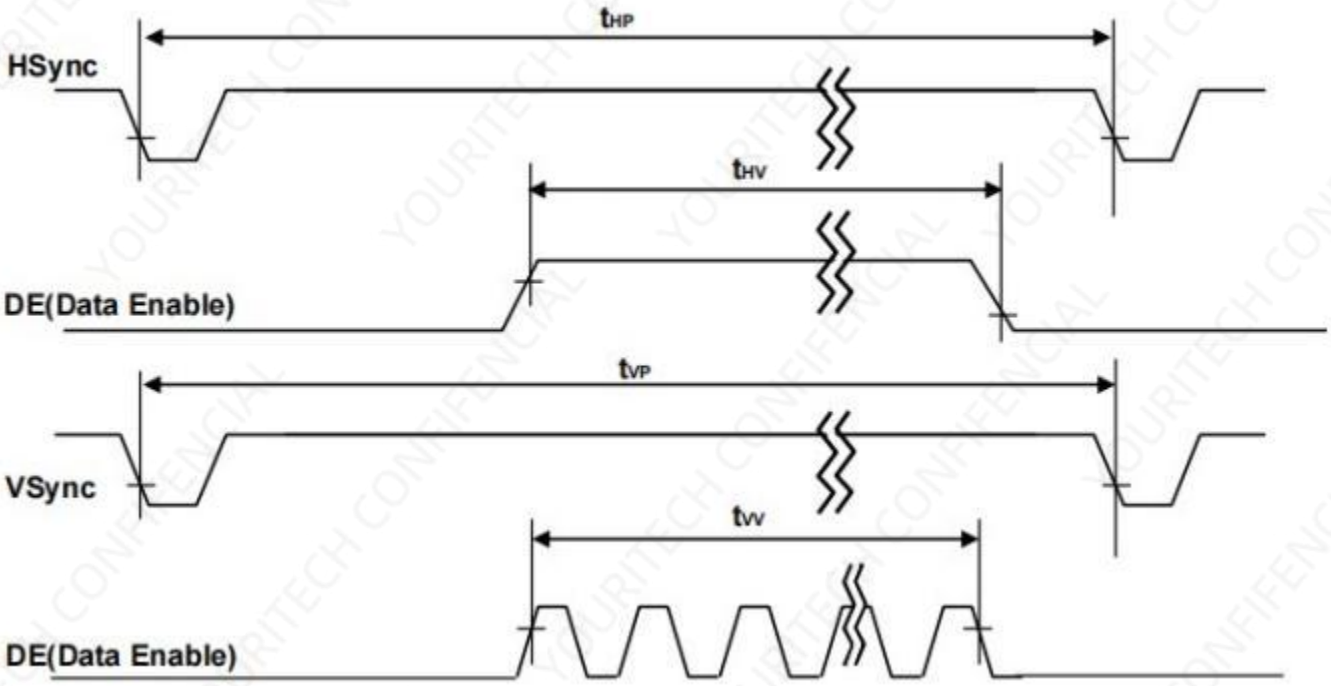
Notes: This product is DE only mode. The input of Hsync & Vsync signal does not have an effect on normal operation.

< LVDS Input SSCG>

Symbol	Parameter	Condition	Min	Typ	Max	Unit
F	LVDS Input frequency	-	45	74.25	85	MHz
T_{LVSK}	LVDS channel to channel skew	F=100MHz V_{IC}=1.2V V_{ID}=±400mV	-380	-	+380	ps
F_{LVMOD}	Modulating frequency of input clock during SSC		60	-	85	KHz
F_{LVDEV}	Maximum deviation of input clock frequency during SSC		-3	-	+3	%
T_{CY-CY}	Cycle to Cycle jitter		-	-	100	ps

5.2 Signal Timing Waveform





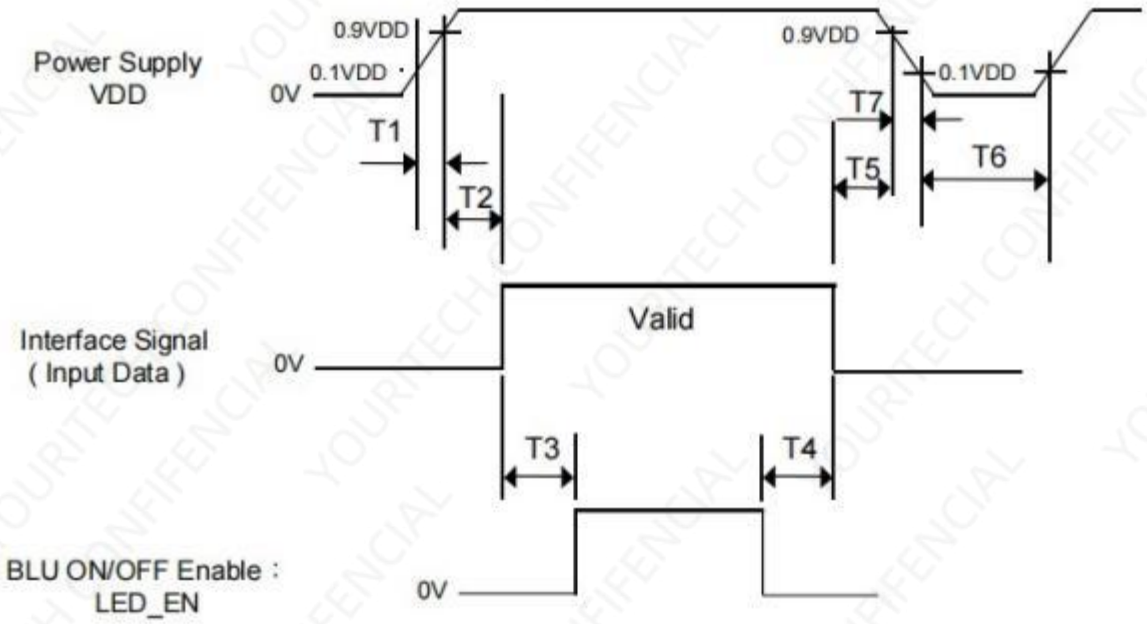
5.3 Input Signals, Basic Display Colors and Gray Scale of Colors

< Input Signal and Display Color Table >

Color & Gray Scale		Input Data Signal																							
		Red Data								Green Data								Blue Data							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale of Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	↑								↑								↑							
	▽	↓								↓								↓							
	Brighter	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	▽	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	△	↑								↑								↑							
	▽	↓								↓								↓							
	Brighter	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	▽	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale of Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	△	↑								↑								↑							
	▽	↓								↓								↓							
	Brighter	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	▽	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Gray Scale of White	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
	Darker	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
	△	↑								↑								↑							
	▽	↓								↓								↓							
	Brighter	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1
	▽	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

5.4 Power Sequence

To prevent a latch-up or DC operation of the Open Cell, the power on/off sequence shall be as shown in below



< Table 11. Sequence Table >

Parameter	Values			Units
	Min	Typ	Max	
T1	0.5	-	20	ms
T2	10	-	100	ms
T3	200	-	-	ms
T4	200	-	-	ms
T5	0	-	-	ms
T6	1	-	-	s

Notes: 1. Back Light must be turn on after power for logic and interface signal are valid.
2. Even though T1 is out of SPEC, it is still ok if the inrush current of VDD is below the limit.
3. When VDD<0.9VDD(Typ.),Power off.
4. T7 decreases smoothly, if there were rebounding voltage, it must smaller than 5 volts.

6. BACKLIGHT UNIT

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
BLU Voltage	U		58		V	
BLU Current	I		720		mA	
BLU Power	P		41.76		W	
BLU lifetime	T	40000			Hrs	(1)

Connector Information

Pin number	Description
1	negative polarity
2	Input voltage Power Supply

Note (1) User's Mating Connector Part No.:

Connector (wire type): PH2.0-2Pin 2 groups

7. OPTICAL CHARACTERISTICS

The test of optical specifications shall be measured in a dark room (ambient luminance≤1 lux and temperature=25±2℃) with the equipment of Luminance meter system (Goniometer system and PR730) and test unit shall be located at an approximate distance 180cm from the LCD surface at a viewing angle of θ and Φ equal to 0°. We refer to $\theta_{Ø=0}$ (=θ_3) as the 3 o'clock direction (the "right"), $\theta_{Ø=90}$ (= θ_{12}) as the 12 o'clock direction ("upward"), $\theta_{Ø=180}$ (= θ_9) as the 9 o'clock direction ("left") and $\theta_{Ø=270}$(= θ_6) as the 6 o'clock direction ("bottom"). While scanning θ and/or Ø, the center of the measuring spot on the Display surface shall stay fixed. The measurement shall be executed after 30 minutes warm-up period. VDD shall be 12.0V at 25°C. Optimum viewing angle direction is 6 'clock.

< Optical Table >

[VDD = 12.0V, Frame rate = 60Hz, Ta =25±2 ℃]

Parameter		Symbol	Condition	Min	Typ	Max	Unit	Remark
Viewing Angle	Horizontal	Θ_3	CR > 10		89	-	Deg.	Note 1
		Θ_9			89	-	Deg.	
	Vertical	Θ_{12}			89	-	Deg.	
		Θ_6			89	-	Deg.	
Brightness		Lv	Θ = 0° (Center) Normal Viewing Angle	-	-	-		
Contrast ratio		CR		800:1	1200:1	-		Note 2
White luminance uniformity		ΔY		-	-	-	%	Note 3
Reproduction of color	White	W_x		TYP. - 0.03	0.28	TYP. + 0.03		Note 4
		W_y			0.29			
	Red	R_x			0.645			
		R_y			0.332			
	Green	G_x			0.280			
		G_y			0.640			
	Blue	B_x			0.150			
		B_y			0.045			
Color Gamut				70	72	-	%	
Response Time	G to G	T_g		-	15	16	ms	Note 5

Note :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface.
2. Contrast measurements shall be made at viewing angle of $\theta = 0°$ and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (See Figure 1 shown in Appendix) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. The White luminance uniformity on LCD surface is then expressed as :
   ΔY = (Minimum Luminance of 9 points / Maximum Luminance of 9 points) * 100
   (See Figure 5 shown in Appendix).
4. The color chromaticity coordinates specified in Table 9.shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel. The BLU is used by BOE.
5. Response time Tg is the average time required for display transition by switching the input signal as below table and is based on Frame rate fV =60Hz to optimize.
   Each time in below table is defined as Figure 3and shall be measured by switching the input signal for "any level of gray(bright)"and "any level of gray(dark)".
6. Definition of Transmittance (T%) :
   Module is with white(L255) signal input

$$\text{Transmittance} = \frac{\text{Luminance of LCD Module}}{\text{Luminance of BLU}} \times 100\ \%$$

8. RELIABILITY TEST

The Reliability test items and its conditions are shown in below.

< Reliability Test Parameters >

No	Test Items	Conditions
1	High temperature storage test	Ta = 60 °C, 240 hrs
2	Low temperature storage test	Ta = -20 °C, 240 hrs
3	High temperature & high humidity operation test	Ta = 50 °C, 80%RH, 240hrs
4	High temperature operation test	Ta = 70 °C, 240hrs
5	Low temperature operation test	Ta = -20 °C, 240hrs
6	Thermal shock	Ta = -20 °C ↔ 60 °C (0.5 hr), 100 cycle
7	Vibration test (non-operating)	Frequency 10 ~ 200 Hz, Sweep rate 30 min Gravity / AMP 1.2 G Period X/60min, Y/30min, Z /30 min

This test condition is based on BOE module.

9.MECHANICAL OUTLINE DIMENSION