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To:

Preliminary

Customer Product Specification

Customer

Product Name :

Product Number :

Citizen Finedevice Co., Ltd.

Product Name : FLCD Module

Product Number : FL1401

(Receipt)

Date : / /

*Please return one signed original.

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Corporate seal

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Reviewed by	-	**Sales**	

Revision History

Rev	Revised date	Contents	Reason
0	June 27, 2018	Initial	-
1	Oct 4, 2018	Some corrections	Update
2	Dec 5, 2018	Correction (Table8-1, item 4.7 and Fig9)	Update

1. Scope

1.1 Scope

This specification covers the full color Ferroelectric Liquid Crystal Display (FLCD) module to be delivered from CITIZEN FINEDEVICE CO., LTD.

2. Specification summary

2.1 Specification summary

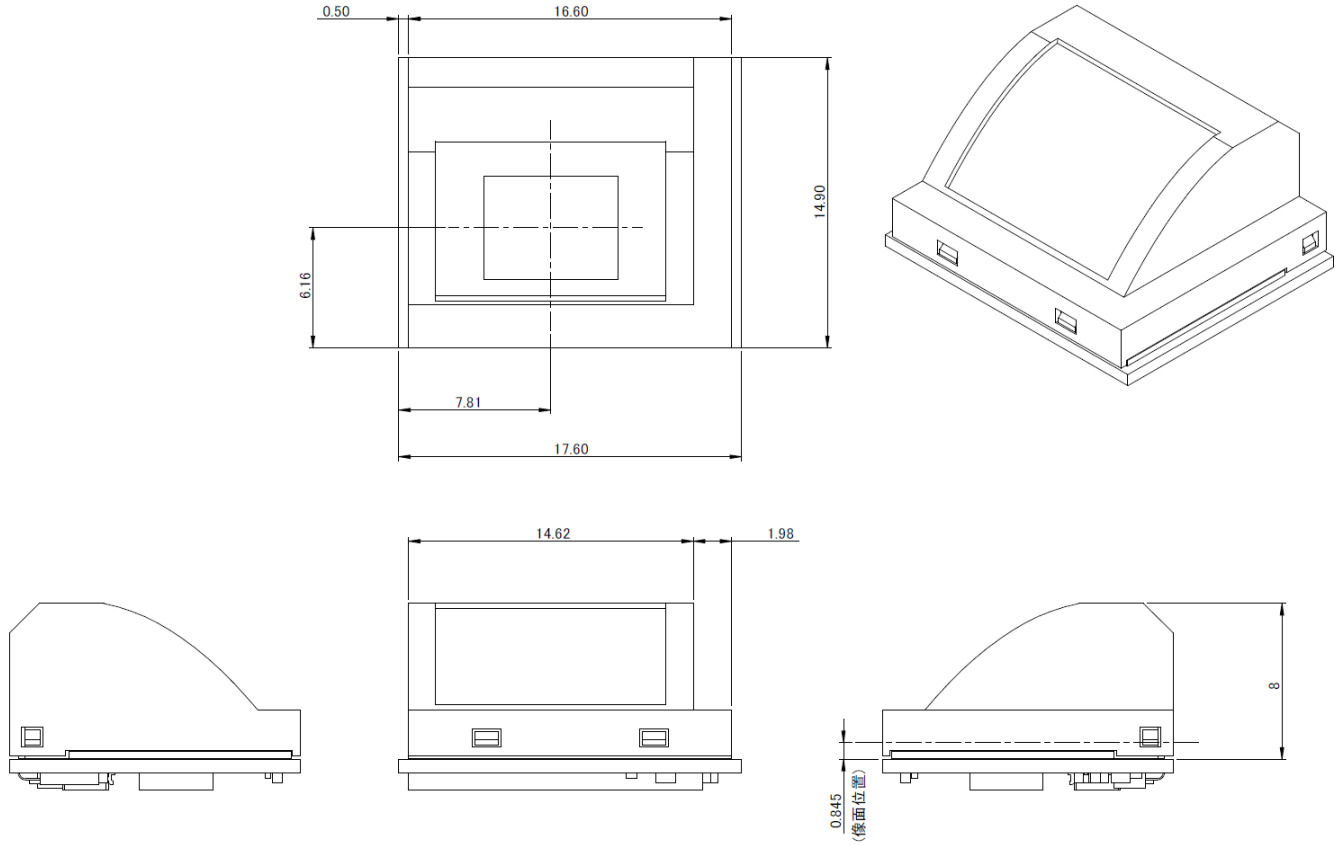
Table 1. Specification summary

Item	Specifications
Display Technology	Ferroelectric Liquid Crystal (FLC) on reflective CMOS
Display Mode	Field sequential color
Display Format	Quad VGA : 1,280(H) x 960 (V)
Display Panel Active Area	8.127 x 6.095mm
Display Area Diagonal	10.16mm (0.40")
Input Grayscale	256levels per color (8bits)
Color Depth	16.77Million unique colors (RGB888 input)
Brightness	220cd/m2 (Typical)
Contrast	250:1 (Typical)
White Point	(x,y)=(0.299,0.315) (Typical)
Display Pixel Pitch	6.35um
Display Frame Rate	60Hz/120Hz (NTSC), 50Hz/100Hz (PAL) Typical
Display Color Rate	540Hz (Max)
Data Clock Rate	24MHz to 103MHz
Digital Display Interface	RGB888 - parallel 24bit data, H/V sync, Clock RGB666 - parallel 18bit data, H/V sync, Clock RGB565 - parallel 16bit data, H/V sync, Clock YCbCr 4:4:4 - parallel 24bit data, H/V sync, Clock YCbCr 4:2:2 - parallel 16bit data, H/V sync, Clock
Control Interface	Industry-standard two-wire serial communication
Operating Supply Voltages	1.8V (Core), 3.3V (Core), 5V (Analog and LED drive), VIO_serial (Serial interface I/O; 1.8V to 3.3V)
Input Signal Level	CMOS 1.8V
Power Consumption *1	Approx. 360mW (Typical)
Size（L×W×H）	17.6 x 14.9 x 9.7mm
Weight	Approx. 1.7g
Operation Temperature	-10C to 70C（Panel temperature）
Storage Temperature	-30C to 83C

*1: Typical value at 60 Hz NTSC, flat field video pattern (data=FFh), gamma correction of 2.1, each power typical value, at room temperature (25C).

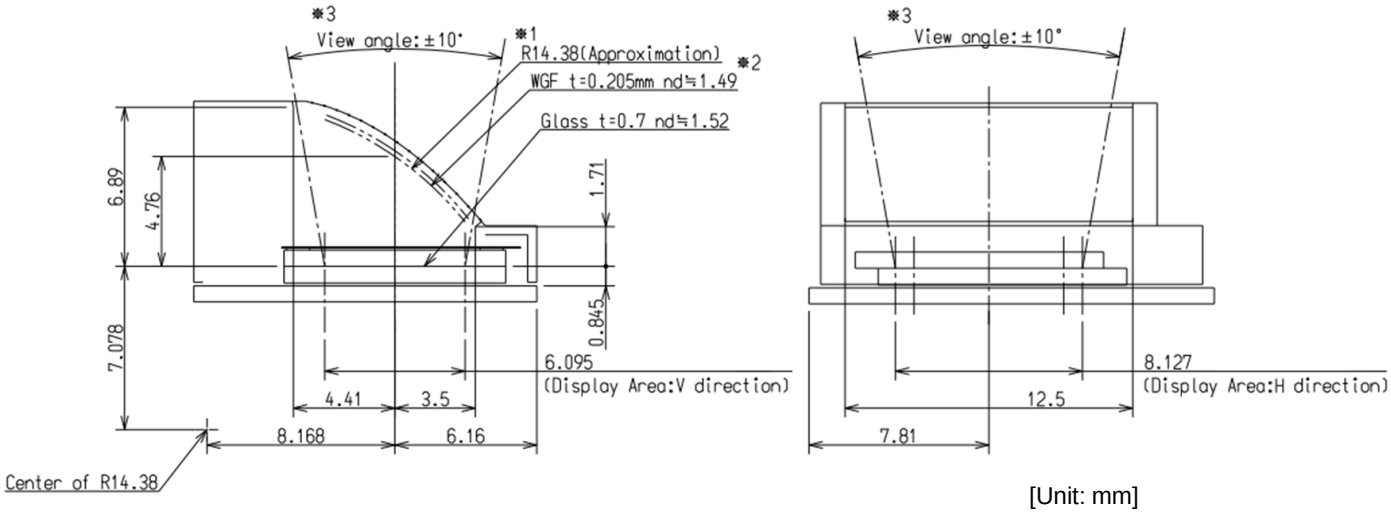
3. Product Appearance

3.1 Appearance



[Unit: mm]
(Unless Otherwise Specified, Tolerance : +/-0.2mm)

Fig.1-1 Appearance



[Unit: mm]
(Unless Otherwise Specified, Tolerance : +/-0.2mm)

*1 The cross-section curve of the WGF(Wire Grid Film) is not true circle and is confidential. Please refer to the proximate radius of the curve as R14.38.

*2 Since WGF has a multilayer structure, the refractive index is not defined. Please refer to the refractive index of TAC which is the main material of WGF (Approx. 1.49).

*3 The View angle is designed center value and not guaranteed value.

Fig.1-2 Cross-Section View (For optical design purpose)

4. Electrical Characteristics

4.1 Digital Video Interface

4.1-1 Video Input Signal Format

The following five kinds of input formats are applicable to the product.

1) RGB888 Format 24bit Parallel
2) RGB666 Format 18bit Parallel (When using, please contact us for the pin assignment.)
3) RGB565 Format 16bit Parallel (When using, please contact us for the pin assignment.)
4) YCbCr 4:4:4 Format 24bit Parallel
5) YCbCr 4:2:2 Format 16bit Parallel

4.1-2 Video Input Signal Timing

All video input signals must meet the timing requirements shown in the Fig.2, 3-1, 3-2, 3-3, & Table 2, 3.

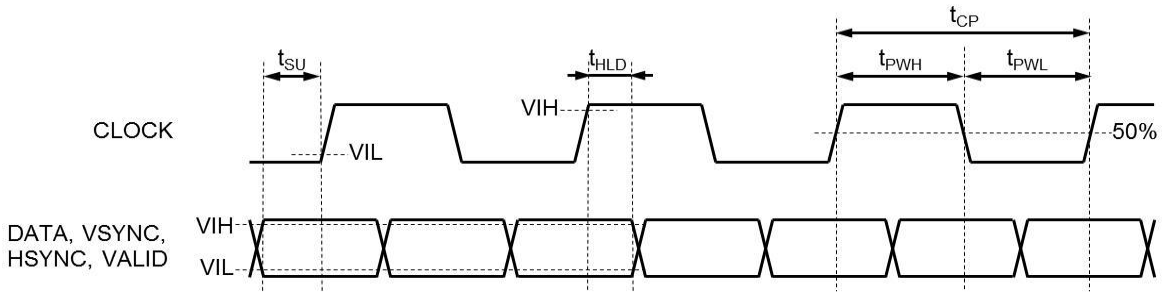


Fig.2 Video Input Signal Timing

Table 2. AC Characteristics (Video Input Signal Timing)

Item	Symbol	Min.	Typ.	Max.	Unit
CLOCK, rate	$1/t_{CP}$	24		103	MHz
CLOCK, pulse width high	t_{PWH}	40% t_{CP}	50% t_{CP}	60% t_{CP}	NA
CLOCK, pulse width low	t_{PWL}	40% t_{CP}	50% t_{CP}	60% t_{CP}	NA
DATA, VSYNC, HSYNC, VALID setup time	t_{SU}	1.25			ns
DATA, VSYNC, HSYNC, VALID hold time	t_{HLD}	1.25			ns

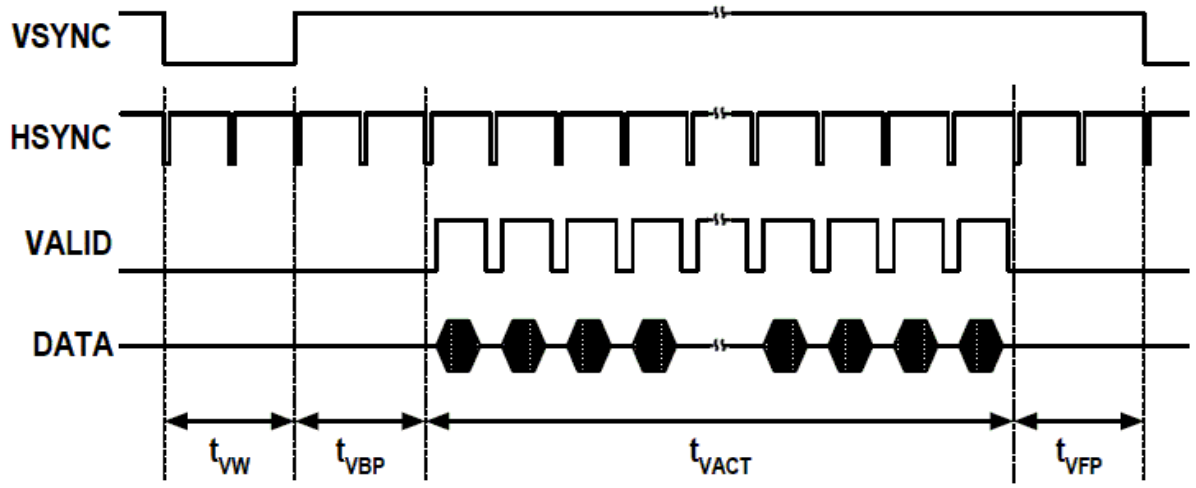


Fig.3-1 Video Input Vertical Timing

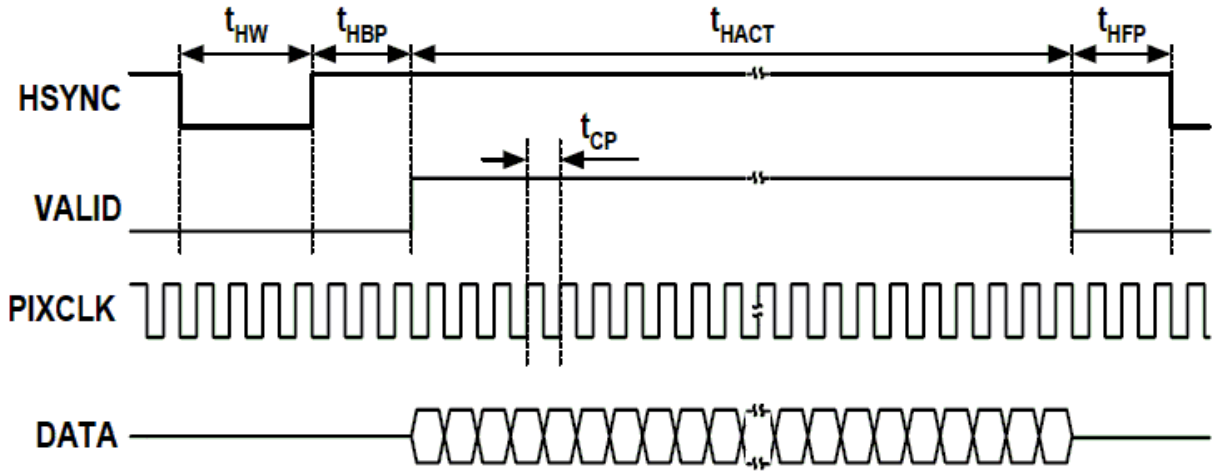


Fig.3-2 Video Input Horizontal Timing

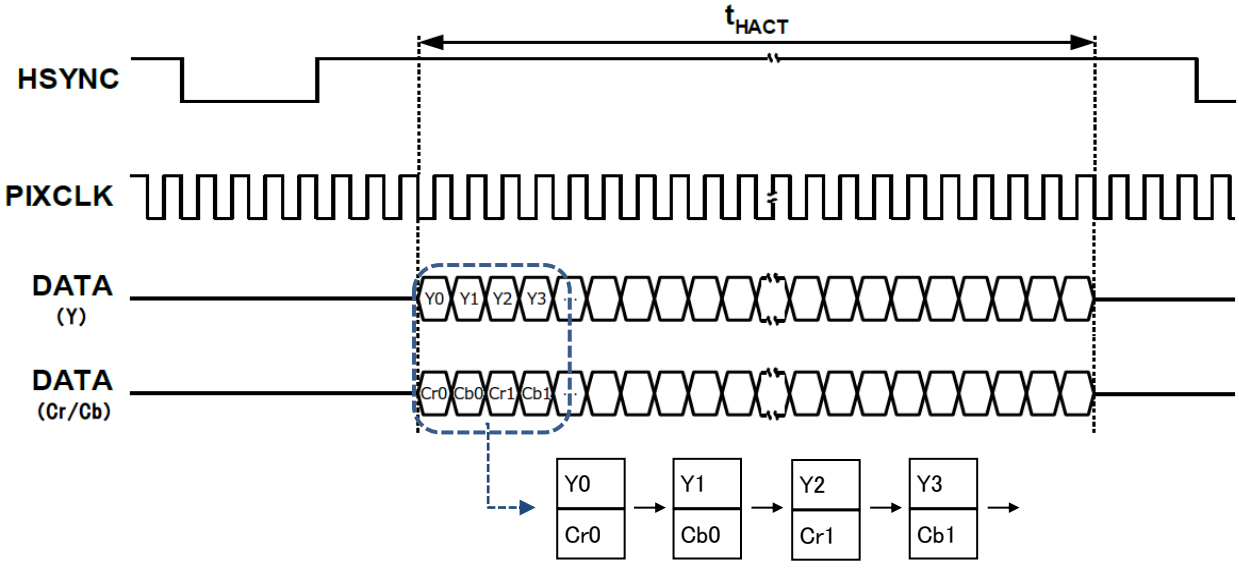


Fig.3-3 Data Sequence in case of YCbCr4:2:2 parallel 16bit input

Table 3. Parallel Data Video Timing Characteristics

Item	Symbol		Min.	Typ.	Max.	Unit
VSYNC, frequency	t_{VF}		47	60	120	Hz
VSYNC, total lines	$t_{VTOT} = t_{VBLK}+t_{VACT}$		255 *1		1022	Lines
VSYNC, active lines	t_{VACT}		240	960	960	Lines
VSYNC, blanking	$t_{VBLK} = t_{VFP}+t_{VW}+t_{VBP}$		15 *1		300	Lines
VSYNC, front porch	t_{VFP}		6 *1		-	Lines
VSYNC, sync pulse width	t_{VW}		3		-	Lines
VSYNC, back porch	t_{VBP}		6 *1		-	Lines
HSYNC, total clocks	$t_{HTOT} = t_{HBLK}+t_{HACT}$	with Valid input	346 *2			Clocks
		no Valid input	364 *2			
HSYNC, active clocks	t_{HACT}		320	1280	1280	Clocks
HSYNC, blanking	$t_{HBLK} = t_{HFP}+t_{HW}+t_{HBP}$	with Valid input	26 *2		-	Clocks
		no Valid input	44 *2		-	
HSYNC, front porch	t_{HFP}	with Valid input	10 *2		-	Clocks
		no Valid input	10 *2		-	
HSYNC, sync pulse width	t_{HW}	with Valid input	6		-	Clocks
		no Valid input	6		511	
HSYNC, back porch	t_{HBP}	with Valid input	10 *2		-	Clocks
		no Valid input	28 *2		511	
Pixel clock rate	$1/t_{CP}$		24		103	MHz

*1: When the number of VSYNC active lines is less than 960, the minimum porch period is to be the following value or the value in the above table, whichever is larger.

V Back Porch >= Ceiling[(VOFFSETTOP * 10us) / (H total clocks * (1/CLOCK freq))]

V Front Porch >= Ceiling[(VOFFSETBOT * 10us) / (H total clocks * (1/CLOCK freq))]

*2: When the number of HSYNC active clocks is less than 1,280, the minimum porch period is to be the following value or the value in the above table, whichever is larger.

H Back Porch >= Ceiling[(300ns + (HOFFSETLEFT*10ns)) / (1/CLOCK freq)]

H Front Porch >= Ceiling[(300ns + (HOFFSETRIGHT*10ns)) / (1/CLOCK freq)]

VOFFSETTOP = voffset_top_pix
VOFFSETBOT = voffset_bot_pix
HOFFSETLEFT = hoffset_left_pix
HOFFSETRIGHT = hoffset_right_pix

} Please refer to [Figure 4.1-3 Cropping and Offset].

Supplementary Caution:

Even within the range (Min to Max) in the table 3, a certain combination of video format timing may limit a certain value of the video format timing above.

It is advisable to contact CFD on the desired concrete values of video format timing.

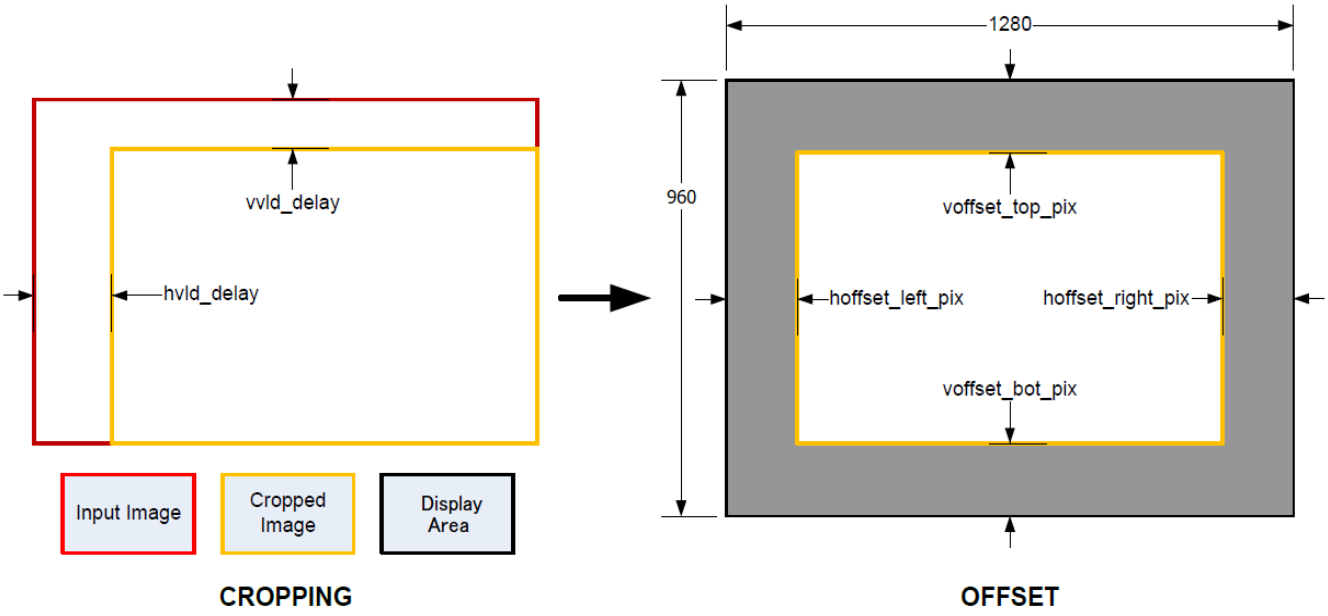
4.1-3 Video Offset and Cropping

By setting horizontal, vertical video offset register (D1h-D5h), it enables to place the picture in the specific position on the display. The hoffset_left_pix and hoffset_right_pix registers are respectively set the display position from the right and left edge on a pixel unit basis. The voffset_top_pix and voffset_bot_pix registers are respectively set the display position from the upper and bottom edge on a two-line unit basis. All the pixels other than display area are black.

The delay from HSYNC (VSYNC) assertion or Horizontal (Vertical) Valid assertion (when using valid input) can be set by hvld_delay (0Dh-0Eh) registers and vvld_delay (0Ch) register (Cropping).

The horizontal sample delay HVldDelay (0Dh-0Eh) is always given in number of clocks, and the vertical sample delay VVldDelay (0Ch) is given in lines.

By offset register setting, the post-cropped picture can be adjust to place in the center of display area.



*Note that the voffset_top_pix and voffset_bot_pix registers should be set on a two-line unit basis.

Fig.4 Cropping and Offset

Supplementary Caution :

Other setting conditions may disable the vertical and horizontal offset functions.

If you want to use the offset register, contact CFD for the optimal values of video format timing.

4.1-4 Scaling

The scaling engine is based on a fractional accumulator to support arbitrary input resolutions from 320 horizontal pixels to 1280 horizontal pixels and from 240 vertical pixels to 960 vertical pixels.

The horizontal and vertical scaling coefficients (HScaleStep and VScaleStep) determine the scaling ratio.

HScaleStep and VScaleStep register settings are determined as follows in round-up decimal values (requires conversion to hexadecimal format).

$$XScaleStep = Ceiling\,[512 * [\frac{Displayed\ Resolution}{Post\ Crop\ Input\ Resolution}]]$$

Table 4. Scaling Setting Sample

Input Resolution	Output Resolution	HScaleStep [dec]	VScaleStep [dec]
QuadVGA (1280x960)	VGA (640x480)	256	256
QuadVGA (1280x960)	qHD (960x540)	384	288
SVGA (800x600)	QuadVGA (1280x960)	820	820
720p (1280x720)	QuadVGA (1280x960)	512	683

Supplementary Caution:

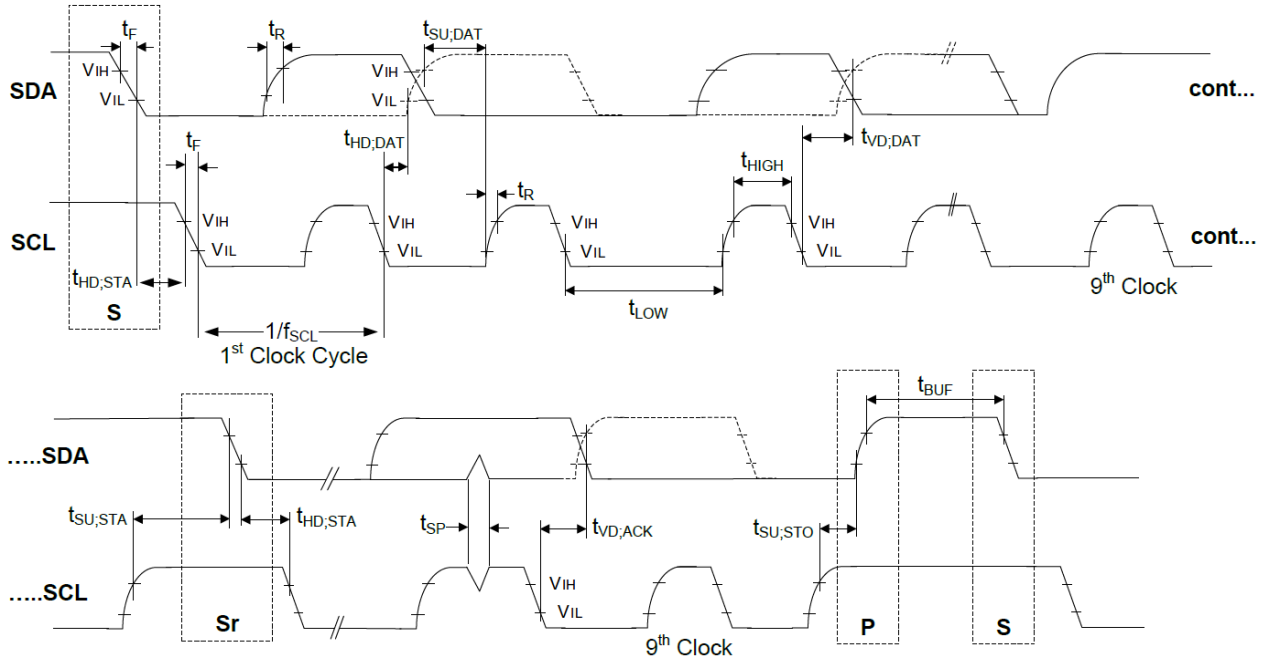
Other setting conditions may disable the scaling function.

If you want to use the scaling function, it is advisable to contact CFD.

4.2 Control Interface

4.2-1 AC characteristics of Interface signal

The product is controlled by writing data in the control registers with two-wire interface. The AC characteristics of interface signal are as follows.



* For the definition of V_{IH} and V_{IL}, please refer to [4.5 Ratings].

Fig.5 Two-wire serial interface signal

Note: SCL and SDA are not pulled-up in the product.

Table 5. AC Characteristics (Two-wire interface)

Symbol	Parameter	Conditions	Standard mode		Fast mode		Unit
			Min.	Max.	Min.	Max.	
f_{SCL}	SCL clock frequency		0	100	0	400	KHz
$t_{HD;STA}$	hold time (& repeated) START condition	After this period, the first clock pulse is generated.	4	-	0.6	-	us
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	us
t_{HIGH}	HIGH period of the SCL clock		4	-	0.6	-	us
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	us
$t_{HD;DAT}$	data hold time		5	-	5	-	ns
$t_{SU;DAT}$	data set-up time		250	-	100	-	ns
t_R	rise time of both SDA and SCL signals		-	1000	20+ 0.1Cb	300	ns
t_F	fall time of both SDA and SCL signals		-	300	20+ 0.1Cb	300	ns
$t_{SU;STO}$	set-up time for STOP condition		4	-	0.6	-	us
t_{BUF}	bus free time between STOP and START condition		4.7	-	1.3	-	us
Cb	capacitive load for each bus line (depends on load and frequency)		-	400	-	400	pF
$t_{VD;DAT}$	data valid time		-	3.45	-	0.9	us
$t_{VD;ACK}$	data valid acknowledge time		-	3.45	-	0.9	us
t_{SP}	pulse width of spikes that must be suppressed by the input filter		n/a	n/a	0	50	ns

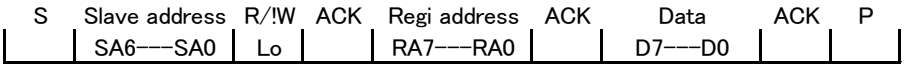
4.2-2 Protocol

The device is always considered a slave in the system and requires a clock to be provided to it for all two-wire serial interface transactions.

- Start Condition : A start condition is generated through the use of pulling down the SDA line while SCL is still high.
- Slave Address : 7bit -- 0111110b.
- R/!W bit : The 8th bit. If a READ is requested then the bit should be kept high, and if a WRITE is requested, the line is pulled down to a low-level signal.
- ACK bit : The 9th bit. The acknowledgment bit from the addressed device. If the addressed device receives its address and is not busy at that time it will respond by pulling the SDA line low and therefore signaling an acknowledgment. If an acknowledgment is detected by the issuing device, then the rest of the message can be sent.
- Stop Condition : If SCL is kept high and SDA changes from low to high, the interface stops.

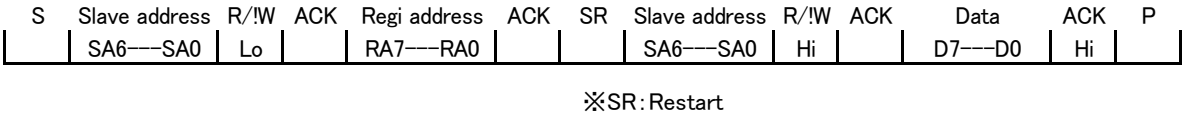
Single Write Protocol

A START signal must be presented first. This is when the SDA line is pulled low while the SCL line is kept high. The first byte sent is always the slave address for the product's I2C interface (0111 110b) followed by the R/!W bit(Lo). An acknowledge (ACK) is returned from the receiving device after each byte sent by pulling the SDA line low for one clock. The clock is still provided by the master device, which is never the product. The second byte sent in the write transactions is the product's 8-bit register address that will be written. After the register address is sent, the byte to be written is sent. The master keeps control of the bus and delivers the byte to be written.



Single Read Protocol

After a START, the slave address and R/!W(Lo) are sent. After an ACK is returned from the receiving device, the register address to be read is sent. Again after an ACK is returned from the receiving device, a START signal is presented again and the slave address is sent followed by the R/!W bit(Hi). After an ACK is returned, the device reads the byte data but not return an ACK. Then, the SDA line is changed from Lo to Hi with keeping the SLC Hi and the interfacing is over.



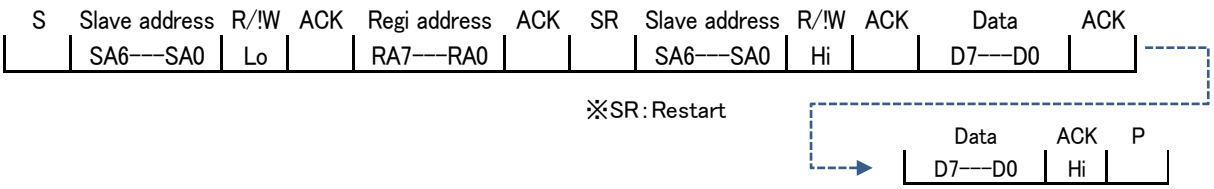
※SR：Restart

Multi-Write Protocol

Similar to single write protocol, after transactions of a START, the slave address, R/W!(Lo), an ACK, and byte data in that order, by continuously outputting data, the register address is auto-incremented for each byte write. After all data are written in the necessary addresses, the SDA line is changed from Lo to Hi with keeping the SLC Hi and the interfacing is over.

Multi-Read Protocol

Similar to single read protocol, after transactions of a START, the slave address, R/W!(Lo), an ACK, the register address, a START(SR), the slave address, R/!W(Hi) and an ACK in that order, by continuously reading data, the register address in the device is auto-incremented and the data is output. After all data are read in the necessary addresses, not returning an ACK, the SDA line is changed from Lo to Hi with keeping the SLC Hi and the interfacing is over.



※SR：Restart

4.3 Control Sequence

The following timing /sequence requirements must be met during Start-up, Shut-down, Sleep and Wake-up to avoid damages to the display panel.

4.3-1 Start-up Sequence

The VCCX power supply must be present before the VCC power supply is present. After the VCCX power supply is present, the VCC, VIO_serial must be present for a time period of t_{VCCXUP}.

No precedence on which supply, the VCC or VIO_serial, is present earlier, however, the both of power supplies must be present for a time period of $t_{VCC2VIO}$.

After the VCC voltage supply is present and in specification, the display panel will load default register values from non-volatile memory to RAM for a time period of t_{CNFG}. During this time period, the two-wire serial interface is ignored. Although the voltage supplies (VCC, VCCX, VIO_serial) can be present simultaneously, the t_{CNFG} starts when the VCC power supply is in specification.

After the t_{CNFG} period, the two-wire serial interface will be active, which enables register setting for all commands other than a turn-on command, if necessary.

After a time period of t_{VIDON} since the voltage supplies (VCC, VCCX, VIO_serial) is present, all the video signals （DATA, CLOCK, Vsync, Hsync and Valid） must be present. After the VCC, VCCX, VIO_serial supplies are present followed by stable presence of all the video signals (DATA, CLOCK, Vsync, Hsync and Valid), the turn-on command must be present.

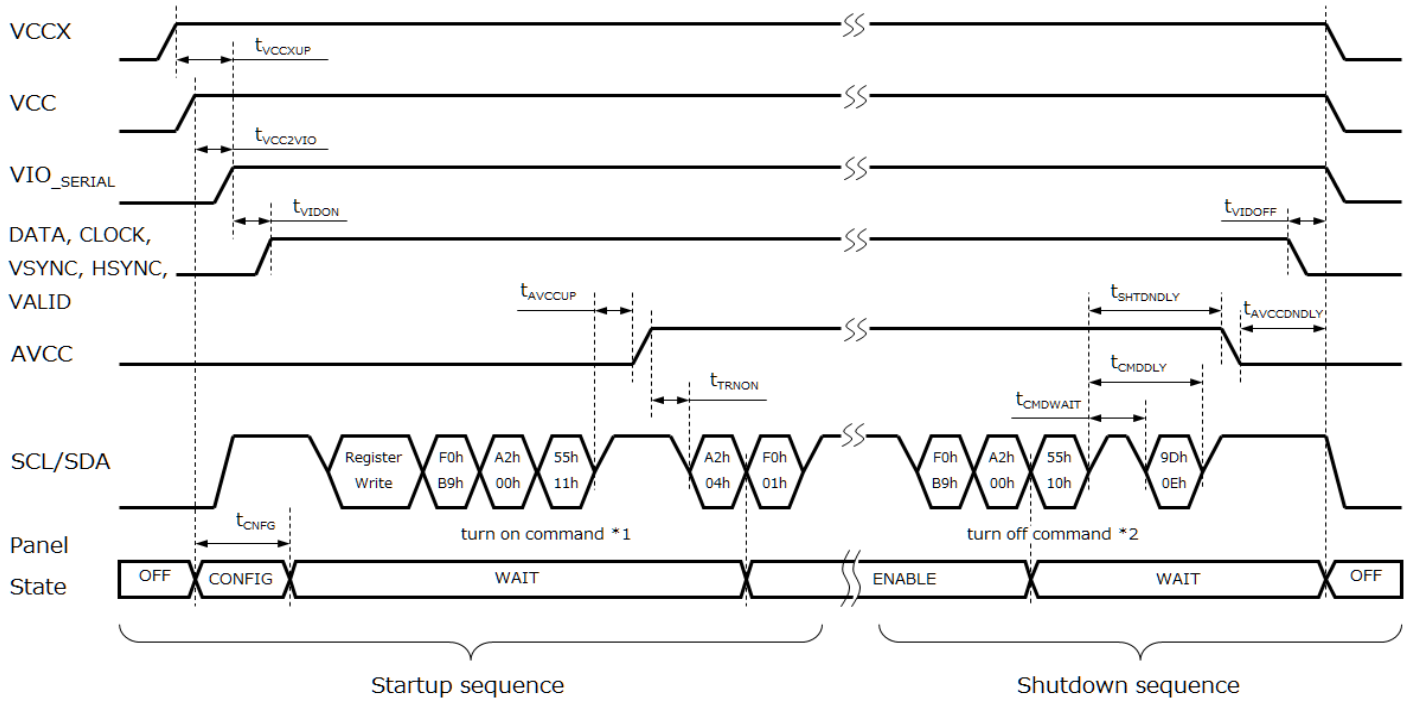
The turn-on command contains the requirement that the AVCC supply must be present after a time period of t_{AVCCUP}. After the turn-on command is complete, the display panel starts image display.

4.3-2 Shut-down Sequence

In case of shut-down of the display, the turn-off command must be present through the serial interface, before the voltage supplies are stopped. After the turn-off command is present, each power supply including the AVCC and the video signals (DATA, CLOCK, Vsync, Hsync, and Valid) must be continuously supplied for a time period of $t_{SHTDNDLY}$. Afterwards, the AVCC power supply is stopped first, and then the video signals (DATA, CLOCK, Vsync, Hsync, and Valid) must be stopped.

After a time period of $t_{AVCCDNDLY}$, the voltage supplies (VCC, VCCX, VIO_serial) must be stopped.

Please note that the video signals (DATA, CLOCK, Vsync, Hsync, and Valid) must be stopped a time period of t_{VIDOFF} or earlier before the voltage supplies (VCC, VCCX, VIO_serial) is stopped.



***1 turn on command**

Register Index		:	Data Value
(#1)	F0h	:	B9h
(#2)	A2h	:	00h
(#3)	55h	:	11h
(#4)	t_{AVCCUP}		
(#5)	AVCC Supply		
(#6)	t_{TRNON}		
(#7)	A2h	:	04h
(#8)	F0h	:	01h

***2 turn off command**

Register Index		:	Data Value
(#1)	F0h	:	B9h
(#2)	A2h	:	00h
(#3)	55h	:	10h
(#4)	$t_{CMDWAIT}$		
(#5)	9Dh	:	0Eh

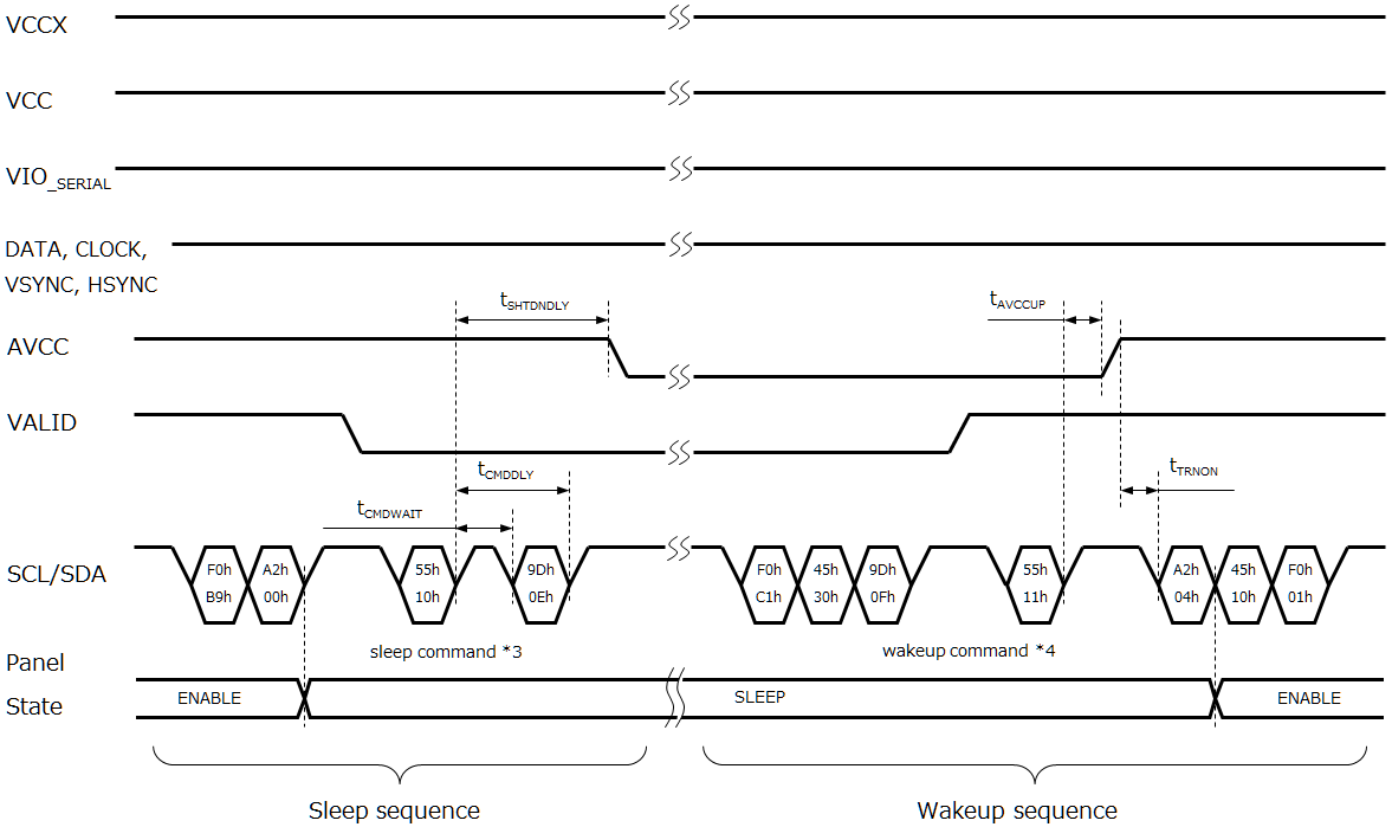
Fig.6-1 Start-up/Shut-down Sequence (sync_mode=00 and 01)

4.3-3 Sleep Sequence

To set the display to the sleep state, the sleep command below must be present through the serial interface. Afterwards, the AVCC power supply must be stopped after the $t_{SHTDNDLY}$ time period.

4.3-4 Wake-up Sequence

To enable the display from the sleep state, the wake-up command below must be present through the serial interface. The wake-up command contains the requirement that the AVCC supply must be present after a time period of t_{AVCCUP}.



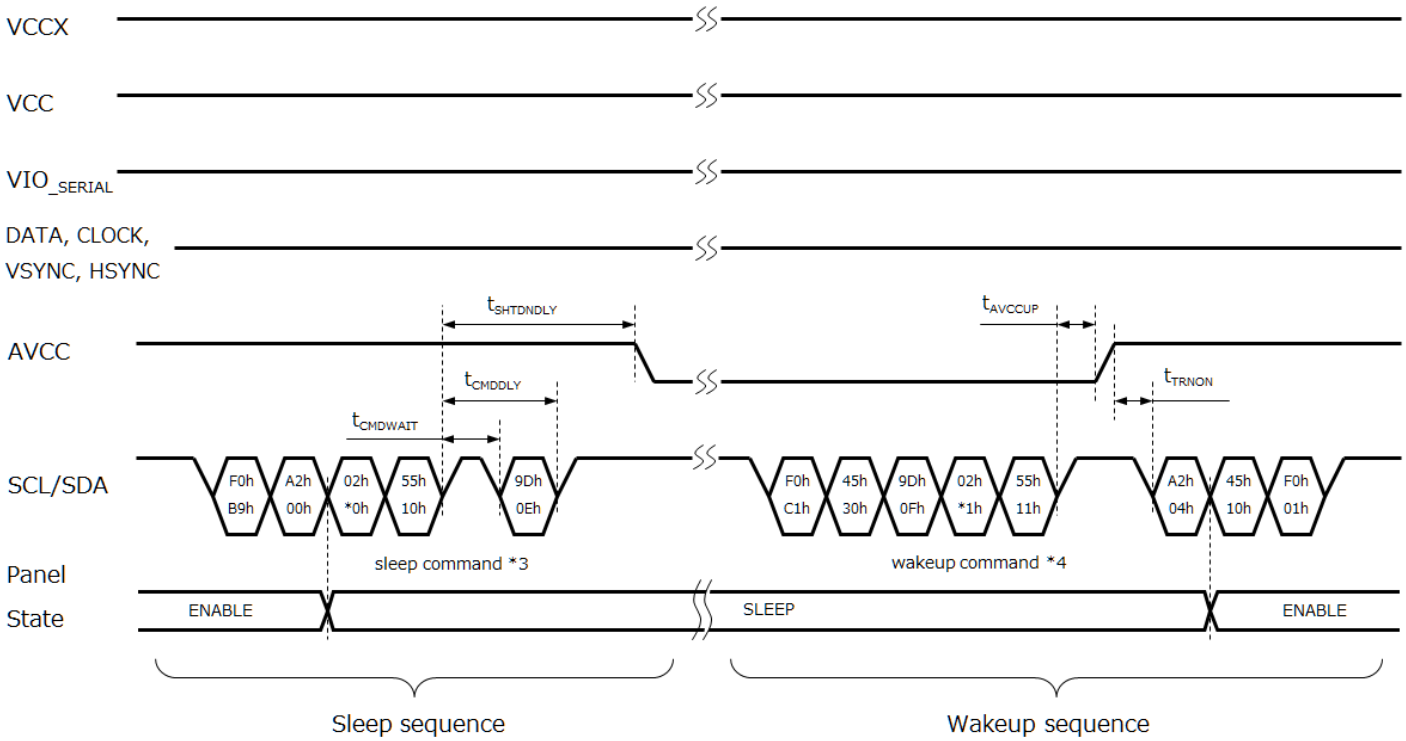
***3 sleep command**

Register Index	:	Data Value
(#1) F0h	:	B9h
(#2) A2h	:	00h
(#3) VALID OFF (Low)		
(#4) 55h	:	10h
(#4) $t_{CMDWAIT}$		
(#5) 9Dh	:	0Eh

***4 wake-up command**

Register Index	:	Data Value
(#1) F0h	:	C1h
(#2) 45h	:	30h
(#3) 9Dh	:	0Fh
(#4) VALID ON (High)		
(#5) 55h	:	11h
(#6) t_{AVCCUP}		
(#7) AVCC Supply		
(#8) t_{TRNON}		
(#9) A2h	:	04h
(#10) 45h	:	10h
(#11) F0h	:	01h

Fig.6-2 Sleep/Wake-up Sequence (sync_mode=00)



***3 sleep command**

Register Index		:	Data Value
(#1)	F0h	:	B9h
(#2)	A2h	:	00h
(#3)	02h	:	*0h
(#4)	55h	:	10h
(#4)	$t_{CMDWAIT}$		
(#5)	9Dh	:	0Eh

***4 wake-up command**

Register Index		:	Data Value
(#1)	F0h	:	C1h
(#2)	45h	:	30h
(#3)	9Dh	:	0Fh
(#4)	02h	:	*1h
(#5)	55h	:	11h
(#6)	t_{AVCCUP}		
(#7)	AVCC Supply		
(#8)	t_{TRNON}		
(#9)	A2h	:	04h
(#10)	45h	:	10h
(#11)	F0h	:	01h

Fig.6-3 Sleep/Wake-up Sequence (sync_mode=01)

Table 6. AC Characteristics (Control sequence timing)

Item	Symbol	Min.	Typ.	Max.	Unit
Start-up Sequence / Wake-up Sequence					
Time from VCCX supply to VCC, VIO_serial supply	t_{VCCXUP}	0	-	5	ms
Time from VCC supply to VIO_serial supply	$t_{VCC2VIO}$	-1	-	1	ms
Time from VCC supply to when Configuration is finished	t_{CNFG}	-	-	100	ms
Time from VCCX, VCC, VIO_serial supply to when video signals are supplied	t_{VIDON}	0	-	-	us
Time after the turn-on command #3 / wake-up command #5 to when AVCC is supplied[*1]	t_{AVCCUP}	6	-	-	video field
Time from AVCC supply[*2] to when the turn-on command #7 /wake-up command #9 is started	t_{TRNON}	0	-	-	us
Shut-down Sequence / Sleep Sequence					
Time of the designated waiting period in the turn-off command /sleep command	$t_{CMDWAIT}$	1.5	-	-	ms
Time after the turn-off command #3 /sleep command #4 to when the turn-off command /sleep command is complete	t_{CMDDLY}	-	-	3	ms
Time after the turn-off command #3 /sleep command #4 to when AVCC is stopped[*2]	$t_{SHTDNDLY}$	t_{CMDDLY}	-	-	ms
Time from stop of video signals to stop of VCCX, VCC, VIO_serial supplies	t_{VIDOFF}	0	-	-	us
Time from stop of AVCC[*1] to stop of VCCX,VCC,VIO_serial supplies	$t_{AVCCDNDLY}$	200+t_{VIDOFF}	-	-	us

Note 1: The definitions of *1 & *2 in the table above with regard to AVCC are as follows.

*1: Point where the AVCC achieves 0.5V.

*2: Point where the AVCC achieves the minimum rating in volt.

Note 2: All the definitions in the table above with regard to VCC, VCCX, VIO_serial mean the point where the voltage achieves the minimum rating.

Supplementary Precaution Statements

- To prevent the display image from being distorted or other failure, the stable video signals must be present during the time from when turn-on command is present to when turn-off command is complete.

- When changing any register setting during the display is working after start-up sequence, firstly the product should be set into sleep mode, then secondly write the desired setting in the sleep period (after sleep command and before wakeup command). After the wake-up sequence, the display starts with the new setting.

4.4 Pin Assignments

Table 7. Pin Assignments

No	Name	I/O	Power Supply	Function		
				24bit RGB	24bit YCbCr (4:4:4)	16bit YCbCr (4:2:2)
1, 2	GND	NA	NA	GND		
3, 4, 5	VCC *2	NA	NA	Panel Core Power Supply (+1.8V)		
6	GND	NA	NA	GND		
7	VCCX	NA	NA	Panel / EEPROM Power Supply (+3.3V)		
8	N.C,	NA	NA	* Open or directly connect to VCC		
9	VIO_serial	NA	NA	Serial Interface I/O Power Supply (+1.8V to +3.3V)		
10	CLOCK	I	1.8V	Video Data Clock		
11	VSYNC	I	1.8V	Vertical Synch Signal		
12	HSYNC	I	1.8V	Horizontal Synch Signal		
13	VALID	I	1.8V	Valid Signal (* If non-use : GND)		
14	GND	NA	NA	GND		
15	DATA 23	I	1.8V	Blue[7] (MSB)	Cr[7] (MSB)	GND
16	DATA 22	I	1.8V	Blue[6]	Cr[6]	GND
17	DATA 21	I	1.8V	Blue[5]	Cr[5]	GND
18	DATA 20	I	1.8V	Blue[4]	Cr[4]	GND
19	DATA 19	I	1.8V	Blue[3]	Cr[3]	GND
20	DATA 18	I	1.8V	Blue[2]	Cr[2]	GND
21	DATA 17	I	1.8V	Blue[1]	Cr[1]	GND
22	DATA 16	I	1.8V	Blue[0]	Cr[0]	GND
23	DATA 15	I	1.8V	Green[7] (MSB)	Cb[7] (MSB)	Cb[7] / Cr[7] (MSB)
24	DATA 14	I	1.8V	Green[6]	Cb[6]	Cb[6] / Cr[6]
25	DATA 13	I	1.8V	Green[5]	Cb[5]	Cb[5] / Cr[5]
26	DATA 12	I	1.8V	Green[4]	Cb[4]	Cb[4] / Cr[4]
27	DATA 11	I	1.8V	Green[3]	Cb[3]	Cb[3] / Cr[3]
28	DATA 10	I	1.8V	Green[2]	Cb[2]	Cb[2] / Cr[2]
29	DATA 9	I	1.8V	Green[1]	Cb[1]	Cb[1] / Cr[1]
30	DATA 8	I	1.8V	Green[0]	Cb[0]	Cb[0] / Cr[0]
31	DATA 7	I	1.8V	Red[7] (MSB)	Y[7] (MSB)	Y[7] (MSB)
32	DATA 6	I	1.8V	Red[6]	Y[6]	Y[6]
33	DATA 5	I	1.8V	Red[5]	Y[5]	Y[5]
34	DATA 4	I	1.8V	Red[4]	Y[4]	Y[4]
35	DATA 3	I	1.8V	Red[3]	Y[3]	Y[3]
36	DATA 2	I	1.8V	Red[2]	Y[2]	Y[2]
37	DATA 1	I	1.8V	Red[1]	Y[1]	Y[1]
38	DATA 0	I	1.8V	Red[0]	Y[0]	Y[0]
39	GND	NA	NA	GND		
40, 41	AVCC	NA	NA	Panel Analog / LED Power Supply (+5V)		
42	GND	NA	NA	GND		
43	SDA	IO	VIO_serial	Serial Interface Data I/O		
44	SCL	I	VIO_serial	Serial Interface Clock Input		
45	GND	NA	NA	GND		

*1: A mapping of video data signal for DATA0 to 23 can be changed. The details are referred to in [5.Configuration Register Settings].
*2: It is recommendable to put a 10uF or larger decoupling capacitor to the VCC on an operation circuit side.

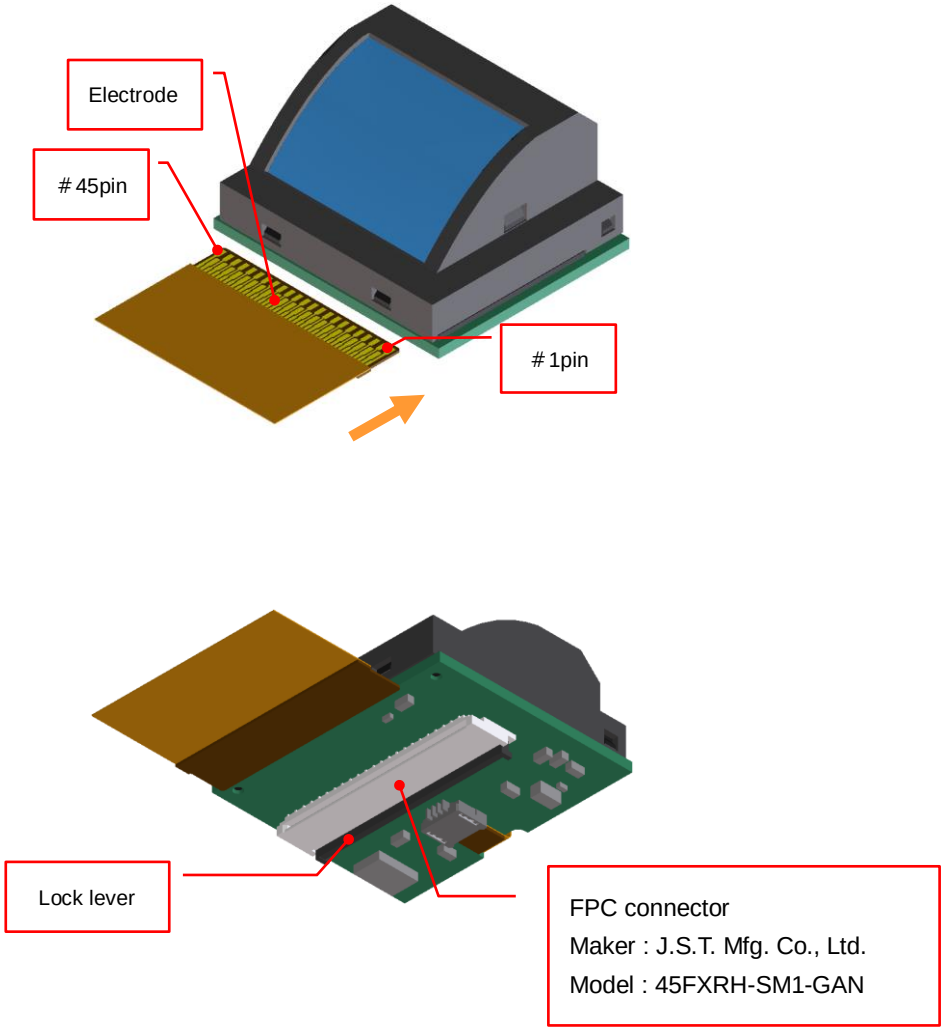


Fig.7 Pin Location and FPC Connector

ATTENTION: Please do not close the lock lever without inserting the FPC. There is a danger of the connector being damaged

4.5 Ratings

Table 8-1. Absolute Maximum Ratings

Item	Absolute Maximum Ratings		Unit
	Min.	Max.	
VCCX	-0.5	3.5	V
VCC	-0.5	1.9	V
AVCC	-0.5	5.3	V
VIO_serial	-0.5	3.5	V
Voltage on any Video Input Pin	-0.4	VCC+0.4	V
Voltage on any Serial Input Pin	-0.4	VIO_serial+0.4	V

Table 8-2. DC Characteristics

Item	Symbol	Condition		Rating			Unit
				Min.	Typ.	Max	
Power Supply Voltage	VCCX	*1		3.1	3.3	3.5	V
	VCC	*1		1.7	1.8	1.9	
	AVCC			4.7	5.0	5.3	
	VIO_serial			1.7	3.3	3.5	
*1: While operating, the VCCX and VCC must fulfill the following conditions. VCCX ≤ (VCC x 2)							
Input Voltage	V_{IH}	For all video inputs		0.74*VCC			V
		For all serial inputs		0.74*VIO_serial			
	V_{IL}	For all video inputs				0.25*VCC	
		For all serial inputs				0.25*VIO_serial	
Input Capacitance	IC	For all inputs 3.3Vp-p, f=5MHz			6	12	pF
Input Leakage Current	I_{IL}	$V_I=V_{IL}$		-10			uA
	I_{IH}	$V_I=V_{IH}$				10	
Average Panel Operating Supply Current	I_{VCCX}	VCCX=3.30V, VCC=1.80V, AVCC=5.00V, VIO_serial=3.30V, Input Reso: 1280x960, Display Reso: 1280x960, White Raster Image, CLOCK=75MHz, Field rate=60Hz, Gamma=2.1, At Room temperature, Normal Environment	Operation		7	9	mA
			Sleep		1.2	3	
	I_{VCC}		Operation		180	225	
			Sleep		7	10	
	I_{AVCC}		Operation		3	7	
			Sleep		0.2	0.6	
	I_{VIO_serial}		Operation		0.1	0.5	
			Sleep		0.1	0.5	

*1 All supply voltages are measured at the display connector.

4.6 Electrical Circuit Diagram

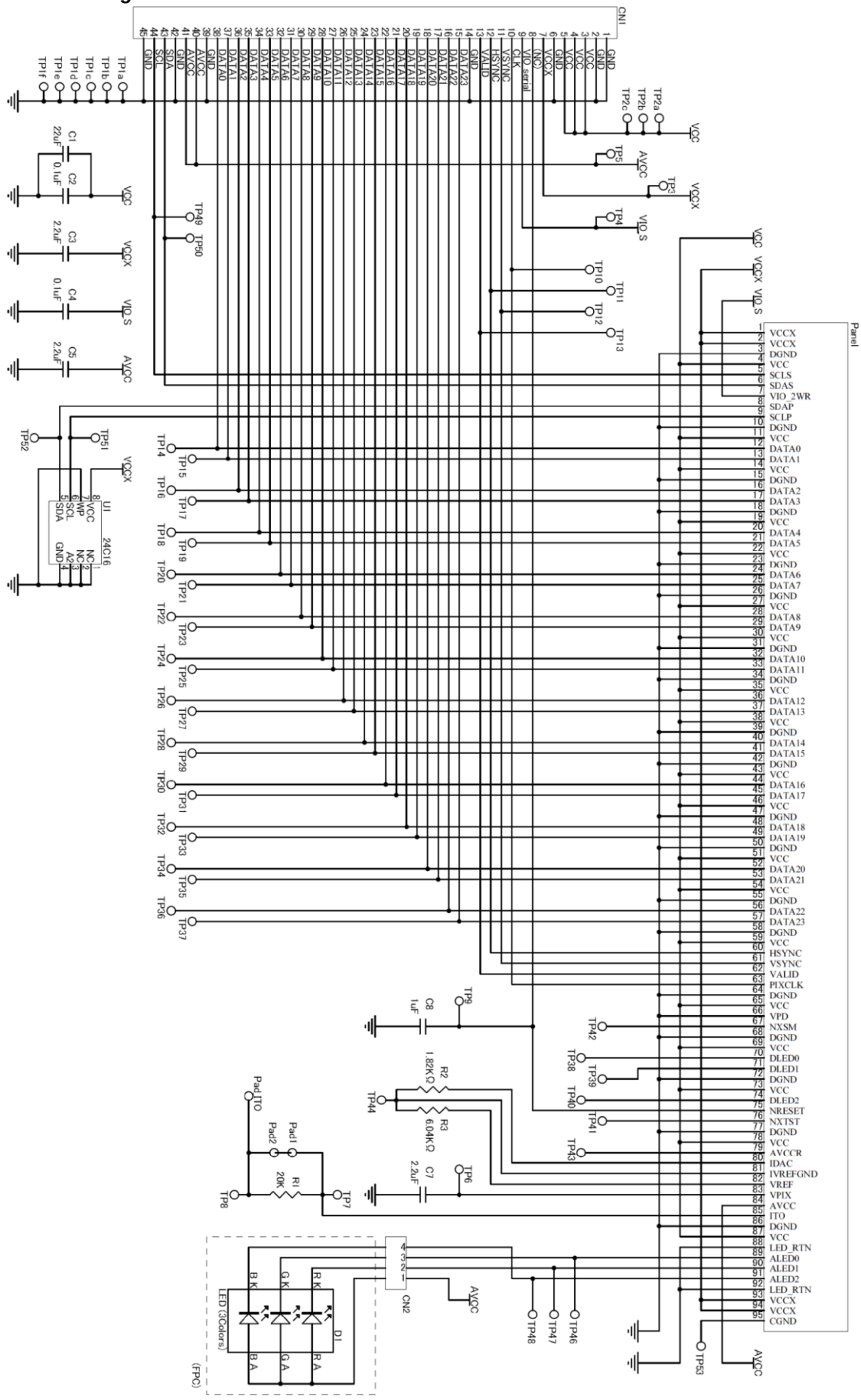


Fig.8 Circuit Diagram

4.7 Input Equivalent Circuit

To prevent ESD damage, protective diodes are provided for each input pin. The equivalent circuit of the input pins is shown below. All resistance values are typical. Since the resistance between Input and VCC is shown schematically, there is no pull-up implemented.

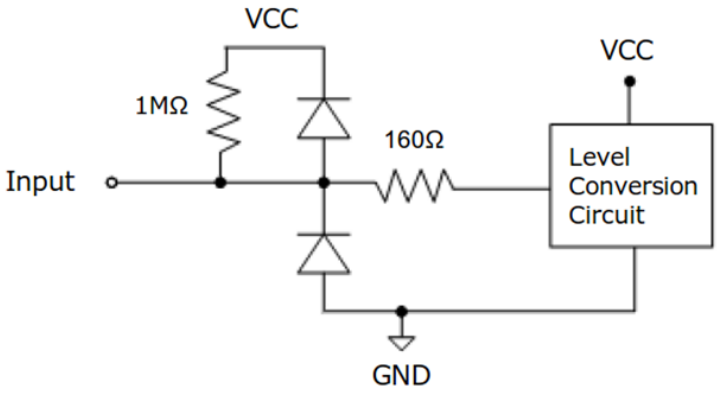


Fig.9 Input Equivalent Circuit

5. Configuration Register Settings

5.1 Configuration Register Settings

Register Index: 00h

Bit	7	6	5	4	3	2	1	0
Name	dither_mode[3:0]				Res			
Value (e.g.)	0001				0001			

dither_mode : Selects Dither mode

4'h1=1/2bit spatial dither, 1/4bit temporal dither
4'h2=1/2bit temporal dither, 1/4bit spatial dither
4'h3=1/2bit spatial dither
4'h5=Reserved（NA）
4'h6=Reserved（NA）
Other=No dither, Input data rounded to 6bit values

Res : Reserved

The above "Res" register value must be set to 0001b.

*** The following "Res" resister values must be set to the value instructed as value (e.g.).**

Register Index: 01h

Bit	7	6	5	4	3	2	1	0
Name	cspace_sel	channel_map[2:0]			data_channel[1:0]		data_seq[1:0]	
Value (e.g.)	0	000			01		00	

cspace_sel : Selects color space

0=RGB
1=YCbCr

channel_map : Selects mapping of data channel to color information, dependent on the data channel setting according to the following table.

channel_map	24bit RGB			24bit YCbCr			16bit YCbCr		
	[23:16]	[15:8]	[7:0]	[23:16]	[15:8]	[7:0]	[23:16]	[15:8]	[7:0]
0h	Blue	Green	Red	Cr	Cb	Y	-	Cb/Cr	Y
1h	Green	Red	Blue	Cb	Y	Cr	-	Y	Cb/Cr
2h	Red	Blue	Green	Y	Cr	Cb	Cb/Cr	Y	-
3h	Red	Green	Blue	Y	Cb	Cr	Y	Cb/Cr	-
4h	Green	Blue	Red	Cb	Cr	Y	Cb/Cr	-	Y
5h	Blue	Red	Green	Cr	Y	Cb	Y	-	Cb/Cr

data_channel : Selects data interface

00=24bit RGB, 24bit YCbCr
01=16bit YCbCr
other=Reserved. Setting is Not Availavle.

data_seq : Data sequence of color information

00=24bit RGB, 24bit YCbCr
01=16bit YCbCr ([Y0Cr0]-[Y1Cb0]) (*Refer to Fig.3-3.)
other=Reserved (N/A)

Register Index: 02h

Bit	7	6	5	4	3	2	1	0
Name	vsync_pol	hsync_pol	valid_pol	Res			sync_mode	
Value (e.g.)	1	1	0	000			00	

vsync_pol : Vertical sync polarity
0=Active High, 1=Active Low

hsync_pol : Horizontal sync polarity
0=Active High, 1=Active Low

valid_pol : Valid signal polarity
0=Active High, 1=Active Low
* When non-use the Valid Signal, this bit must be set to 0b.

sync_mode : Selects data sampling mode
00=Use VALID inputs for valid video timing.
01=Use HSYNC and VSYNC inputs, valid timing specified from valid_delay registers.
10 and 11=Reserved (N/A)

Register Index: 06h-07h, 09h-0Ah

Index	Value (e.g.)	7	6	5	4	3	2	1	0
06h	02h	Res (0000 0)					vscale_step[10:8]		
07h	00h	vscale_step[7:0]							
09h	02h	Res (0000 0)					hscale_step[10:8]		
0Ah	00h	hscale_step[7:0]							

vscale_step, vscale_cycle : Vertical scaling coefficient [range: 0-1024d]
hscale_step, hscale_cycle : Horizontal scaling coefficient [range: 0-1024d]
* Refer to [4.1-4 Scaling].

Register Index: 0Ch

Bit	7	6	5	4	3	2	1	0
Name	vvld_delay[7:0]							
Value (e.g.)	0000 0000							

vvld_delay : Vertical Valid Delay specified in number of lines
sync_mode=00 : Delay from vertical valid assertion to video data sampling. The setting value will crop the video.
sync_mode=01 : Delay from VSync assertion to video data sampling. The value should nominally be set to tVW+tVBP. The part of value (lines) beyond the tVW+tVBP will crop the video. (Refer to Figure 3-1 & Figure 4)

Register Index: 0Dh-0Eh

Index	Value (e.g.)	7	6	5	4	3	2	1	0
0Dh	00h	Res (0000 00)						hvld_delay[9:8]	
0Eh	00h	hvld_delay[7:0]							

hvld_delay : Horizontal Valid Delay specified in number of clocks
sync_mode=00 : Delay from horizontal valid assertion to video data sampling. The setting value will crop the video.
sync_mode=01 : Delay from HSync assertion to video data sampling –2. The value should nominally be set to tHW+tHBP-2. The part of value(clocks) beyond the tHW+tHB-2 will crop the video. (Refer to Fig. 3-2 & Fig. 4)

Register Index: 0Fh-17h

Index	Value (e.g.)	7	6	5	4	3	2	1	0
0Fh	00h	color_space_bus (cs_{11})							
10h	00h	color_space_bus (cs_{12})							
11h	00h	color_space_bus (cs_{13})							
12h	00h	color_space_bus (cs_{21})							
13h	00h	color_space_bus (cs_{22})							
14h	00h	color_space_bus (cs_{23})							
15h	00h	color_space_bus (cs_{31})							
16h	00h	color_space_bus (cs_{32})							
17h	00h	color_space_bus (cs_{33})							

color_space_bus : Parameters to change color space setting

* Refer to Register index 18h-1Ah.

Register Index: 18h-1Ah

Index	Value (e.g.)	7	6	5	4	3	2	1	0
18h	00h	color_offset_bus (O_1)							
19h	00h	color_offset_bus (O_2)							
1Ah	00h	color_offset_bus (O_3)							

color_offset_bus : Parameters to change color space setting

The RGB/YCbCr values are 'transformed' or converted to RGB values displayed by the values highlighted in yellow in the following equations. By setting the values highlighted in blue, the base color space transformation can be modified as needed.

(RGB Input)

$$\begin{bmatrix} R_O \\ G_O \\ B_O \end{bmatrix} = \frac{1}{128} \begin{bmatrix} 128+cs_{11} & 0+cs_{12} & 0+cs_{13} \\ 0+cs_{21} & 128+cs_{22} & 0+cs_{23} \\ 0+cs_{31} & 0+cs_{32} & 128+cs_{33} \end{bmatrix} \bullet \begin{bmatrix} R_I+O_1 \\ G_I+O_2 \\ B_I+O_3 \end{bmatrix}$$

(YCbCr Input)

$$\begin{bmatrix} R_O \\ G_O \\ B_O \end{bmatrix} = \frac{1}{128} \begin{bmatrix} 128+cs_{11} & 0+cs_{12} & 197+cs_{13} \\ 128+cs_{21} & -24+cs_{22} & -59+cs_{23} \\ 128+cs_{31} & 232+cs_{32} & 0+cs_{33} \end{bmatrix} \bullet \begin{bmatrix} Y_I+O_1 \\ Cb_I-128+O_2 \\ Cr_I-128+O_3 \end{bmatrix}$$

Fig.10 Color Space Conversion Equation

Register Index: 50h

Bit	7	6	5	4	3	2	1	0
Name	Res		led_bright_ratio[5:0]					
Value (e.g.)	11		3Fh					

led_bright_ratio : LED brightness for display lighting

Brightness is divided into 64 scales and can be set.

0h=Minimum brightness (1/64)

~

3Fh=Maximum brightness (64/64)

Register Index: D0h

Bit	7	6	5	4	3	2	1	0
Name	Res						vflip	hflip
Value (e.g.)	0000 00						1	1

vflip: Display vertical flip
0=disable
1=enable

hflip: Display horizontal flip
0=disable
1=enable

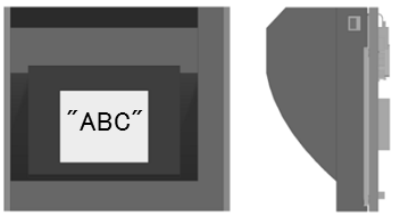


Fig.11 Display position at vflip=1, hflip=1

Register Index: 18h-1Ah

Index	Value (e.g.)	7	6	5	4	3	2	1	0
D1h	00h	voffset_top_pix[7:0]							
D2h	00h	voffset_bot_pix[7:0]							
D3h	00h	hoffset_left_pix[7:0]							
D4h	00h	hoffset_right_pix[7:0]							
D5h	00h	hoffset_right_pix[9:8]		hoffset_left_pix[9:8]		voffset_bot_pix[9:8]		voffset_top_pix[9:8]	

voffset_top_pix: Vertical offset from the top edge
The offset line from the top edge of the vertical 960 lines to the top edge of picture display (Unit : 2line).

voffset_bot_pix: Vertical offset from the bottom edge
The offset line from the bottom edge of the vertical 960 lines to the bottom edge of picture display (Unit : 2line)

hoffset_left_pix: Horizontal offset from the left edge
The offset pixel from the left edge of the horizontal 1280 pixels to the left edge of picture display (Unit : pixel)

hoffset_right_pix: Horizontal offset from the right edge
The offset pixel from the right edge of the horizontal 1280 pixels to the right edge of picture display (Unit : pixel)

Register Index: CEh

Bit	7	6	5	4	3	2	1	0
Name	Res				gamma_val[3:0]			
Value (e.g.)	0001				9h			

gamma_val : Gamma correction value select (1.7 to 2.2)
4'h5=gamma 1.7
4'h6=gamma 1.8
4'h7=gamma 1.9
4'h8=gamma 2.0
4'h9=gamma 2.1
4'hA=gamma 2.2
other=Reserved (Not Available)

Note) The gamma value affects the display's luminance and contrast ratio.

6. Display Panel Specification

6.1 Optical characteristics

Table 9. Optical Characteristics（at Room Temp.）

Item	Condition		Min.	Typ.	Max.	Unit
Brightness	White raster image		200	220		cd/m^2
Contrast ratio	White raster and Black raster image		100:1	150:1		-
xy chromaticity	White raster image	x	0.284	0.299	0.314	-
		y	0.300	0.315	0.330	-

Note: Measurement conditions of the optical characteristics are as follows.

[Measurement condition]

Supply voltage	:	VCC=1.80V, VCCX=3.30V, VIO_serial=3.30V, AVCC=5.00V
Video signal input	:	24bit RGB, Resolution:1280x960 (White) R=FFh, G=FFh, B=FFh (Black) R=00h, G=00h, B=00h
Gamma Correction	:	2.1
LED brightness register	:	Set ‘led_bright_ratio’ register to maximum (3Fh)
Clock / Field Frequency	:	Clock=75MHz, Field rate=60Hz
Temperature	:	Room temperature (25C Typ.)
Luminance and Color meter	:	CS-100A (Konica minolta)
xy chromaticity	:	Measured on white raster image
Brightness	:	Measured on white raster image
Contrast ratio	:	Calculated by white luminance vs black luminance

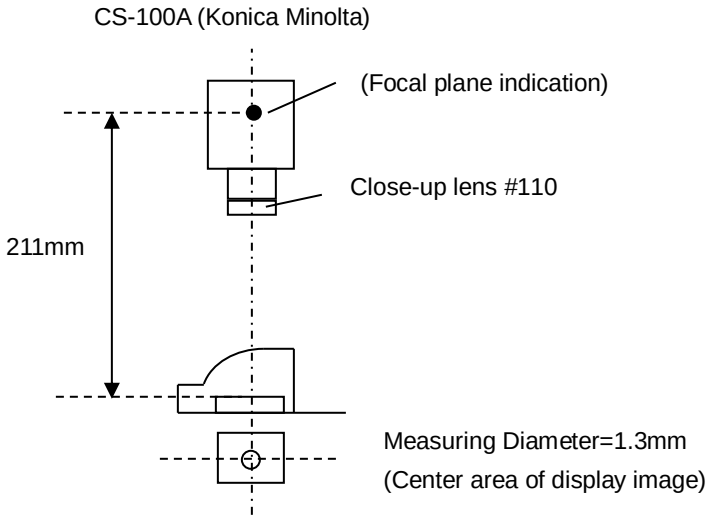


Fig.12 Optical measurement

7. Serial Number

7.1 Serial Number

1) Serial No

X X XXXXXX X
a b c d

a: Manufacturing Year – Last digit of the western calendar year.

b: Manufacturing Month – shown by a letter as below.

Jan	:	A	Jul	:	G
Feb	:	B	Aug	:	H
Mar	:	C	Sep	:	I
Apr	:	D	Oct	:	J
May	:	E	Nov	:	K
Jun	:	F	Dec	:	L

c: Serial No (6digits maximum)

d: CFD control code (1digit Number or Alphabet)

2) Label position

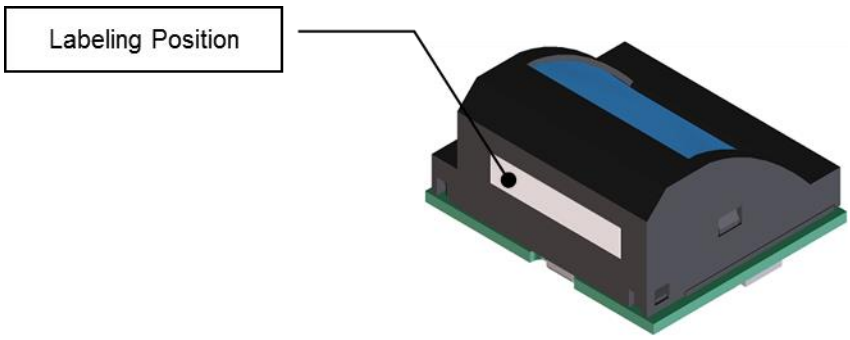


Fig.13 Labeling position

8. Environmental Standards and Export Trade Control Order

8.1 Environmental Standards

The product is compliant with RoHS Directive [EUROPEAN DIRECTIVES 2002/95/EC on the restriction of the use of certain hazardous substances in electrical and electronic equipment].

8.2 Export Trade Control Order

Rows 1 to 15 of Appended Table 1 of Export Trade Control Order are not applicable to the product.

9. Others

9.1 Notes of others

When the issue that is not described in this document arises, the both parties will mutually solve it.