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(V) Preliminary Specifications
( ) Final Specifications

Module	**10.1”WUXGA 16:10 Color TFT-LCD**
Model Name	**G101UAN04.0**
Note	***LED Backlight without driving circuit design***

Company	**Approved by** LeaDer Feng **Date** 2023/07/24
Checked & Approved by **Date**	**Prepared by** Jon Tseng 2023/07/24
	General Display Business Unit / AUO Display Plus Corporation

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Record of Revision

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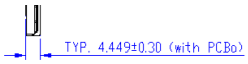
	24		
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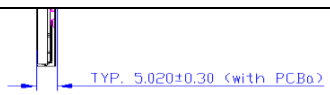
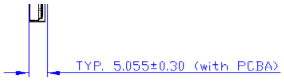
	24		

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<tr><td></td><td>Ry</td><td>0.305</td><td>0.335</td><td>0.365</td></tr>
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1. Operating Precautions

1) Since front polarizer is easily damaged, please be cautious and not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or soft cloth.
5) Since the panel is made of glass, it may be broken or cracked if dropped or bumped on hard surface.
6) To avoid ESD (Electro Static Discharde) damage, be sure to ground yourself before handling TFT-LCD Module.
7) Do not open nor modify the module assembly.
8) Do not press the reflector sheet at the back of the module to any direction.
9) In case if a module has to be put back into the packing container slot after it was taken out from the container, do not press the center of the LED light bar edge. Instead, press at the far ends of the LED light bar edge softly. Otherwise the TFT Module may be damaged.
10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) TFT-LCD Module is not allowed to be twisted & bent even force is added on module in a very short time. Please design your display product well to avoid external force applying to module by end-user directly.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13) Severe temperature condition may result in different luminance, response time and lamp ignition voltage.
14) Continuous operating TFT-LCD display under low temperature environment may accelerate lamp exhaustion and reduce luminance dramatically.
15) Continuous displaying fixed pattern may induce image sticking. It's recommended to use screen saver or shuffle content periodically if fixed pattern is displayed on the screen.
16) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.

2. General Description

G101UAN04.0 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:10 WUXGA, 1200(H) x1920(V) screen and 16.7M colors (Real 8 bits) without LED backlight driving circuit. All input signals are MIPI interface compatible.
G101UAN04.0 is designed for a display unit of tablet application and industrial machine.
G101UAN04.0 is a RoHS product.

2.1 Display Characteristics

The following items are characteristics summary on the table under 25 ºC condition:

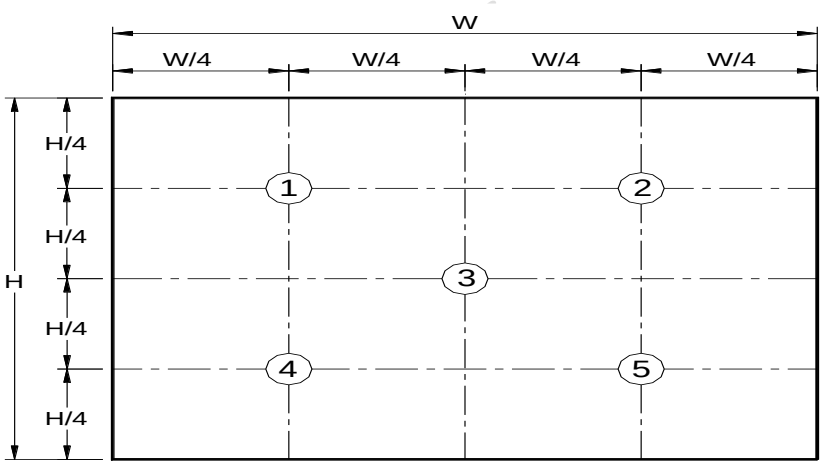
Items	Unit	Specifications			
Screen Diagonal	[mm]	255.40			
Active Area	[mm]	135.36(H) x 216.58(V)			
Pixels H x V		1200 x 3(RBG) x 1920			
Pixel Pitch	[mm]	0.1128 X 0.1128			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		AHVA, Normally Black			
White Luminance	[cd/m2]	500 typ. (center point)			
Luminance Uniformity	δ_{5P}	5P Max. 1.25			
Contrast Ratio		900:1 (Typ.)			
Response Time	[ms]	Typ.30			
Input Voltage VDD	[Volt]	+3.3V typ.			
Power Consumption	[Watt]	Logic: 0.45W @ full white pattern BLU: 2.1 W (max)			
Weight	[Grams]	167 g Max			
Physical Size	[mm]		Min	Typ	Max
		Length	141.8	142.1	142.4
		Width	228.25	228.55	228.85
		Thickness	2.532 4.755	2.690 (Panel side) 5.055 (PCBA side) Without protection Film	2.95 5.355
Electrical Interface		4 lane MIPI			
Surface Treatment		Glare			
Support Color		16.7M colors			
Temperature Range Operating Storage (Non-Operating)	[ºC] [ºC]	-10 to +50 -20 to +60			
RoHS Compliance		RoHS Compliance			

2.2 Optical Characteristics

The optical characteristics are measured under stable conditions at 25 °C (Room Temperature):

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance			Center Point	400	500	---	cd/m^2	1, 3, 4.
Viewing Angle		θ_R θ_L	Horizontal (Right) CR ≧ 10 (Left)	80 80	89 89	---	degree	3, 8
		ψ_H ψ_L	Vertical (Upper) CR ≧ 10 (Lower)	80 80	89 89	---		
Luminance Uniformity		%	5 Points	80	---	---		1, 2, 3
Contrast Ratio		CR		800	900	---		3, 5
Cross talk		%		---	---	2		3, 6
Response Time		T_{RT}	Rising + Falling	---	30	35	msec	3, 7
Color / Chromaticity Coordinates	Red	Rx	CIE 1931	0.608	0.638	0.668		3
		Ry		0.305	0.335	0.365		
	Green	Gx		0.295	0.325	0.355		
		Gy		0.589	0.619	0.649		
	Blue	Bx		0.127	0.157	0.187		
		By		0.022	0.052	0.082		
	White	Wx		0.283	0.313	0.343		
		Wy		0.299	0.329	0.359		
NTSC		%			70			

Note 1: 5 points position (Ref: Active area)

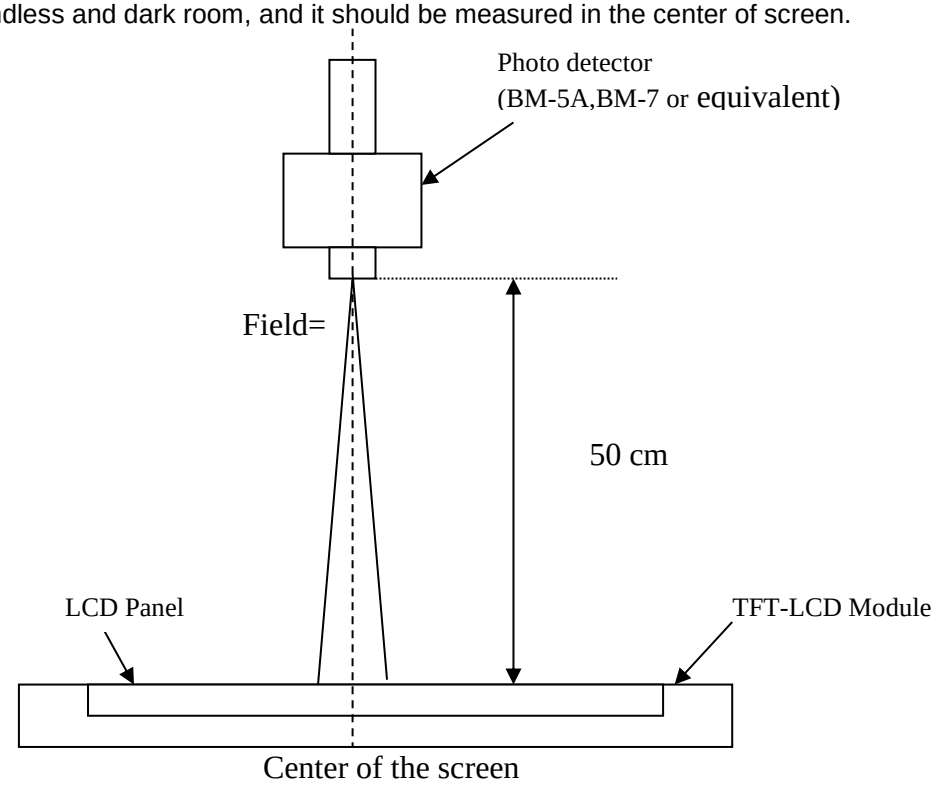


Note 2: The luminance uniformity of 5 points is defined as minimum luminance divided by the maximum luminance values:

$$\delta_{W5} = \frac{\text{Minimum Brightness of five points}}{\text{Maximum Brightness of five points}}$$

Note 3: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 4： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 5： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

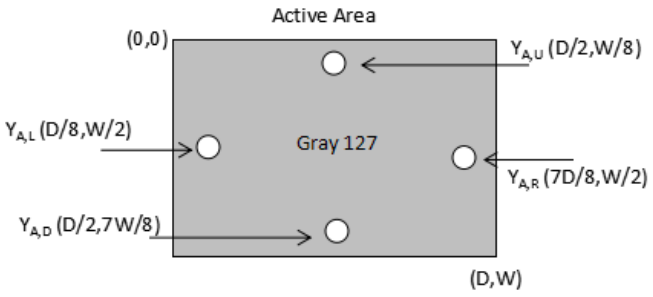
Note 6： Definition of Cross Talk (CT)

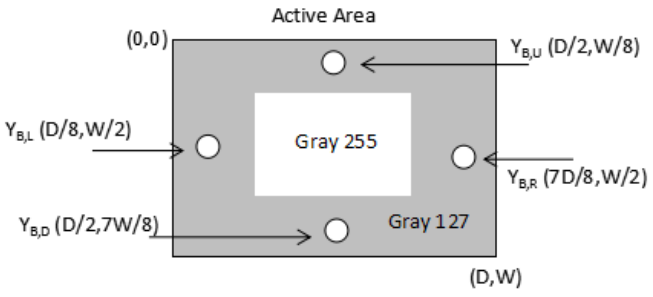
CT = | YB – YA | / YA × 100 (%)

Where

YA = Luminance of measured location without gray level 255 pattern (cd/m2)

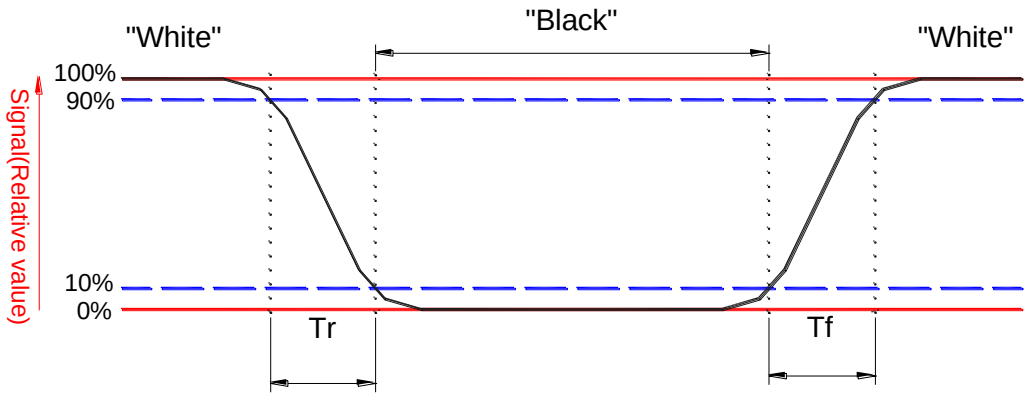
YB = Luminance of measured location with gray level 255 pattern (cd/m2)





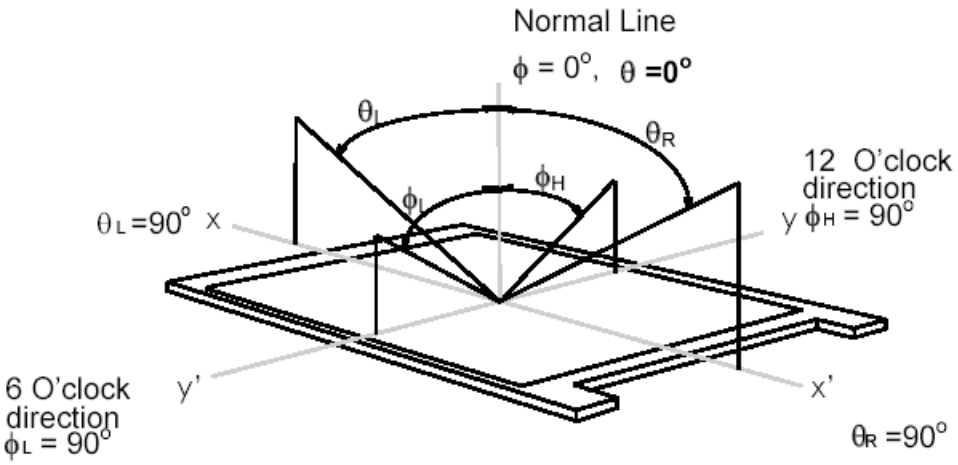
Note 7: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



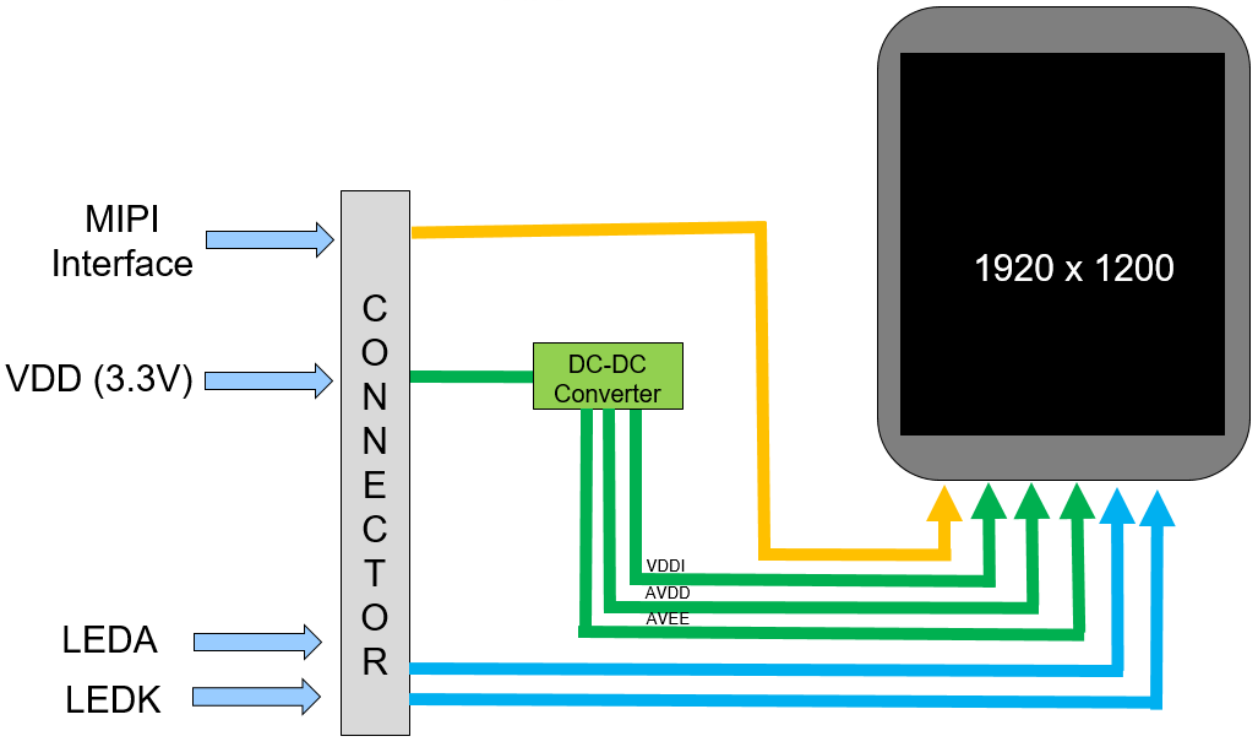
Note 8. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 10.1 inches wide Color TFT/LCD 45 Pin four channel Module



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage	VDD	-0.3	+6.0	[Volt]	Note 1,2

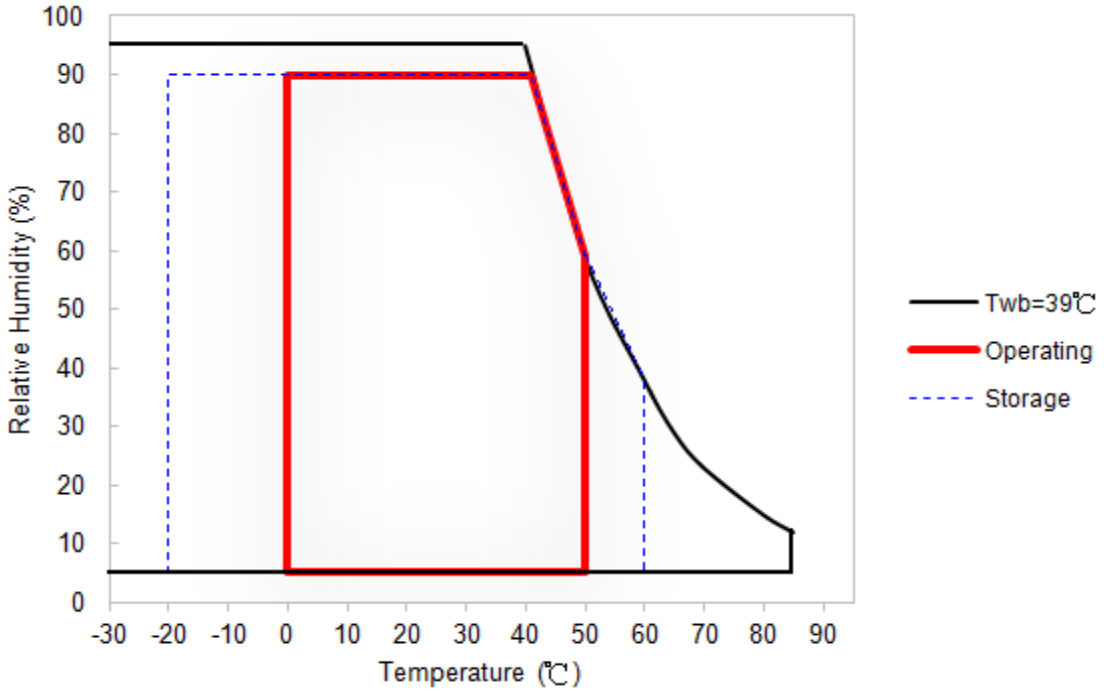
4.2 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 3
Operation Humidity	HOP	5	95	[%RH]	Note 3
Storage Temperature	TST	-20	+60	[°C]	Note 3
Storage Humidity	HST	5	95	[%RH]	Note 3

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows. The power specification are measured under 25℃ and frame frequency under 60Hz

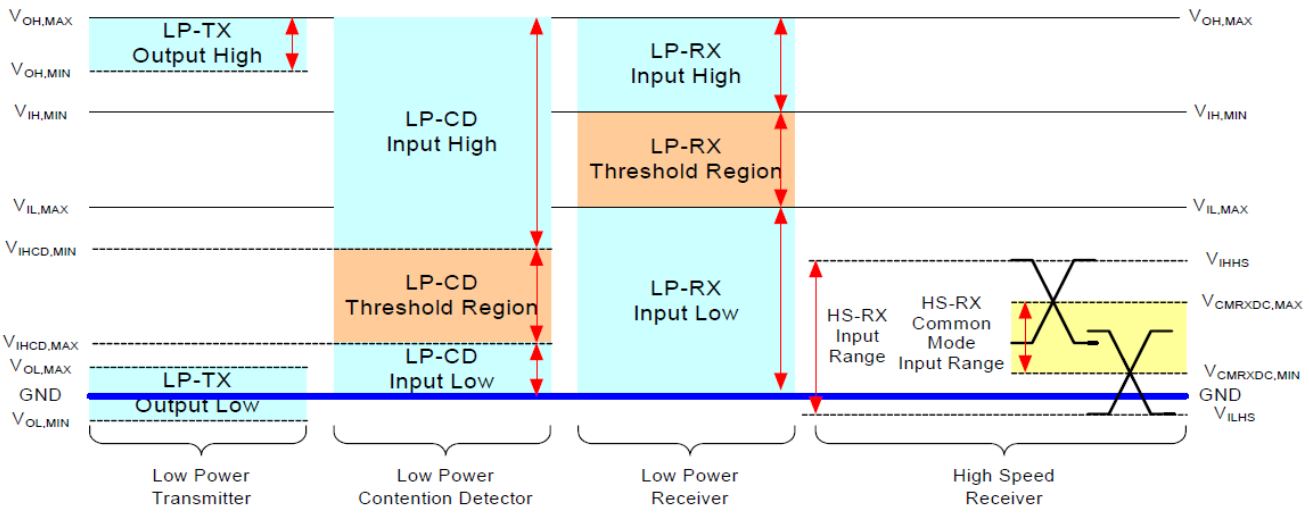
Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
P_{VDD}	VDD Power Consumption	-	0.45	-	[Watt]	Note 1
I_{VDD}	VDD Current	-	136	-	[mA]	Note 1
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	
VIH	MIPI Logic High-level Input Voltage(*Except REST*)	1.26	1.8	1.95	[Volt]	
VIL	MIIP Logic Low-level Input Voltage(*Except REST*)	0	-	0.54	[Volt]	
VIH	Logic High-level Input Voltage(*RESET*)	1.44	1.8	1.95	[Volt]	
VIL	Logic Low-level Input Voltage(*RESET*)	0	-	0.36	[Volt]	
VOH	MIPI Logic High-level Output Voltage	1.44	-	1.8	[Volt]	
VOL	MIPI Logic Low-level Output Voltage	0	-	0.36	[Volt]	

Note 1 : Typical power consumption is measured in white pattern @ 60Hz.
Note 2 : VIH max to be VDDI typ +0.15V

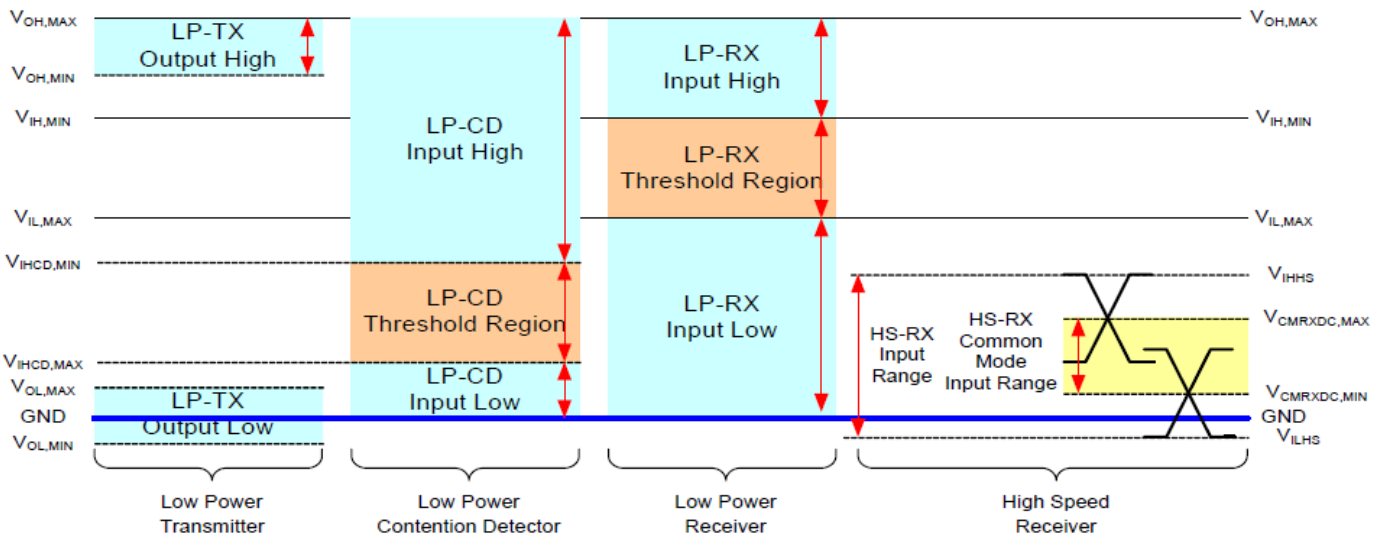
5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.
MIPI DC characteristics are as follows:

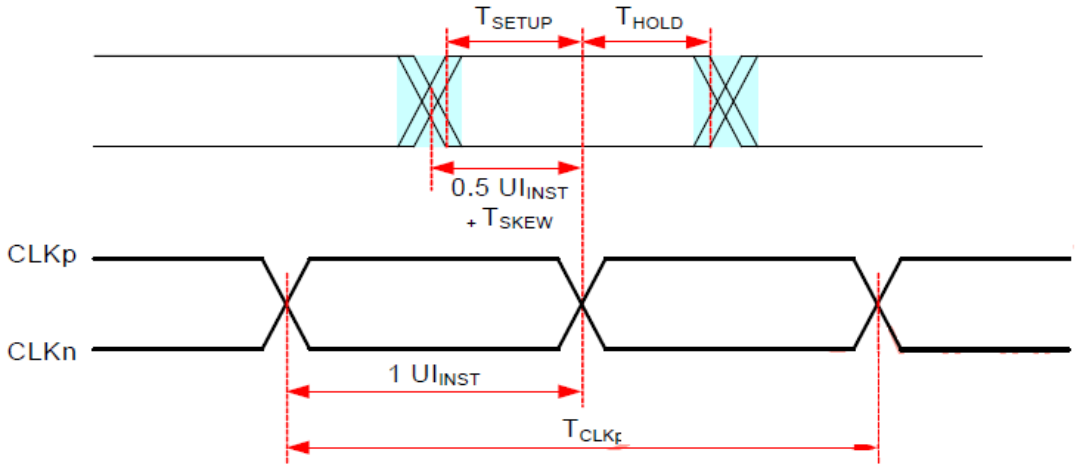
MIPI DPHY DC Characteristics					
Symbol	Parameter	Min	Typ	Max	Unit
Power and Operation Voltage for MIPI Receiver					
VDDAM	Power supply voltage for MIPI RX	1.65	1.8	1.95	V
VP_HSSI	High speed / Low power mode operating voltage		1.2		V
MIPI Characteristics for High Speed Receiver					
VILHS	Single-ended input low voltage	-40			mV
VIHHS	Single-ended input high voltage			460	mV
VCMRXDC	Common-mode voltage	70		330	mV
ZID	Differential input impedance	80	100	125	ohm
|VOD|	HS transmit differential voltage (VOD=VDP-VDN)	140	200	250	mV
VIDTH	Different input high threshold			70	mV
VIDTL	Different input low threshold	-70			mV
VTERM-EN	Single-ended threshold for HS termination enable			450	mV
MIPI Characteristics for Low Power Mode					
VI	Pad signal voltage range	-50		1350	mV
VGNDSH	Ground shift	-50		50	mV
VIL	Logic 0 input threshold	0		550	mV
VIH	Logic 1 input threshold	880		VDDAM	mV
VHYST	Input hysteresis	25			mV
VOL	Output low level	-50		50	mV
VOH	Output high level	1.1	1.2	1.3	V
ZOLP	Output impedance of Low Power Transmitter	80	100	125	ohm
VIHCD,MAX	Logic 0 contention threshold	0		200	mV
VILCD,MIN	Logic 1 contention threshold	450		VDDAM	mV



MIPI CPHY DC Characteristics					
Symbol	Parameter	Min	Typ	Max	Unit
Power and Operation Voltage for MIPI Receiver					
VDDI	Power supply voltage for MIPI RX	1.65	1.8	1.95	V
VDD	High speed / Low power mode operating voltage		1.2		V
MIPI Characteristics for High Speed Receiver					
VILHS	Single-ended input low voltage	-40			mV
VIHHS	Single-ended input high voltage			535	mV
VCMRXDC	Common-mode voltage	95		390	mV
ZID_AB ZID_BC	Differential input impedance	80	100	120	ohm
VIDTH	Different input high threshold			40	mV
VIDTL	Different input low threshold	-40			mV
VTERM-EN	Single-ended threshold for HS termination enable			450	mV
MIPI Characteristics for Low Power Mode					
VPIN	Pad signal voltage range	-50		1350	mV
VGNDSH	Ground shift	-50		50	mV
VIL	Logic 0 input threshold	0		550	mV
VIH	Logic 1 input threshold	740			mV
VHYST	Input hysteresis	25			mV
VOL	Output low level	-50		50	mV
VOH	Output high level	0.95	1.2	1.3	V
ZOLP	Output impedance of Low Power Transmitter	110			ohm
VIHCD,MAX	Logic 1 contention threshold	450			mV
VILCD,MIN	Logic 0 contention threshold			200	mV



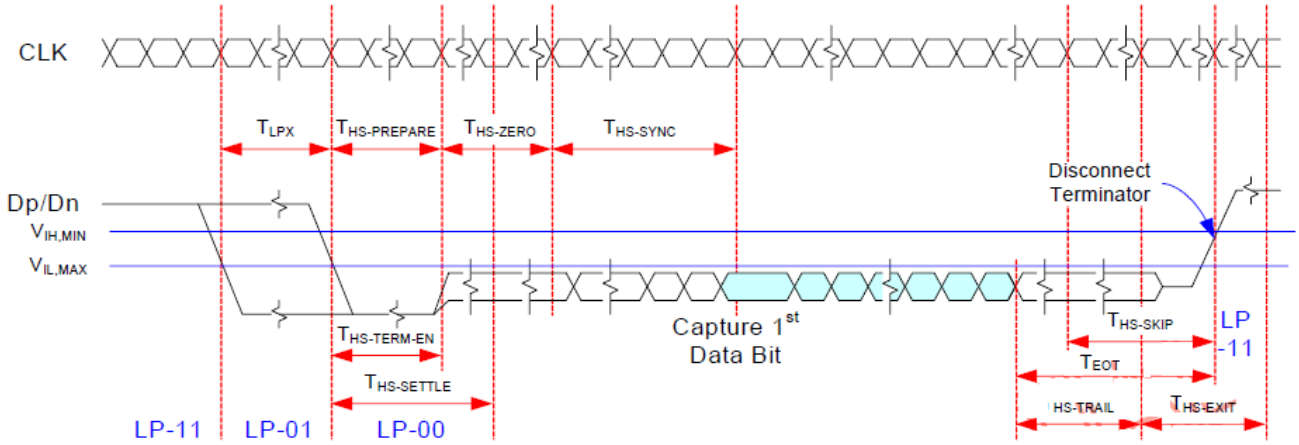
High Speed Data Transmission: Data-Clock Timing



Symbol	Parameter	Min	Typ	Max	Units	Notes
UIINST	UI instantaneous	0.833		4	ns	1,2,10
TSKEW[TX]	Data to Clock Skew [measured at tansmitter]	-0.15		0.15	UIINST	3
		-0.2		0.2	UIINST	4
TSETUP[RX]	Data to Clock Setup Time [measured at receiver]	-0.15		0.15	UIINST	5
		-0.2		0.2	UIINST	6
THOLD[RX]	Data to Clock Hold Time [measured at reciever]	-0.15		0.15	UIINST	5
		-0.2		0.2	UIINST	6
tR/ tF	20% -80% rise time and fall time	100			ps	9
				0.3	UIINST	7
				0.35	UIINST	8

Note:
1. This value corresponds to a minimum 80 MHz data rate.
2. The minimum UI shall not be violated for any single bit period, i.e.,any DDR half cycle within a data burst.
3. Total silicon and package delay budget of 0.3* UIINSTwhen D-PHY is supporting maximum data rate = 1Gbps.
4. Total silicon and package delay budget of 0.4* UIINSTwhen D-PHY is supporting maximum data rate > 1Gbps.
5. Total setup and hole window for receiver of 0.3* UIINSTwhen D-PHY is supporting maximum data rate = 1Gbps.
6. Total setup and hole window for receiver of 0.4* UIINSTwhen D-PHY is supporting maximum data rate > 1Gbps.
7. Applicable when operating at HS bit rates ≤ 1 Gbps (UI ≥ 1 ns).
8. Applicable when operating at HS bit rates > 1 Gbps (UI < 1 ns).
9. Applicable for all HS bit rates. However, to avoid excessive radiation, bit rates ≤ 1 Gbps (UI ≥ 1 ns), should not use values below 150 ps.
10. For MIPI speed limitation:
    10.1. Per lane bandwidth is 1Gbps,
    10.2. Total Bit Rate: 4Gbps for 8-8-8; and 2.67Gbps for5-6-5.

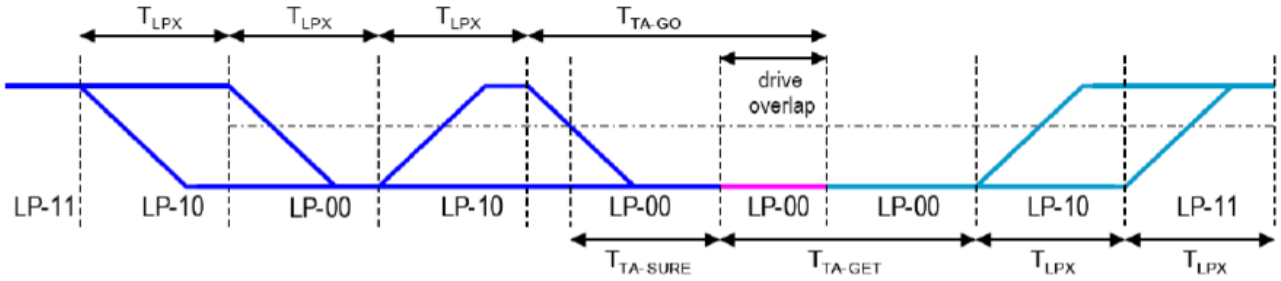
High-Speed Data Transmission in Bursts



Symbol	Parameter	Min	Typ	Max	Units
THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40+4UI		85+6UI	ns
TEOT	Time from start of tHS-TRAIL or tCLK-TRAIL period to start of LP-11 state			105+12UI	ns
THS-TERM-EN	Time to enable Data Lane receiver line termination measured from when Dn cross VIL,MAX			35+4UI	ns
THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4UI			ns
THS-SKIP	Time-out at RX to ignore transition period of EoT	40		55+4UI	ns
THS-EXIT	Time to drive LP-11 after HS burst	100			ns
TLPX	Length of any Low-Power state period	50			ns
THS-SYNC	Sync sequence period		8UI		ns
THS-ZERO	Minimum lead HS-0 drive period before the Sync sequence	105+6UI			ns

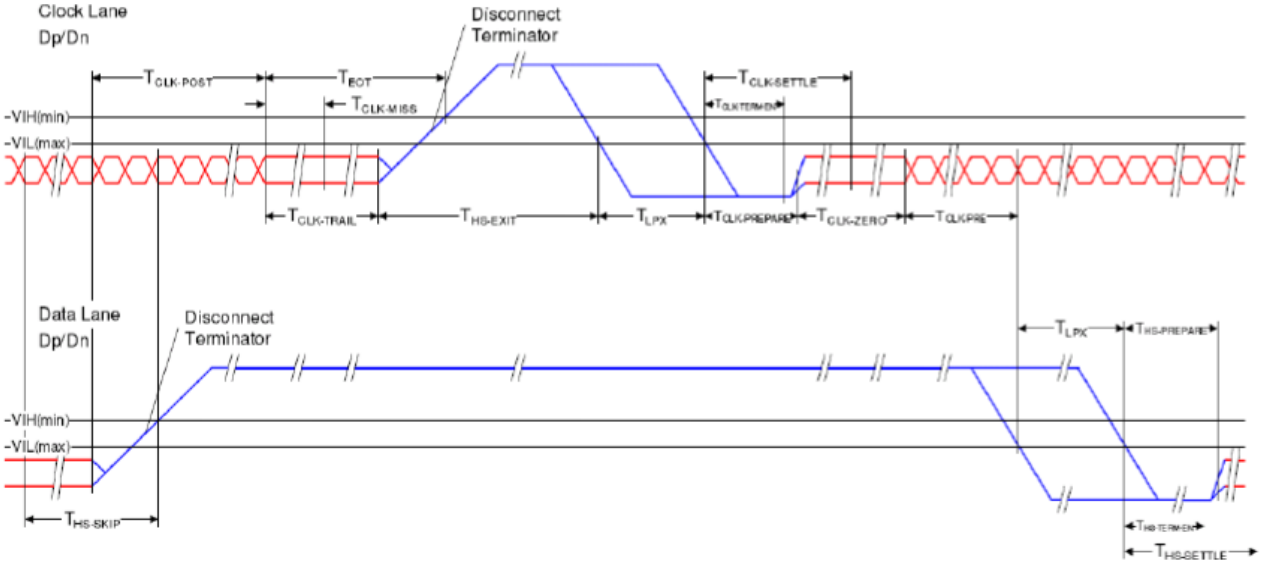
Note:
1: The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.
2: UI means Unit Interval, equal toone half HS the clock period on the Clock Lane.
3: TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

Turnaround Procedure



Symbol	Parameter	Min	Typ	Max	Units
TLPX	Length of any Low-Power state period : Master side	50		75	ns
TLPX	Length of any Low-Power state period : Slave side	50		75	ns
Ratio TLPX	Ratio of TLPX(MASTER)/TLPX(SLAVE) between Master and Slave side	2/3		3/2	
TTA-SURE	Time-out before new TX side start driving	TLPX		2TLPX	ns
TTA-GET	Time to drive LP-00 by new TX		5TLPX		ns
TTA-GO	Time to drive LP-00 after Turnaround Request		4TLPX		ns

Switching the Clock Lane between Clock Transmission and Low-Power Mode



Symbol	Parameter	Min	Typ	Max	Units
TCLK-POST	Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode. ***Note: Due to this value need to correspond with a minimum 500 Mbps data rate***	60+**52**UI			ns
TCLK-MISS	Detection time that the clock has stopped toggling			60	ns
TCLK-PREPARE	Time to drive LP-00 to prepare for HS clock transmission	38		95	ns
TCLK-PREPARE+TCLK-ZERO	Minimum lead HS-0 drive period before starting Clock	300			ns
THS-TERM-EN	Time to enable Clock Lane receiver line termination measured from when Dn cross VIL,MAX			38	ns
TCLK-PRE	Minimum time that the HS clock must be set prior to any associated date lane beginning the transmission from LP to HS mode	8			UI
TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60			ns

5.2 Backlight Unit

5.2.1 LED characteristic

Following characteristics are measured under a stable condition using an inverter at 25℃ (Room Temperature):

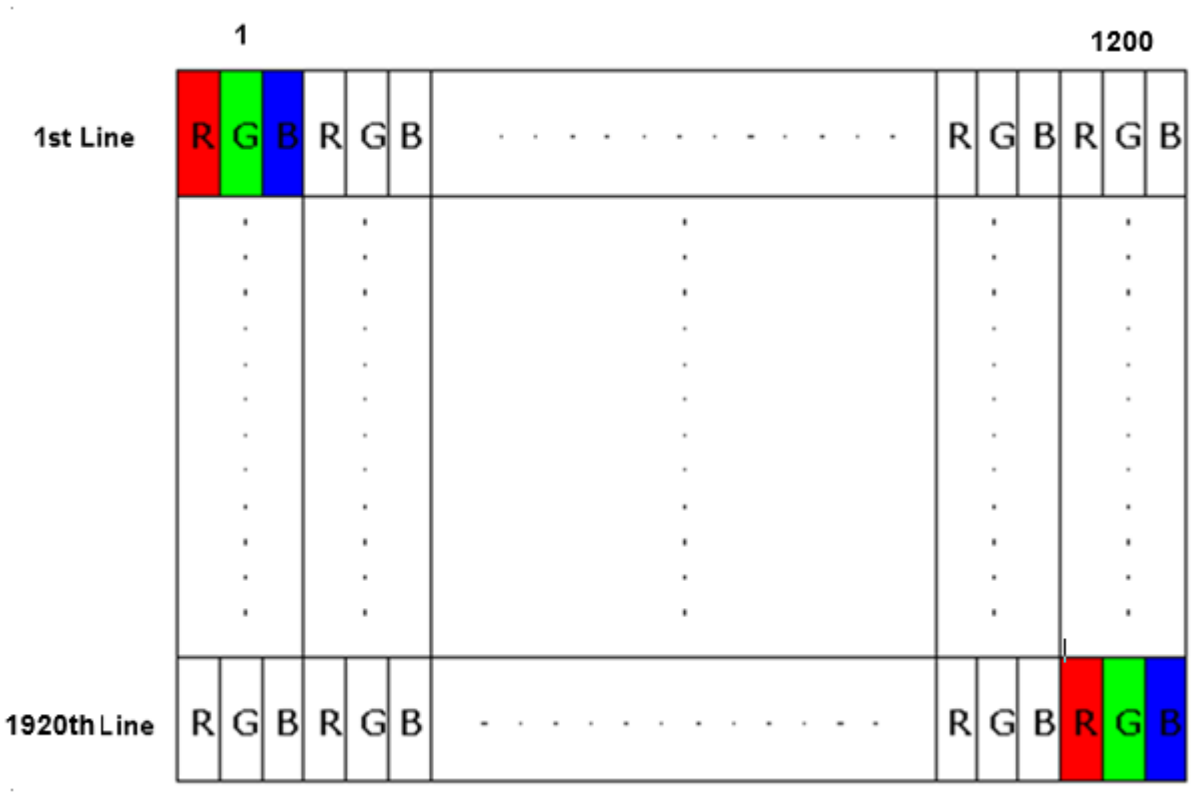
Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption (W/O Efficiency)	PLED		2.0	2.1	[Watt]	Note 1 (Ta= 25℃)
LED Forward Voltage	VF		2.85	3.0	[Volt]	(Ta= 25℃)
LED Forward Voltage of every LED string	Vf-string		19.95 (2.85X7)	21 (3.0X7)	[Volt]	(Ta= 25℃)
LED Forward Current	IF		25		[mA]	(Ta= 25℃)
LED Forward Current of every LED string	IF-string		100 (25X4)		[mA]	(Ta= 25℃)
LED Life time	N/A	≧15000			Hour	Note 1 (Ta=25℃)

Note 1: calculator value for reference PLED based on 25 mA

6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship between input signal and LCD pixel format.



6.2 Integration Interface Requirement

6.2.1 MIPI Connector Description

Physical interface is described as for the connector on module.
These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	Panasonic
Type / Part Number	AYF564035
Mating Housing/Part Number	FPC

6.2.2 MIPI Pin Assignment

MIPI is a differential signal technology for LCD interface and high speed data transfer device.

Pin No.	Symbol	Description	I/O
1	GND	Ground	P
2	NC	Reserved for Analog Operating Voltage	-
3	NC	Reserved for Analog Operating Voltage	-
4	ID0	ID0 – high level (+1.8V)	I/O
5	ID1	ID0 – high level (+1.8V)	I/O
6	NC	Reserved for Analog Operating Voltage	-
7	NC	Reserved for Analog Operating Voltage	-
8	GND	Ground	P
9	D3N	MIPI differential data3 input (Negative)	I
10	D3P	MIPI differential data3 input (Positive)	I
11	GND	Ground	P
12	D0N	MIPI differential data0 input (Negative)	I
13	D0P	MIPI differential data0 input (Positive)	I
14	GND	Ground	P
15	CLKN	MIPI differential clock input (Negative)	I
16	CLKP	MIPI differential clock input (Positive)	I
17	GND	Ground	P
18	D1N	MIPI differential data1 input (Negative)	I
19	D1P	MIPI differential data1 input (Positive)	I
20	GND	Ground	P
21	D2N	MIPI differential data2 input (Negative)	I
22	D2P	MIPI differential data2 input (Positive)	I
23	GND	Ground	P
24	LED PWMO	LED PWM Out	O
25	TE	Tearing Effect Pin	O
26	RESET	RESET Display (Typ:+1.8V)	I
27	VDD	Power Supply (Typ:+3.3V)	P
28	VDD	Power Supply (Typ:+3.3V)	P
29	GND	Ground	P
30	NC	Reserved for I2C Clock for Touch (Typ:+1.8V)	I
31	NC	Reserved for I2C Data for Touch (Typ:+1.8V)	I/O
32	NC	Reserved for Interrupt for Touch (Typ:+1.8V)	I
33	NC	No Connect	-
34	GND	Ground	P
35	NC	No Connect	-
36	LEDA	Power for LED Anode	P
37	LEDA	Power for LED Anode	P
38	NC	No Connect	-
39	LEDK	Power for LED Cathode	P
40	LEDK	Power for LED Cathode	P

6.3 MIPI Interface Timing

6.3.1 Timing Characteristics

Basically, interface timings should match the 1200 x 1920 /60 Hz manufacturing guide line timing.

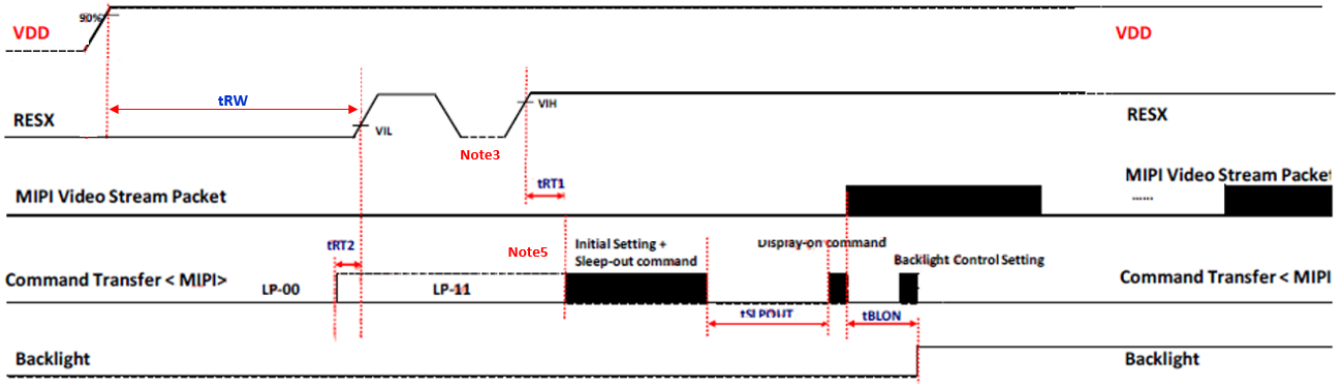
Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		---	59.7	60.0	60.3	Hz
Clock frequency		fCLK		157.6		MHz
Vertical	Vertical total time	tvp		2037		tH
	Vertical Active time	tVadr	1920			
	Vertical Pulse Width	tVsync		1		
	Vertical Back Porch	tVBP		86		
	Vertical Front Porch	tVFP		30		
Horizontal	Horizontal total time	tHP		1289		tCLK
	Horizontal Active time	tHadr	1200			
	Horizontal Pulse Width	tHsync		1		
	Horizontal Back Porch	tHBP		44		
	Horizontal Front Porch	tHFP		44		
Bit Rate		TX SPD (MBPS)		1020		Mbps

6.4 Power ON/OFF sequence

6.4.1 Power

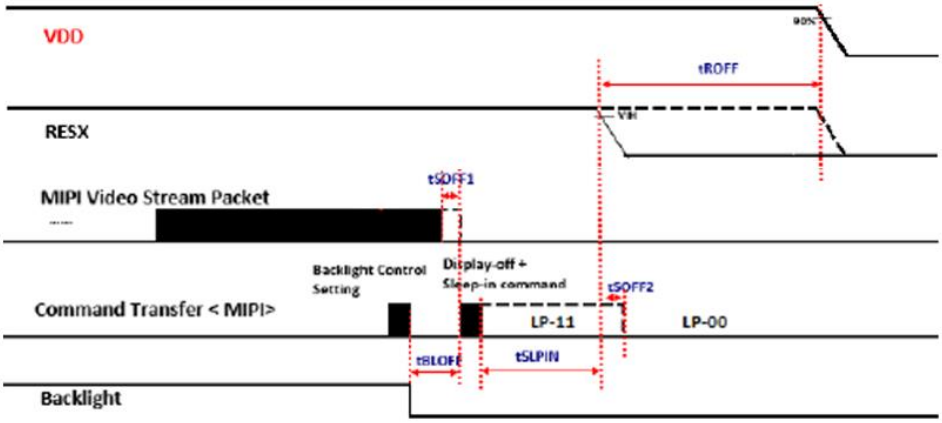
Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart.

<Power on>



Note 1: After Sleep-Out Command, Driver IC will reload MTP registers and do internal power on action. Therefore, any initial settings (such as 3Ah, 3Bh, etc.) by MIPI should be set after Sleep-Out command with minimum delay time 100mS.
Note 2: For detailed panel-related power sequence, please refer to NT36523 Application Notes.
Note 3: Two finger Reset is necessary.
Note 4: MIPI sleepout = 0x11 ; sleep in = 0x10 ; display on = 0x29 ; display off = 0x28
Note 5: MIPI pull LP-00 to LP-11 time is allowed during dotted line interval, moreover, if this LP-00 to LP-11 time behind last RESX=High which will cause a MIPI false control error report.

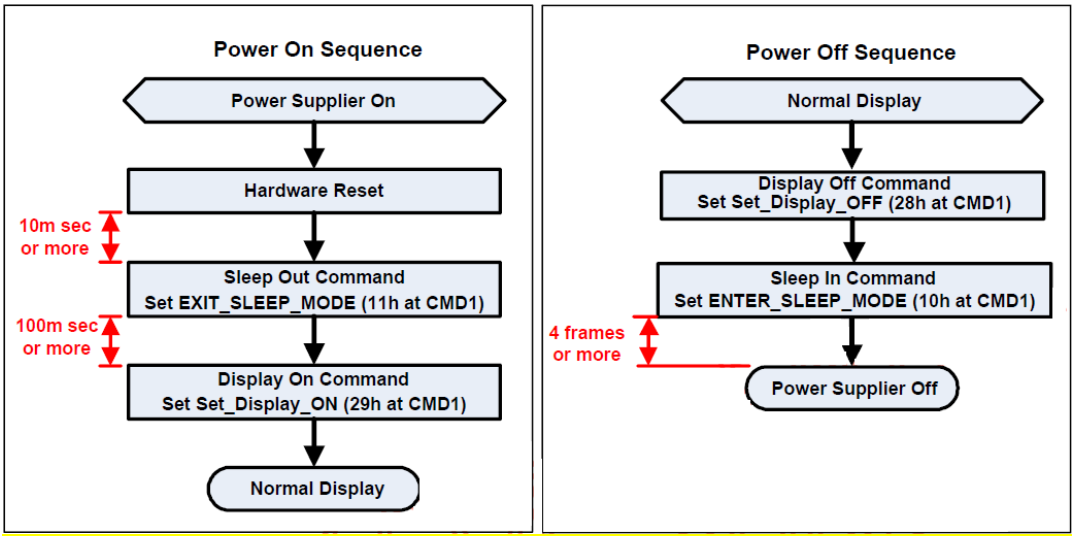
<Power off>



Item	Symbol	Condition	Min	Typ	Max	Unit
All Power On to RESX Hi-level time (90% to VIL)	tRW	Power On	10			ms
(MIPI goes to LP11 state) to RST goes to Low-level (VIL)	tRT2	Power On		0		ms
RST Hi-level (VIH) to 1st Command time	tRT1	Power On	10			ms
SLPOUT Sequence Request time	tSLPOUT	Power On	100			ms
MIPI Video Stream On time to BL On time	tBLON	Power On	40			ms
RST Low to VDD Off time (VIH to 90%)	tROFF	Power Off	0			us
BL Off to Display Off Command time	tBLOFF	Power Off	0			us
SLPIN Sequence Request time	tSLPIN	Power Off	60			ms
VDD regulator turn off time	tVDDOFF	Suspend	20		80	ms

MIPI Video Stream Off time to DISPLAY OFF command	tSOFF1	Power Off	0			us
RST goes to Low-level (VIH) to (MIPI goes to LP00 state)	tSOFF2	Power Off	0			us

The power supply on/off setting for Display ON/OFF, Standby Set/Exit, and Sleep Set/Exit sequences in figure below.



6.4.2 MIPI Command

COMMAND	ADDRESS	PARAMETER
REGW	0xFF	0xD0
REGW	0xFB	0x01
REGW	0x00	0x33
REGW	0xFF	0x2A
REGW	0xFB	0x01
REGW	0xF1	0x03
REGW	0xFF	0x20
REGW	0xFB	0x01
REGW	0x30	0x10
REGW	0xFF	0x10
REGW	0xFB	0x01
REGW	0x35	0x00
REGW	0x51	0x0F, 0xFF
REGW	0x53	0x2C
REGW	0x55	0x00
REGW	0xB2	0x80
REGW	0xB3	0x00
REGW	0xBB	0x13
REGW	0x3B	0x03 , 0x57 , 0x1E , 0x04 , 0x04 , 0x00
REGW	0x11	0x00
REGW	0x29	0x00

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

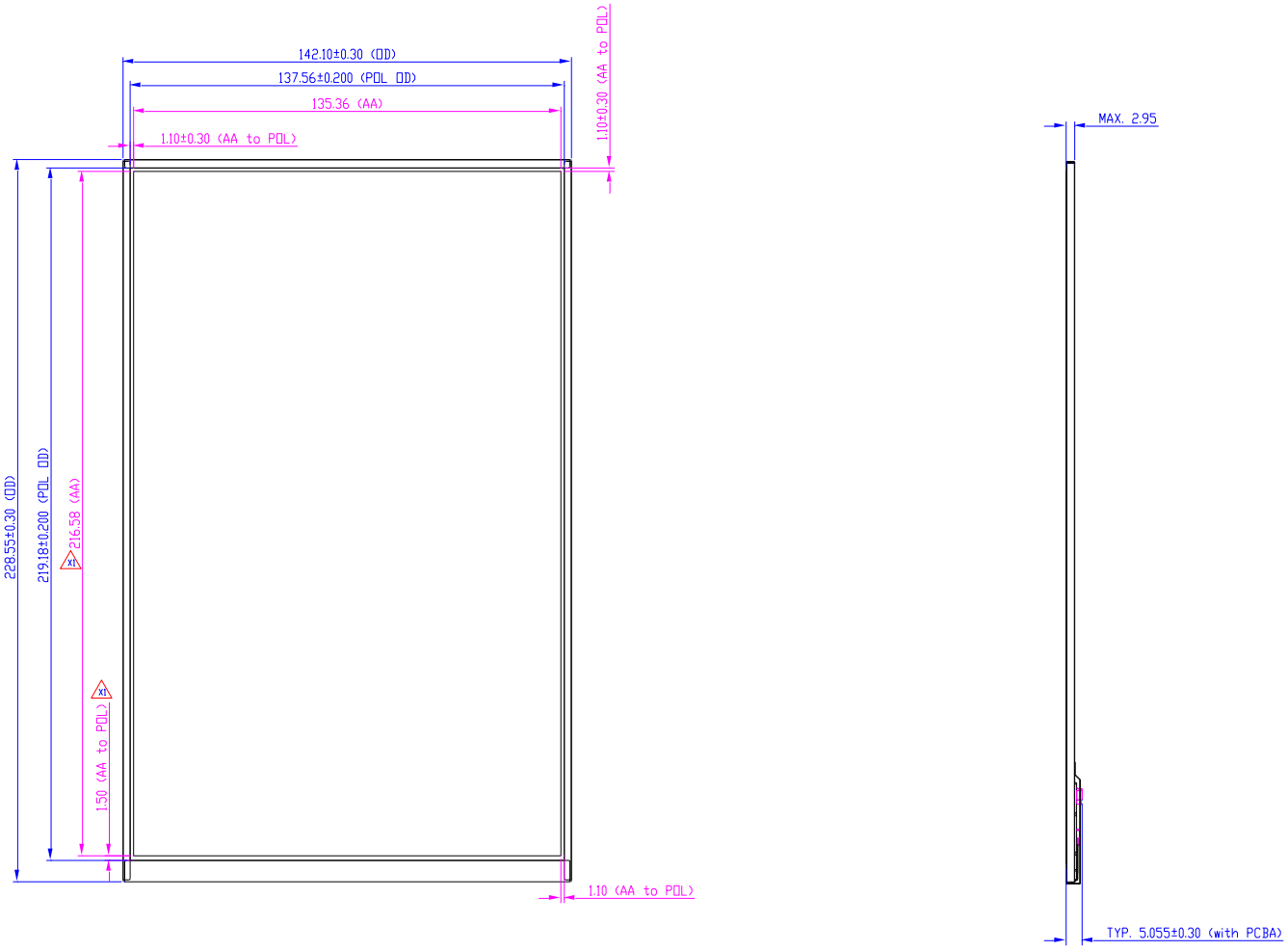
Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 90%RH, 300h	
High Temperature Operation	Ta= 50℃, Dry, 300h	
Low Temperature Operation	Ta= -10℃, 300h	
High Temperature Storage	Ta= 60℃, 300h	
Low Temperature Storage	Ta= -20℃, 300h	
Thermal Shock Test	Ta=-20℃to 60℃, Duration at 30 min, 100 cycles	
ESD	TBD	Note 1

Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost . Self-recoverable. No hardware failures.

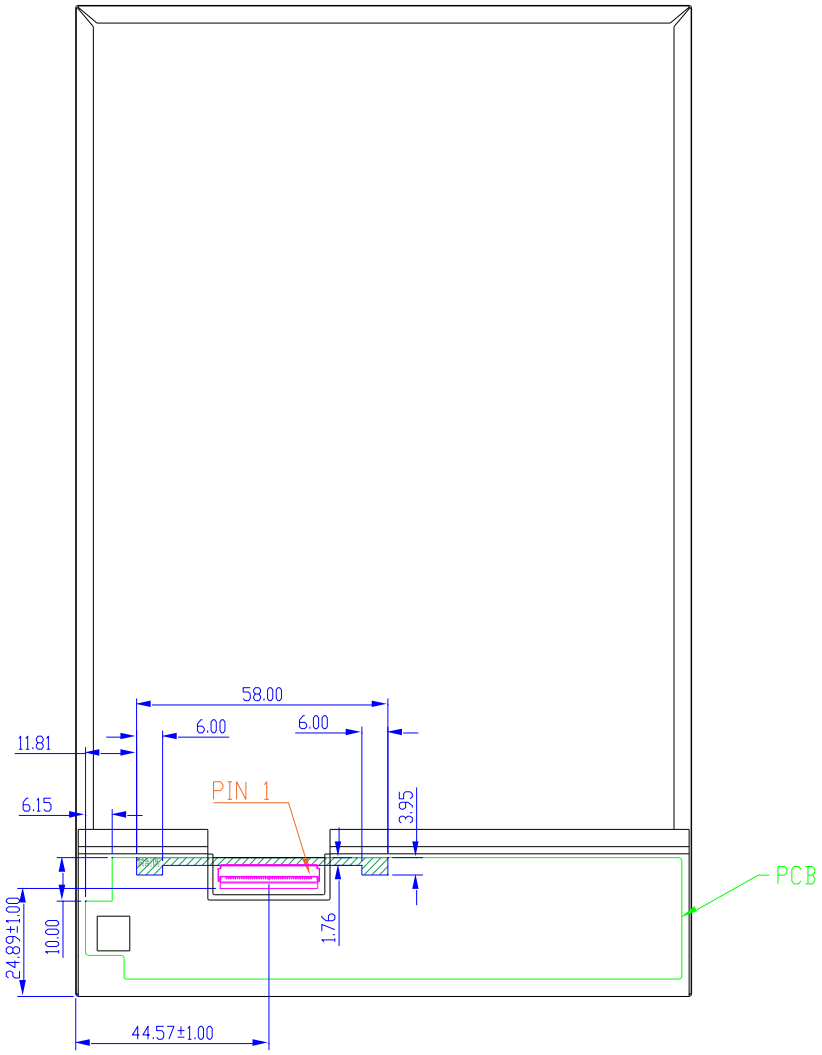
Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

8. Mechanical Characteristics

8.1 LCM Standard Outline Dimension (Front View)



8.2 LCM Standard Outline Dimension (Rear View)



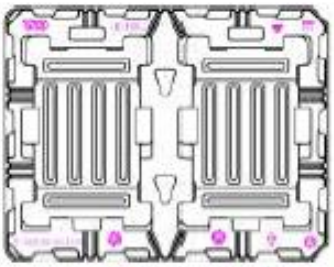
9. Label and Packaging

9.1 Shipping Label (on the rear side of TFT-LCD display)

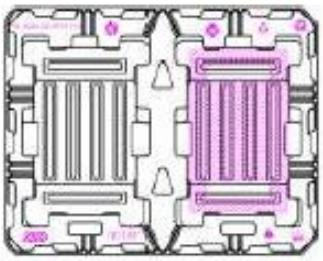
9.2 Carton Label Format

9.3 Shipping Package of Palletizing Sequence

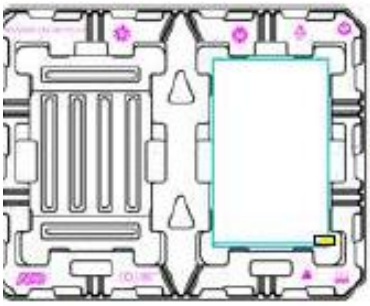
取出 PP 瓦楞板



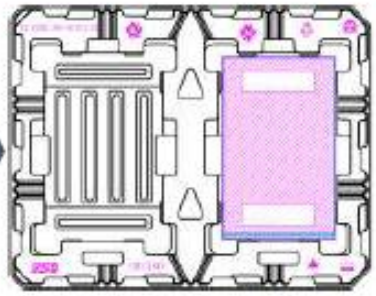
Tray 置放於 PP 瓦楞板上



各放下 EPE SPACER 1 張於 Tray 內穴中，1 穴 1 張



放上產品(AA 面朝上)，1 片 1 穴



各再放入 EPE SPACER1 張於產品上，1 穴 1 張

Tray 依上述方式依序旋轉堆疊，共堆疊 13+1 層 tray(共 26 片產品,最上面第 14 個 tray 為空 tray)

完成堆疊的 tray 放入靜電袋中，並使用 tape 封口

底面和四周的 EPE cushion 放入紙箱

將包好靜電袋的 tray 整疊放入紙箱中

頂面 EPE cushion 放入紙箱

膠帶封箱

Pallet size：1150mm x 840mm x 132mm
Box stacked Max
Module by air：(2 *2) *5 layers，one pallet put 20 boxes，total 520pcs module
Module by sea：One pallet (2 *2) *5 layers + One pallet (2 *2) *1 layers,total 624pcs module
Module by sea_ HQ :One pallet (2 *2) *5 layers + One pallet (2 *2) *2 layers,Total 728 pcs module
Box stacked on pallet (Picture):