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1. BASIC SPECIFICATIONS

LPM013M501A is a 1.342 inch reflective active matrix liquid crystal display (LCD) module.
The Active area of the LCD module has 320(H) x 320(V) pixels.
A sub-pixel has 1-bit static random-access memory (SRAM) to store the image data and
it is capable of displaying 8 colors.
This display is a reflective LCD therefore the specifications are defined in reflective mode only unless otherwise specified in this specification sheet.

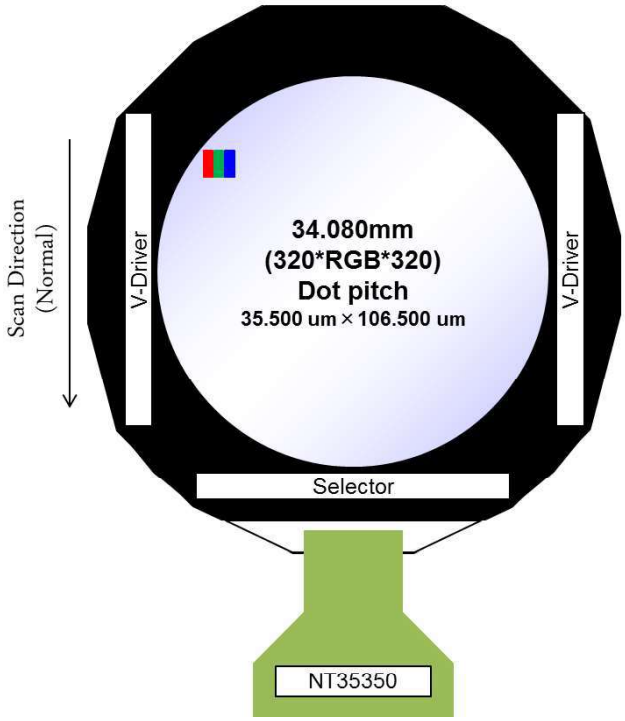
1.1 STRUCTURES

No.	FACTOR	SPECIFICATIONS	UNIT
1	LCD structure	LTPS Analog driving(normal) mode or Memory in Pixel mode	-
2	Outward (W x H x D)	37.68 x 38.49 x 1.835 (*1-1)	mm
3	Weight	3.60	g
4	Screen size	34.08 (1.34 inch) diameter	mm
5	Number of pixels	320(H) x 320(V)	Dot
6	Interface	MIPI-DSI (1lane) &SPI	-
7	Dot pitch (Horizontal x Vertical)	0.0355(H) x 0.1065(V)	mm
8	Dot layout	RGB stripe	-
9	Number of colors	262K colors at normal mode or 8 colors an MIP mode	
10	Liquid crystal mode	ECB normally black (Reflective type)	-
11	Front Polarizer	Hard Coat type (*Pencil Hardness : 2H)	-
12	Rear Polarizer	w/o APCF	-

Note)
(*1-1) Excluding FPC and part of protruding. See attached drawing for details.

1.2 BLOCK DIAGRAM

The block diagram of a panel is shown below.



Viewing in front of an LCD panel
※Driver IC on back side of COF

1.3 INPUT / OUTPUT TERMINAL NAME AND FUNCTIONS

P: Power supply I: Input O: Output

PIN	SYMBOL	TYPE	DESCRIPTION	REMARK
1	DCX	I	Data command select signal	(*1)
2	SCL	I	Synchronous clock signal	
3	SDI	I/O	Serial data input/output	
4	GND	-	GND	
5	HSSI_CLK_P	I	MIPI positive clock signal	
6	HSSI_CLK_N	I	MIPI negative clock signal	
7	GND	-	GND	
8	HSSI_D0_P	I	MIPI positive data signal	
9	HSSI_D0_N	I	MIPI negative data signal	
10	GND	-	GND	
11	NFC_1	I	NFC pin for customer	
12	NFC_1	I	NFC pin for customer	
13	NFC_2	I	NFC pin for customer	
14	NFC_2	I	NFC pin for customer	
15	VCI	P	Power Supply for Analog Circuit	
16	VDDI	P	Power Supply for I/O	
17	RESX	I	Reset pin (Active Low)	
18	GND	-	GND	
19	LEDPWM	O	PWM feedback Signal for LED Driver	
20	TE	O	Frame Head Signal	
21	CSX	I	Chip select signal	
22	IM0	I	Selects the interface to 3/4-Wires Mode SPI	
23	LED_A	P	Power supply for LED backlight anode	
24	LED_K	P	Power supply for LED backlight cathode	

Note)
(*1) If not used, please tie this pin to VDDI.

2. ABSOLUTE MAXIMUM RATINGS

PARAMETER	Symbol	RATINGS	UNIT	REMARKS
Power supply for I/O	VDDI	-0.3 ~ +4.0	V	
Power Supply for Analog Circuit	VCI	-0.3 ~ +5.5	V	
Digital input terminal voltage	VIN	-0.3 ~ VDDI + 0.3	V	
	VO	-0.3 ~ VDDI + 0.3	V	
Operating temperature range (LCD Panel surface)	Topr	-20 ~ +70	°C	(*2-1)
Storage temperature range	Tstg	-30 ~ +80	°C	(*2-1)
LED Forward current	Iled	+30	mA	(*2-2)

Note)

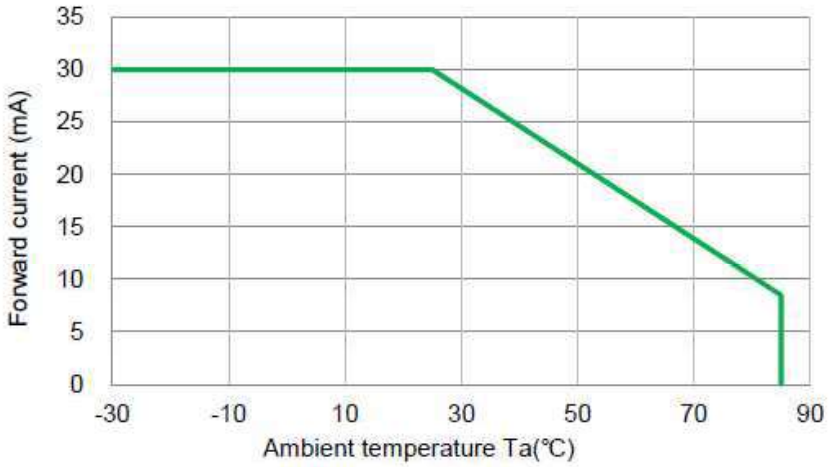
(*2-1) Maximum humidity is defined as follows:

Ta≦40℃ : 85%RH Max.

Ta> 40℃ : Absolute humidity needs to be equal or less than the numeric value at the condition of Ta=40℃, 85%RH.

Don't condense dew

(*2-2) Ambient Temperature vs Allowable Forward Current is due to the following graph.



3. OPERATING CONDITIONS

3.1 POWER SUPPLY VOLTAGE

(GND=0V)

PARAMETER	SYMBOL	Min.	Typ.	Max.	UNIT	REMARK
Power supply voltage for I/O	VDDI	1.7	1.8	1.9	V	
Power Supply for Analog Circuit	VCI	3.0	3.1	3.2	V	

3.2 INPUT SIGNAL VOLTAGE

PARAMETER	SYMBOL	Min.	Typ.	Max.	UNIT	Application Terminal
H level threshold voltage	VIH	0.8xVDDI	-	VDDI	V	All Input terminal
L level threshold voltage	VIL	VSS	-	0.2xVDDI	V	
H level current leakage	ILIH	-	-	10	uA	
L level current leakage	ILIL	-10	-	-	uA	

4. ELECTRICAL CHARACTERISTICS

4.1 POWER CONSUMPTION

* Ta=25ºC, Driving Condition: VDDI=1.8V, VCI=3.1V

Mode	Symbol	Display	Min.	Typ.	Max.	UNIT	Remark
Normal mode	Ivvdi	White raster	-	1.21	1.70	mA	
	Ivci	White raster	-	1.94	3.20	mA	
MIP Mode	Ivvdi	White raster	-	0.27	0.40	mA	
	Ivci	White raster	-	0.12	0.27	mA	
DSTB mode	Ivvdi	-	-	-	0.05	mA	
	Ivci	-	-	-	0.05	mA	

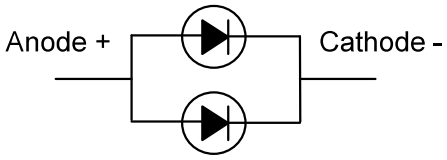
Power consumption: NOT peek, the mean value per second

4.2 BACKLIGHT OPERATING CONDITIONS

Mode	Symbol	Min.	Typ.	Max.	UNIT	Remark
Backlight Forward voltage	Vfbl	2.9	3.05	3.2	V	Iled=19mA (*4-1)

Note)

(*4-1) Back light LED_FPC schematic:

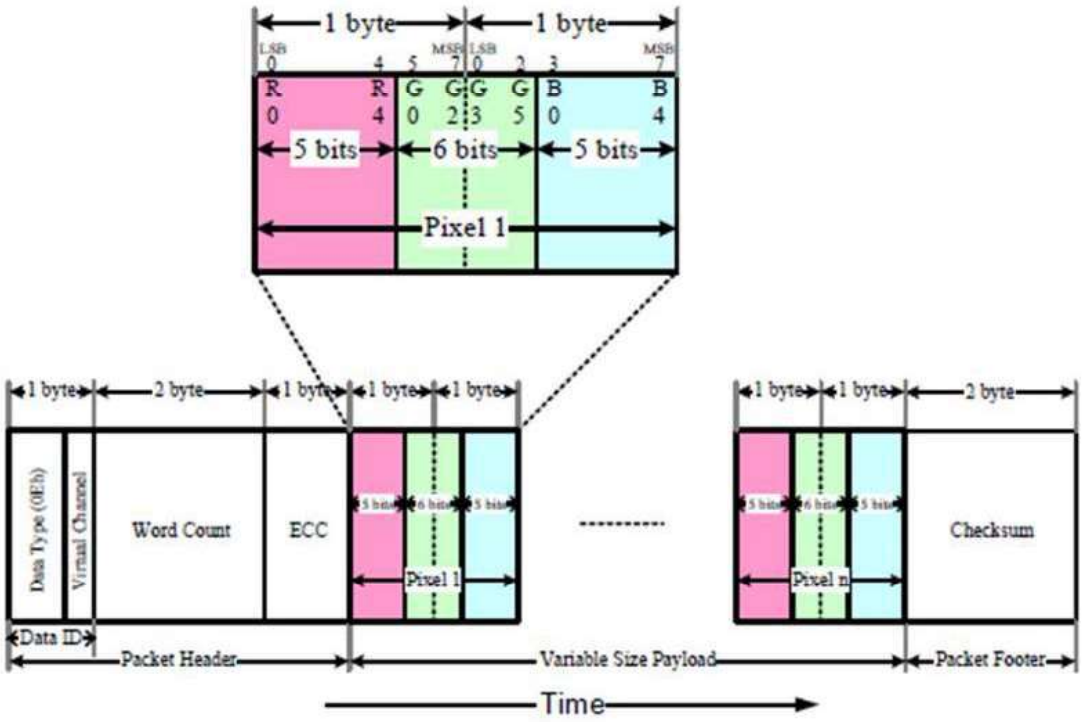


5. INTERFACE

5.1 MIPI INTERFACE

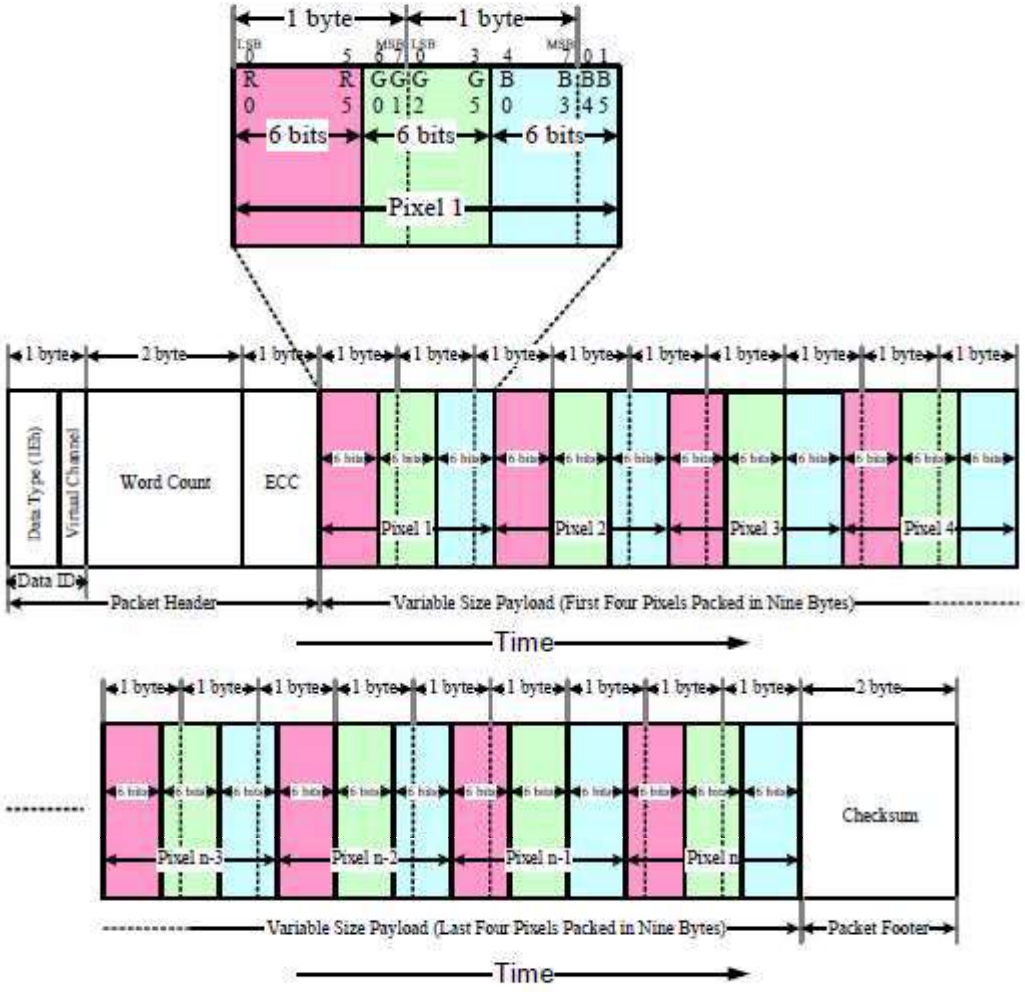
Follow the MIPI Standerd.
D-PHY: V1.0
DSI:1.01.00
DCS:1.01.00
MIPI I/F Supported 1 data lane (MIPI CLK speed up to 300Mbps).
MIPI I/F Supported only command mode.

Packed Pixel Stream, 16-bits Format, Long packet, Data Type 1228 pe 00 1110 (0Eh)



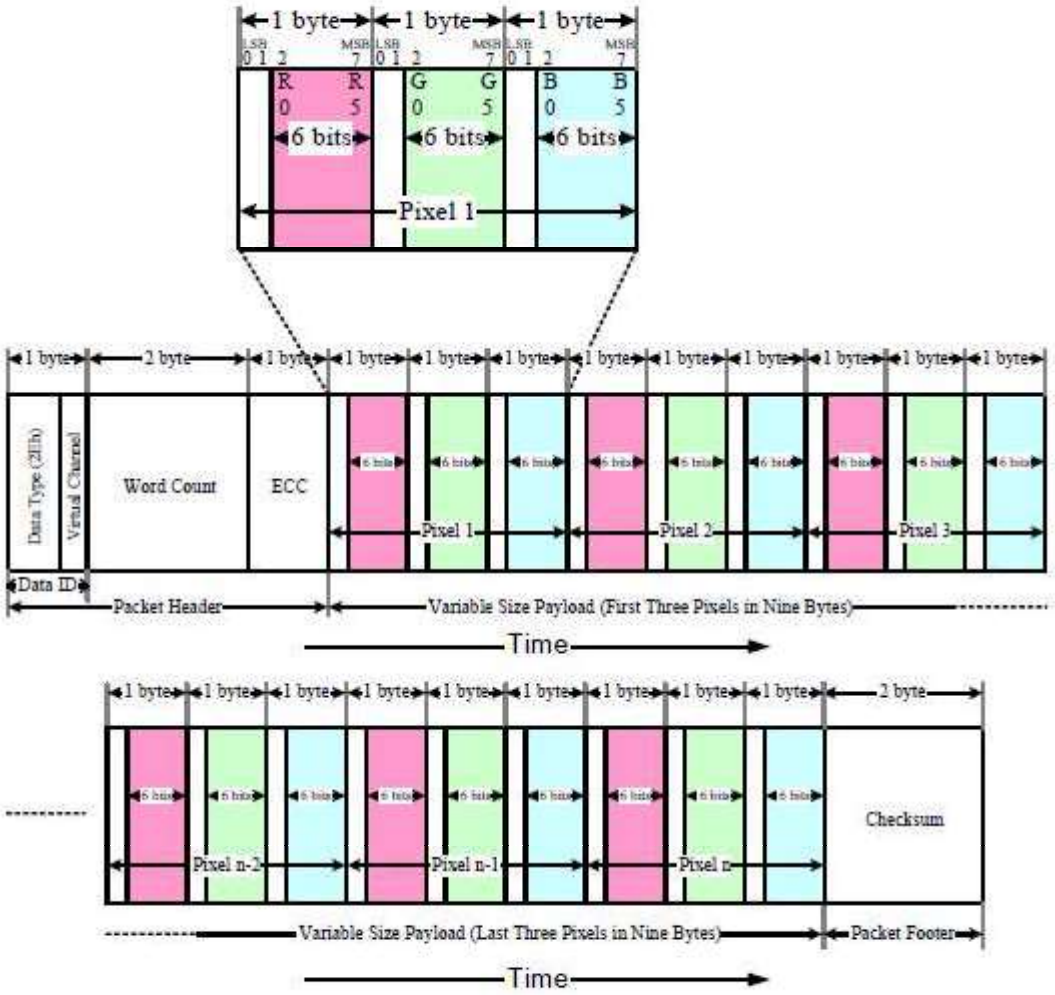
16-bit per Pixel – RGB Color Format, Long packet

Packed Pixel Stream, 18-bits Format, Long packet, Data type = 01 1110 (1Eh)



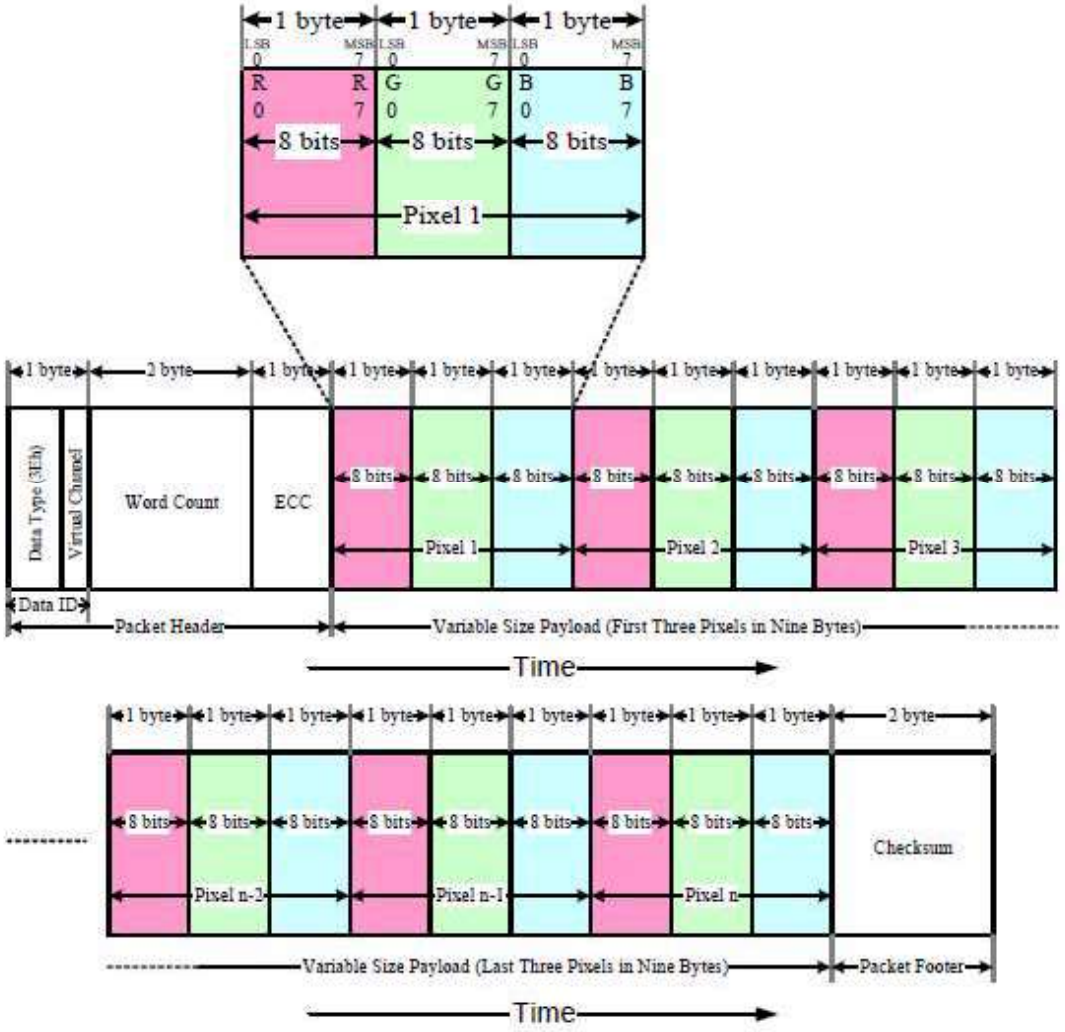
18-bit per Pixel (Packed)– RGB Color Format, Long packet

Pixel Stream, 18-bits Format in Three Bytes, Long packet, Data Type = 101110 (2Eh)



18-bit per Pixel (Loosely Packed)– RGB Color Format, Long packet

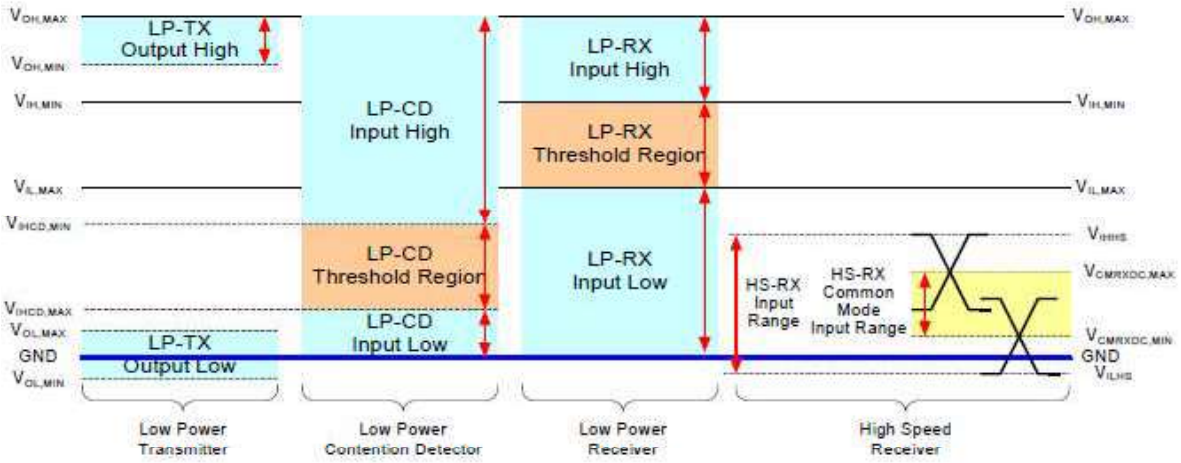
Packed Pixel Stream, 24-bits Format, Long packet, Data Type = 11 1110 (3Eh)



24-bit per Pixel – RGB Color Format, Long packet

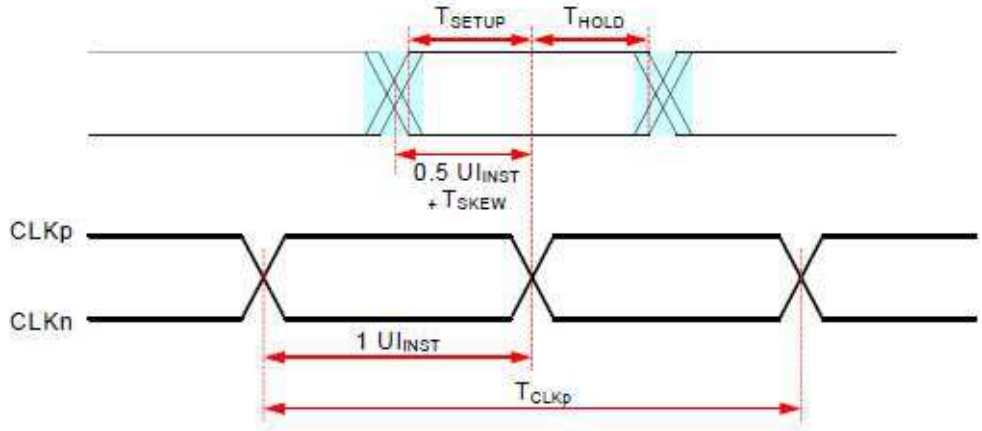
5.2 MIPI DC CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
MIPI Characteristics for High Speed Receiver					
VILHS	Single-ended input low voltage	-40	-	-	mV
VIHHS	Single-ended input high voltage	-	-	460	mV
VCMRXDC	Common-mode voltage	70	-	330	mV
ZID	Differential input impedance	80	100	125	ohm
V_{IDTH}	Different input high threshold	-	-	70	mV
V_{IDTL}	Different input low threshold	-70	-	-	mV
$V_{TERM-EN}$	Single-ended threshold for HS termination enable	-	-	450	mV
MIPI Characteristics for Low Power Mode					
VI	Pad signal voltage range	-50	-	1350	mV
VGNDSH	Ground shift	-50	-	50	mV
VIL	Logic 0 input threshold	0.0	-	550	mV
VIH	Logic 1 input threshold	880	-	VDD	mV
VHYST	Input hysteresis	25	-	-	mV
VOL	Output low level	-50	-	50	mV
VOH	Output high level	1.1	1.2	1.3	V
VIHCD,MAX	Logic 0 contention threshold	0.0	-	200	mV
VILCD,MIN	Logic 1 contention threshold	450	-	VDD	mV



5.3 MIPI AC CHARACTERISTICS

High Speed Data Transmission: Data-Clock Timing



Parameter	Symbol	Min	Typ	Max	Units	Notes
UI instantaneous	UI_{INST}	3.33	-	12.5	ns	
Data to Clock Skew [measured at transmitter]	T_{SKEW}[TX]	-0.15	-	0.15	UI_{INST}	
Data to Clock Setup Time [measured at receiver]	T_{SETUP}[RX]	0.15	-	-	UI_{INST}	
Data to Clock Hold Time [measured at receiver]	T_{HOLD}[RX]	0.15	-	-	UI_{INST}	
20% - 80% rise time and fall time	t_R / t_F	150	-	-	ps	
		-	-	0.3	UI_{INST}	

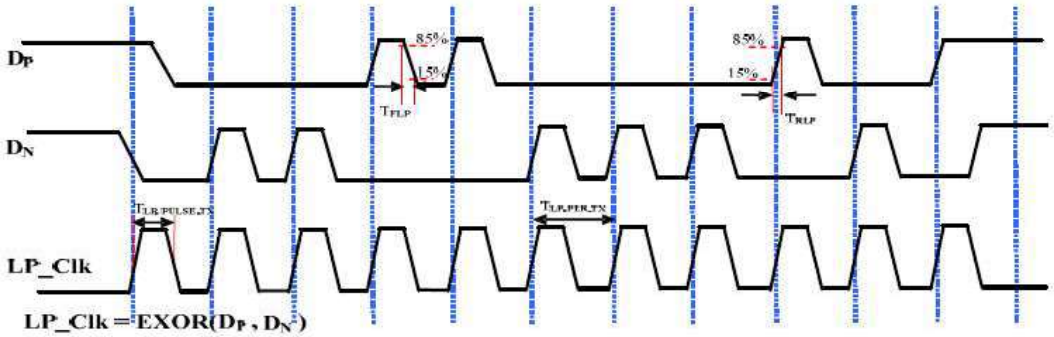
Note:

1. This value corresponds to a minimum 80 MHz data rate.

2. The minimum UI shall not be violated for any single bit period, i.e.,any DDR half cycle within a data burst.

3. For MIPI speed limitations: 300Mbps.

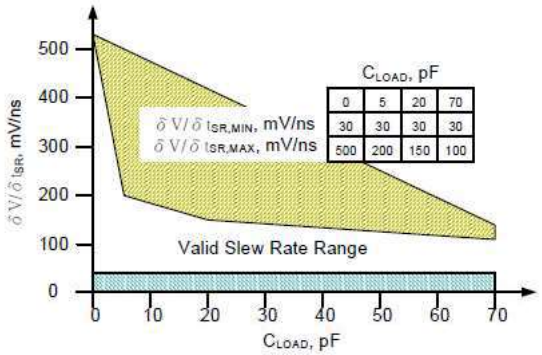
LP Transmission AC Specification



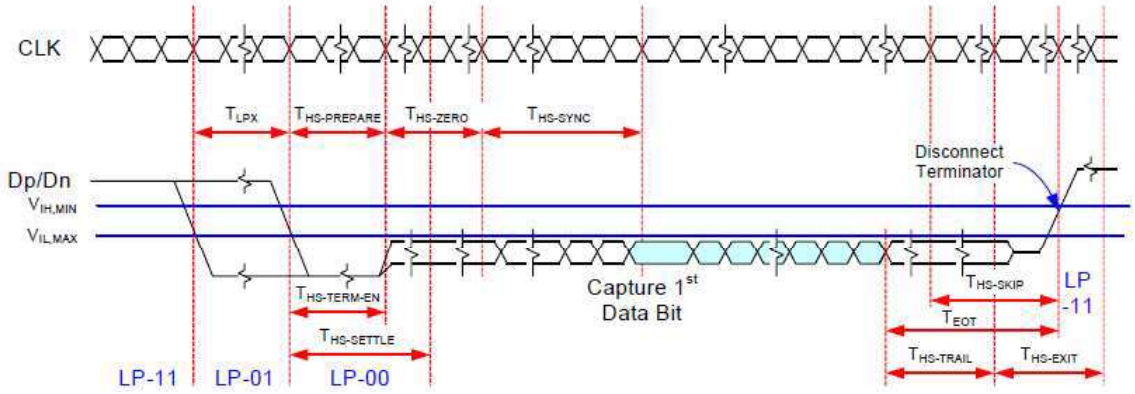
Parameter		Symbol	Min	Typ	Max	Units	Notes
15%-85% rise time and fall time		T_{RLP} / T_{FLP}	-	-	25	ns	1
30%-85% rise time and fall time		T_{REOT}	-	-	35	ns	1,5,6
Pulse width of the LP exclusive-OR clock	First LP exclusive-OR clock pulse after STOP state or last pulse before stop state	$T_{LP-PULSE-TX}$	40	-	-	ns	4
	All other pulses		20	-	-	ns	4
Period of the LP exclusive-OR clock		$T_{LP-PER-TX}$	90	-	-	ns	
Slew Rate@ C_{LOAD} = 0pF		$\delta V/\delta t_{SR}$	30	-	500	mV/ns	1,2,3,7
Slew Rate@ C_{LOAD} = 5pF			30	-	200	mV/ns	1,2,3,7
Slew Rate@ C_{LOAD} = 20pF			30	-	150	mV/ns	1,2,3,7
Slew Rate@ C_{LOAD} = 70pF			30	-	100	mV/ns	1,2,3,7
Load Capacitance		C_{LOAD}	-	-	70	pF	1

Note:

1. *CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.*
2. *When the output voltage is between 15% and below 85% of the fully settled LP signal levels.*
3. *Measured as average across any 50 mV segment of the output signal transition.*
4. *This parameter value can be lower then TLPX due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters. Any LP exclusive-OR pulse observed during HS EoT (transition from HS level to LP-11) is glitch behavior.*
5. *The rise-time of TREOT starts from the HS common-level at the moment the differential amplitude drops below 70mV, due to stopping the differential drive.*
6. *With an additional load capacitance CCM between 0-60pF on the termination center tap at RX side of the Lane.*
7. *This value represents a corner point in a piecewise linear curve as bellowed.*



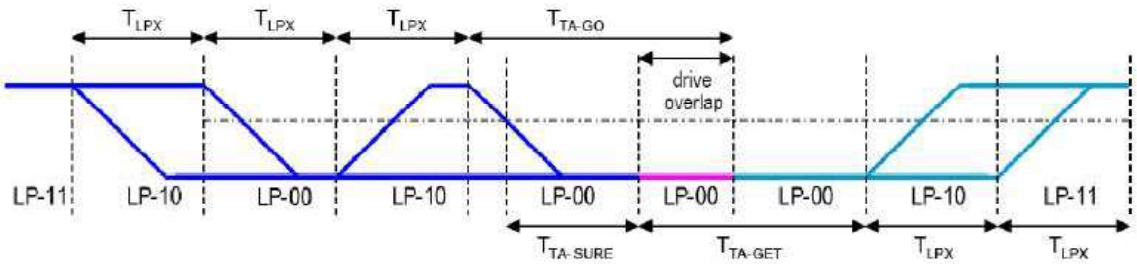
High-Speed Data Transmission in Bursts



Parameter	Symbol	Min	Typ	Max	Units
Time to drive LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI		85+6UI	ns
Time from start of tHS-TRAIL or tCLK-TRAIL period to start of LP-11 state	T_{EOT}			105+12UI	ns
Time to enable Data Lane receiver line termination measured from when Dn cross VIL,MAX	$T_{HS-TERM-EN}$			35+4UI	ns
Time to drive flipped differential state after last payload data bit of a HS transmission burst	$T_{HS-TRAIL}$	60+4UI			ns
Time-out at RX to ignore transition period of EoT	$T_{HS-SKIP}$	40		55+4UI	ns
Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100			ns
Length of any Low-Power state period	T_{LPX}	50			ns
Sync sequence period	$T_{HS-SYNC}$		8UI		ns
Minimum lead HS-0 drive period before the Sync sequence	$T_{HS-ZERO}$	105+6UI			ns

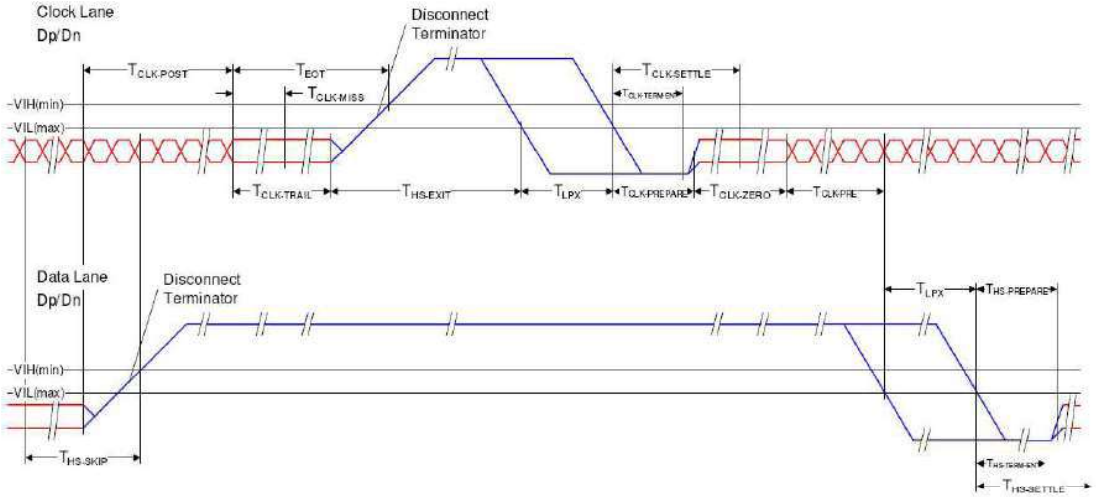
Note:
1: The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.
2: UI means Unit Interval, equal to one halt HS the clock period on the Clock Lane.
3: TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

Turnaround Procedure



Parameter	Symbol	Min	Typ	Max	Units
Length of any Low-Power state period : Master side	T_{LPX}	50		75	ns
Length of any Low-Power state period : Slave side	T_{LPX}	50		75	ns
Ratio of TLPX(MASTER)/TLPX(SLAVE) between Master and Slave side	Ratio T_{LPX}	2/3		3/2	
Time-out before new TX side start driving	$T_{TA-SURE}$	T_{LPX}		$2T_{LPX}$	ns
Time to drive LP-00 by new TX	T_{TA-GET}		$5T_{LPX}$		ns
Time to drive LP-00 after Turnaround Request	T_{TA-GO}		$4T_{LPX}$		ns

Switching the Clock Lane between Clock Transmission and Low-Power Mode

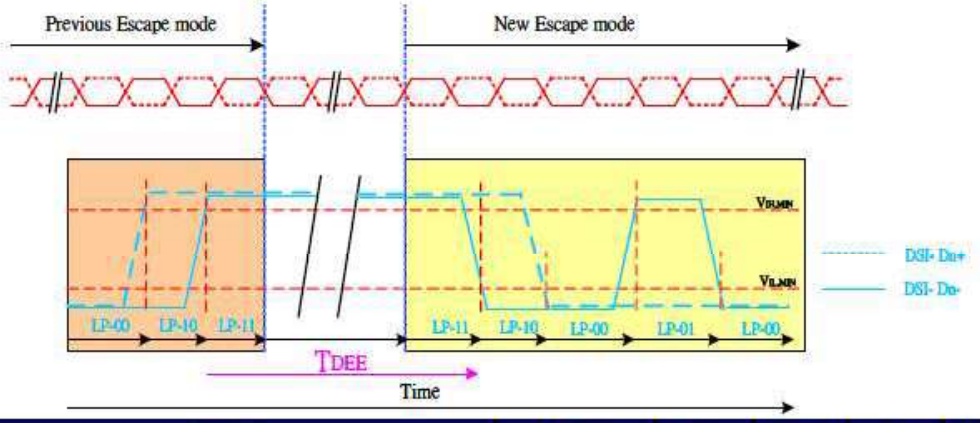


Parameter	Symbol	Min	Typ	Max	Units
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode.	$T_{CLK-POST}$	60+52UI	-	-	ns
Detection time that the clock has stopped toggling	$T_{CLK-MISS}$	-	-	60	ns
Time to drive LP-00 to prepare for HS clock transmission	$T_{CLK-PREPARE}$	38	-	95	ns
Minimum lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE}$ +$T_{CLK-ZERO}$	300	-	-	ns
Time to enable Clock Lane receiver line termination measured from when Dn cross VIL,MAX	$T_{HS-TERM-EN}$	-	-	38	ns
Minimum time that the HS clock must be set prior to any associated date lane beginning the transmission from LP to HS mode	$T_{CLK-PRE}$	8	-	-	UI
Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK-TRAIL}$	60	-	-	ns

LP11 timing request between data transformation

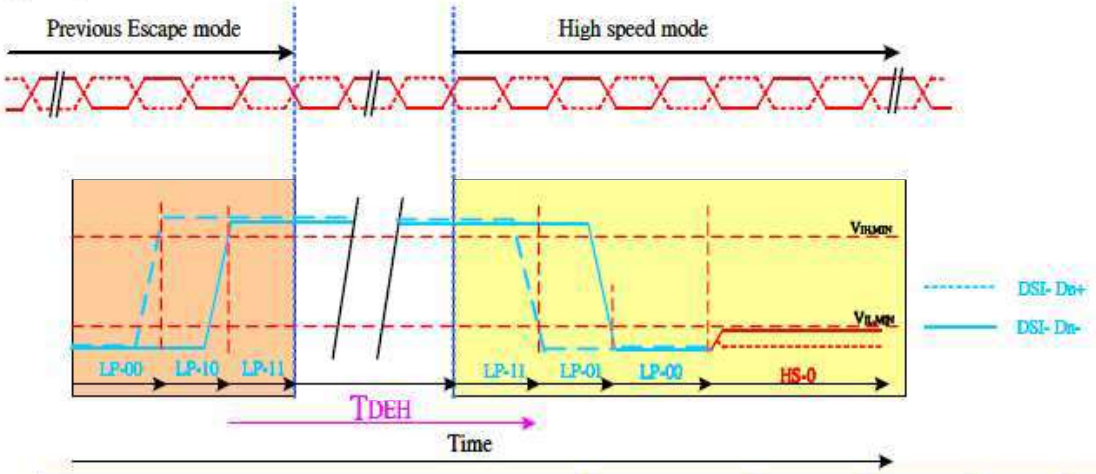
When Clock lane of DSI TX chip always keeps High speed mode, then Clock lane never go back to Low power mode. If Date lane of TX chip needs to transmit the next new data transmission or sequence, after the end of Low power mode or High speed mode or BTA. Then TX chip needs to keep LP-11 stop state before the next new data transmission, no matter in Low power mode or High speed mode or BTA. The LP-11 minimum timing is required for RX chip in the following 9 conditions, include of LP – LP, LP – HS, HS – LP, HS – HS, BTA – BTA, LP – BTA, BTA – LP, HS – BTA, and BTA – HS. This rule is suitable for short or long packet between TX and RX data transmission.

(1) Timing between LP – LP command



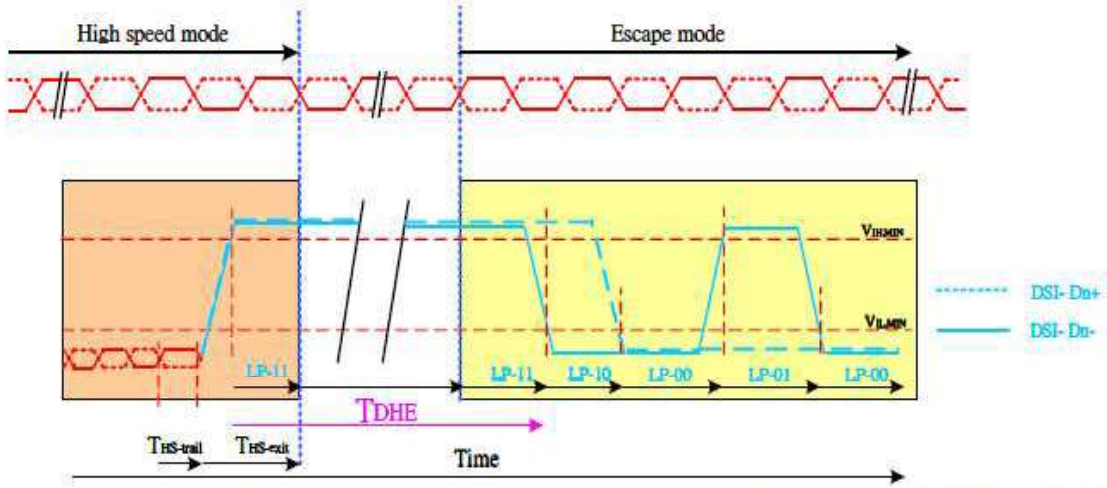
Parameter	Symbol	Min	Typ	Max	Units
LP-11 delay to a start of the new Escape Mode Entry	T_{DEE}	100			ns

(2)Timing between LP – HS command



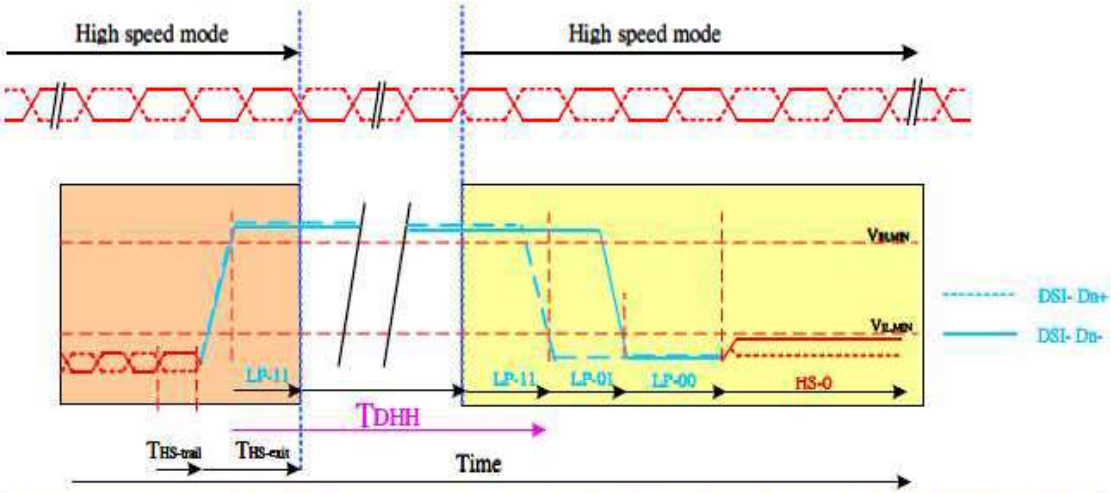
Parameter	Symbol	Min	Typ	Max	Units
LP-11 delay to a start of the Entering High Speed Mode	T_{DEH}	Max(100,32UI)			ns

(3)Timing between HS – LP command



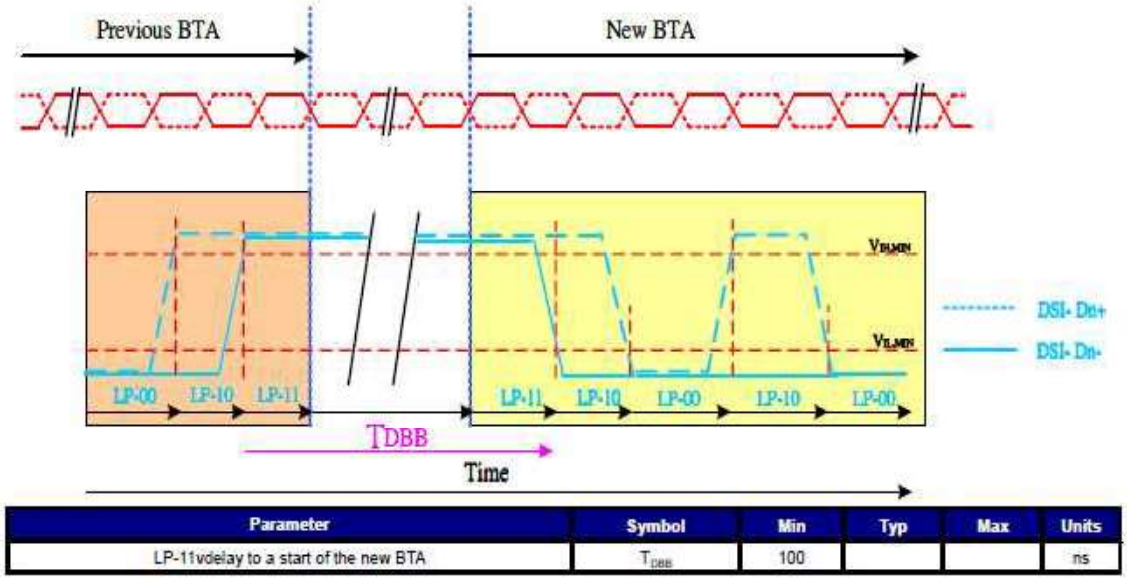
Parameter	Symbol	Min	Typ	Max	Units
LP-11 delay to a start of the Escape Mode Entry	T_{DHE}	Max(100,32UI)			ns

(4)Timing between HS –HS command



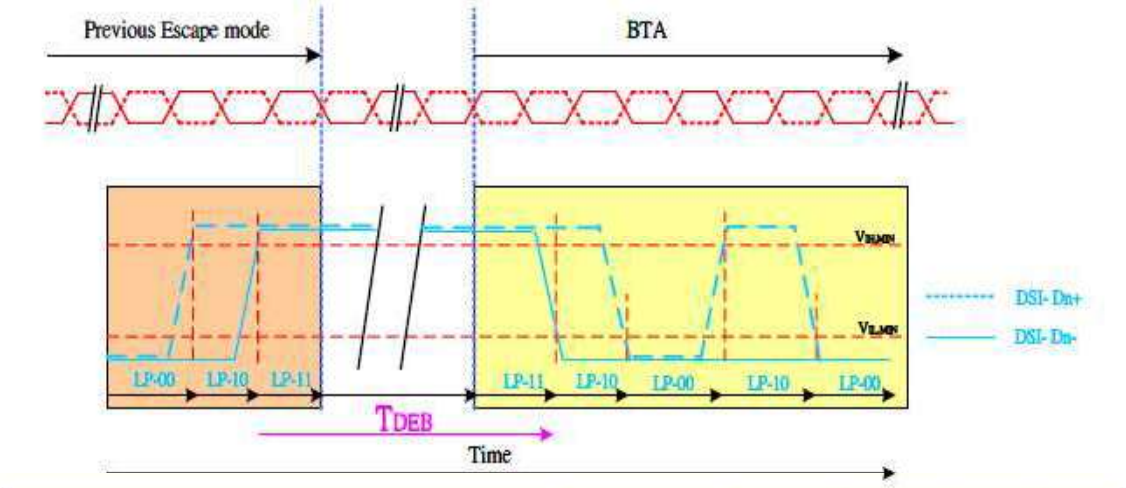
Parameter	Symbol	Min	Typ	Max	Units
LP-11vdelay to a start of the Entering High Speed Mode	T_{DHH}	Max(100,32UI)			ns

(5)Timing between BTA – BTA command



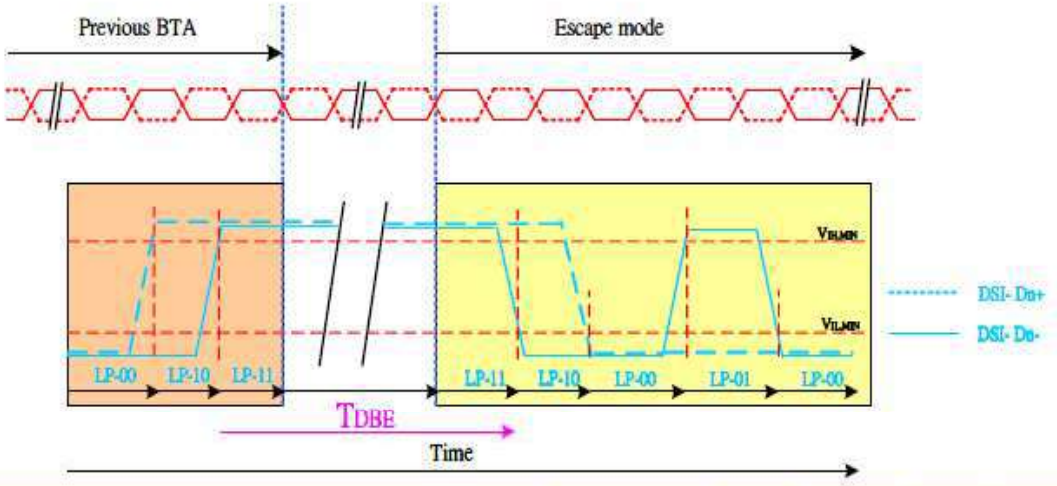
Parameter	Symbol	Min	Typ	Max	Units
LP-11vdelay to a start of the new BTA	T_{DBB}	100			ns

(6)Timing between LP– BTA command



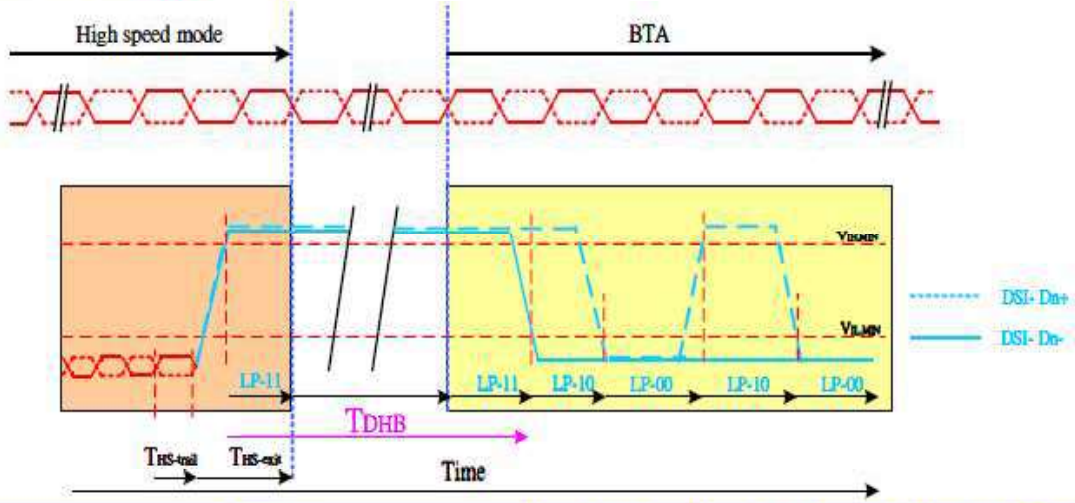
Parameter	Symbol	Min	Typ	Max	Units
LP-11vdelay to a start of the BTA	T_{DEB}	100			ns

(7)Timing between BTA – LP command



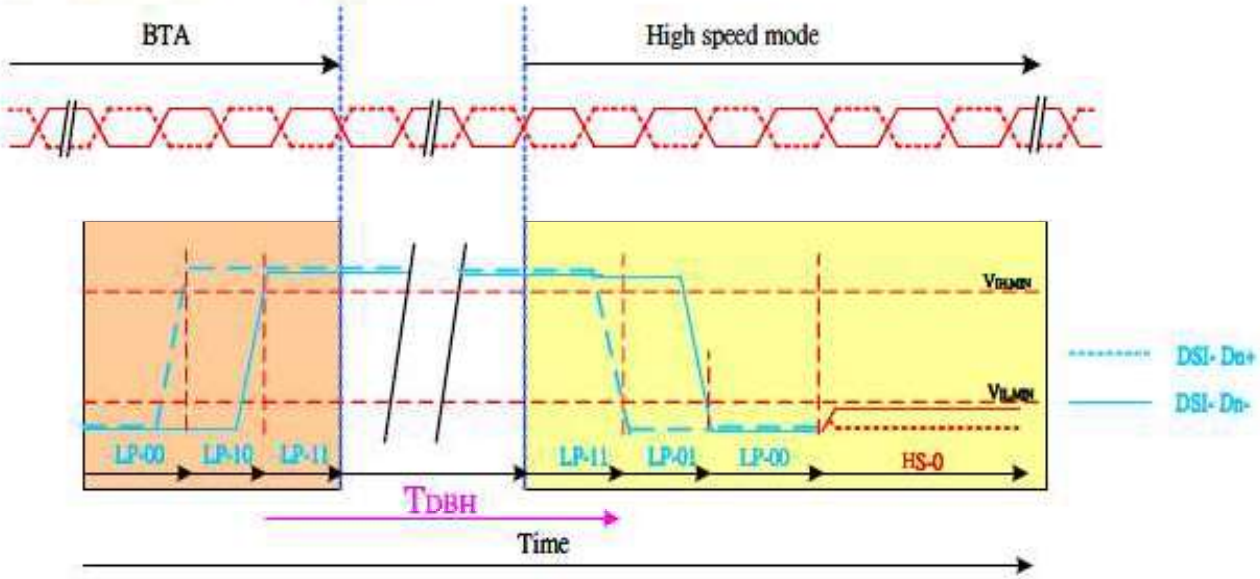
Parameter	Symbol	Min	Typ	Max	Units
LP-11vdelay to a start of the Escape Mode Entry	T_{DBE}	100			ns

(8)Timing between HS – BTA command



Parameter	Symbol	Min	Typ	Max	Units
LP-11vdelay to a start of the BTA	T_{DHB}	Max(100,32UI)			ns

(9)Timing between BTA – HS command

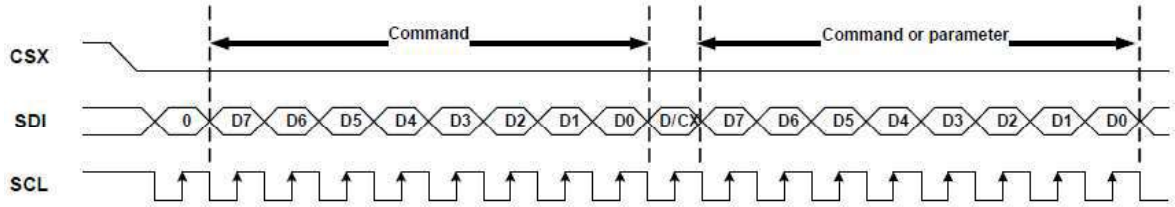


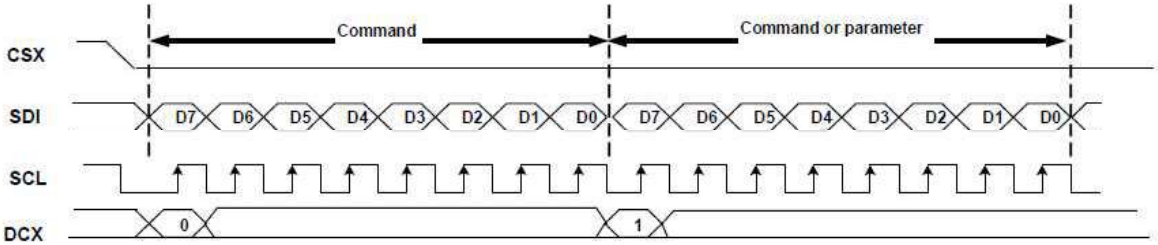
Parameter	Symbol	Min	Typ	Max	Units
LP-11vdelay to a start of the Entering High Speed Mode	T_{DBH}	Max(100;32UI)			ns

5.4 SPI INTERFACE

Command Write for LoSSI

The host CPU drives the CSX pin low and starts by setting the D/CX-bit on SDI or by DCX pin. The bit is read by the display on the first rising
edge of SCL. For 4-Wires Mode, first bit is data bit (D7) is set on SDI by the CPU. Then on the next falling edge of SCL the MSB data bit (D6) is
set on SDI by the CPU and so on. For 3-Wires Mode, the next falling edge of SCL the MSB data bit (D7) is set on SDI by the CPU. On the next
falling edge of SCL the next bit (D6) is set on SDI and so on. This continues until all 8 Data bits have been transmitted as shown in below figures:
Command Write.



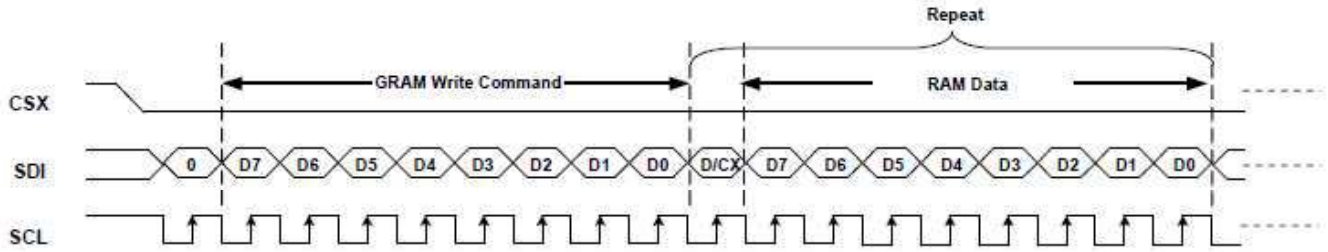


Note: The GRAM write command should be 2Ch/3Ch.

Serial Interface SPI for RAM Data Write/Read

Different display data formats are available for two colors depth supported by the NT35350 listed below.

- 8 colors, RGB 1-1-1-bits pixel data input. (Only support GRAM Write by 0x2C command, not support GRAM Read)
- 65k colors, RGB 5-6-5-bits pixel data input.
- 262k colors, RGB 6- 6-6-bits pixel data input.



TYPE1:

RGB 1-1-1-bits	DCX	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Note
CMDWR	0	0	0	1	0	1	1	0	0	0x2C for GRAM Write
1st RAM Data Write	1	R1[0]	G1[0]	B1[0]	R2[0]	G2[0]	B2[0]	R3[0]	G3[0]	1, 2, 3 Pixel Data write
2nd RAM Data Write	1	B3[5]	R4[0]	G4[0]	B4[0]	R5[0]	G5[0]	B5[0]	R6[0]	3, 4, 5, 6 Pixel Data write
3rd RAM Data Write	1	G6[0]	B6[0]	R7[0]	G7[0]	B7[0]	R8[0]	G8[0]	B8[0]	6, 7, 8 Pixel Data write
So on…										

Note: Transfer data including DCX bit

Table 1. RGB 1-1-1-bits GRAM Write for 3-Wires Mode 9-bit Type SPI

TYPE2:

RGB 1-1-1-bits	DCX	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Note
CMDWR	0	0	0	1	0	1	1	0	0	0x2C for GRAM Write
1st RAM Data Write	1	X	X	R1[0]	G1[0]	B1[0]	R2[0]	G2[0]	B2[0]	1, 2 Pixel Data write
2nd RAM Data Write	1	X	X	R3[0]	G3[0]	B3[5]	R4[0]	G4[0]	B4[0]	3, 4 Pixel Data write
3rd RAM Data Write	1	X	X	R5[0]	G5[0]	B5[0]	R6[0]	G6[0]	B6[0]	5, 6 Pixel Data write
So on…										

Note: Transfer data including DCX bit

Table 2. RGB 1-1-1-bits GRAM Write for 3-Wires Mode 9-bit Type SPI

RGB 5-6-5-bits	DCX	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Note
CMDWR	0	0	0	1	0	1	1	0	0	0x2C for GRAM Write
1st RAM Data Write	1	R1[4]	R1[3]	R1[2]	R1[1]	R1[0]	G1[5]	G1[4]	G1[3]	1st Pixel Data Write (R1, G1, B1)
2nd RAM Data Write	1	G1[2]	G1[1]	G1[0]	B1[4]	B1[3]	B1[2]	B1[1]	B1[0]	
3rd RAM Data Write	1	R2[4]	R2[3]	R2[2]	R2[1]	R2[0]	G2[5]	G2[4]	G2[3]	2nd Pixel Data Write (R2, G2, B2)
4th RAM Data Write	1	G2[2]	G2[1]	G2[0]	B2[4]	B2[3]	B2[2]	B2[1]	B2[0]	
5th RAM Data Write	1	R3[4]	R3[3]	R3[2]	R3[1]	R3[0]	G3[5]	G3[4]	G3[3]	3rd Pixel Data Write (R3, G3, B3)
6th RAM Data Write	1	G3[2]	G3[1]	G3[0]	B3[4]	B3[3]	B3[2]	B3[1]	B3[0]	
So on…										

Note: Transfer data including DCX bit

Table 3. RGB 5-6-5-bits GRAM Write for 3-Wires Mode 9-bit Type SPI

RGB 6-6-6-bits	DCX	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Note
CMDWR	0	0	0	1	0	1	1	0	0	0x2C for GRAM Write
1st RAM Data Write	1	R1[5]	R1[4]	R1[3]	R1[2]	R1[1]	R1[0]	X	X	1st Pixel Data Write (R1, G1, B1)
2nd RAM Data Write	1	G1[5]	G1[4]	G1[3]	G1[2]	G1[1]	G1[0]	X	X	
3rd RAM Data Write	1	B1[5]	B1[4]	B1[3]	B1[2]	B1[1]	B1[0]	X	X	
4th RAM Data Write	1	R2[5]	R2[4]	R2[3]	R2[2]	R2[1]	R2[0]	X	X	2nd Pixel Data Write (R2, G2, B2)
5th RAM Data Write	1	G2[5]	G2[4]	G2[3]	G2[2]	G2[1]	G2[0]	X	X	
6th RAM Data Write	1	B2[5]	B2[4]	B2[3]	B2[2]	B2[1]	B2[0]	X	X	
So on…										

Note: Transfer data including DCX bit

Note: x means don't case

Table 4. RGB 6-6-6-bits GRAM Write for 3-Wires Mode 9-bit Type SPI

Serial Interface Timing Characteristics

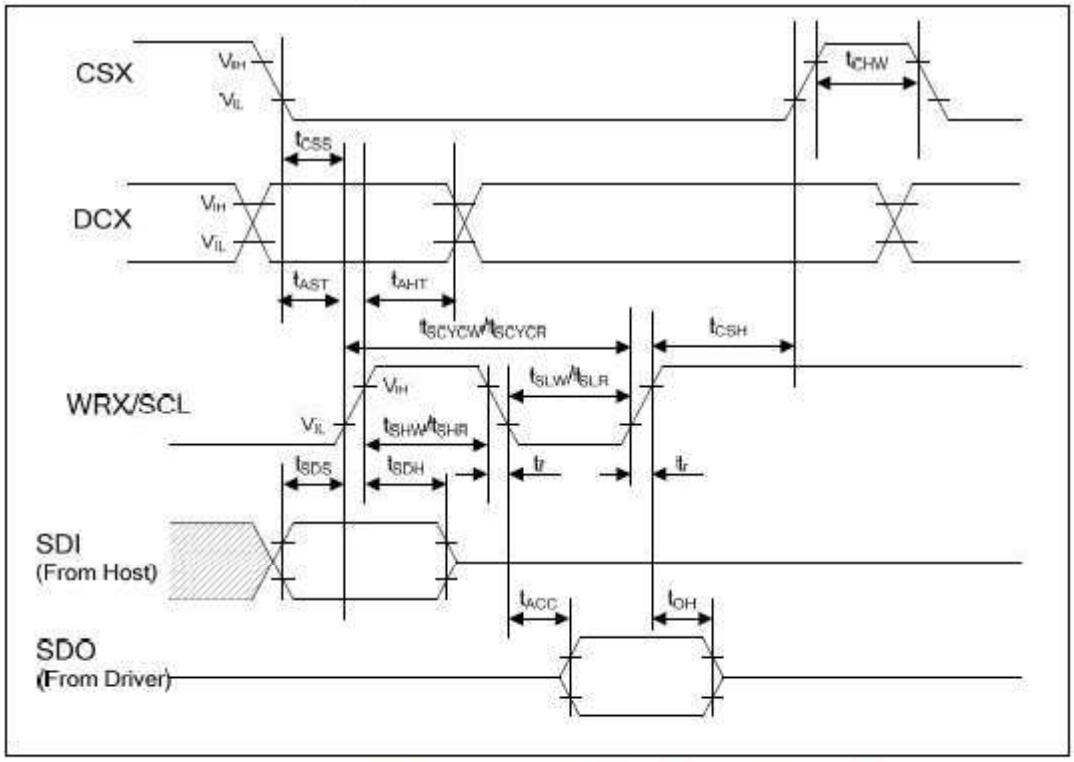


Figure 1. Serial Interface Operation for 3-Wires/4-Wires 9/8-bit Type SPI

VCI = 2.5 V to 3.6V, VDDI = 1.65V to 3.6V (Register Access/ GRAM Read, refer to Figure 39)

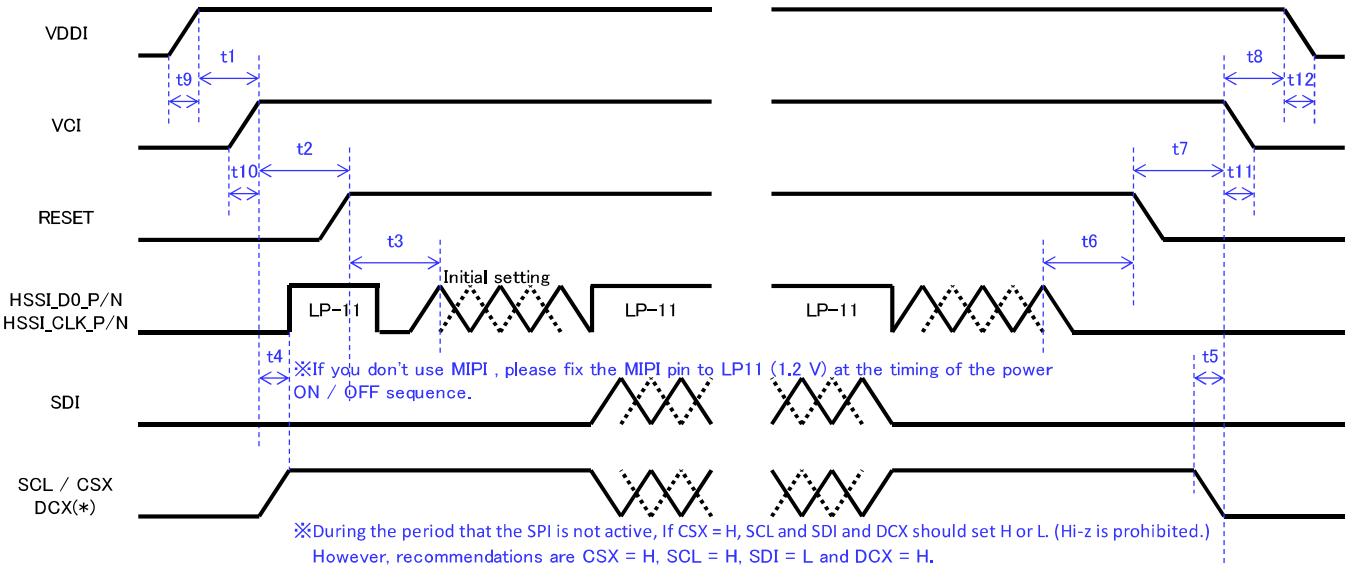
Item	Symbol	Min.	Typ.	Max.	Unit
SCL clock cycle time Write (received)	t_{SCYCW}	80	-	20,000	ns
SCL clock cycle time Read (transmitted)	t_{SCYCR}	280	-	20,000	ns
SCL "High" pulse width Write (received)	t_{SHW}	40	-	-	ns
SCL "High" pulse width Read (transmitted)	t_{SHR}	140	-	-	ns
SCL "Low" pulse width Write (received)	t_{SLW}	40	-	-	ns
SCL "Low" pulse width Read (transmitted)	t_{SLR}	140	-	-	ns
SCL clock rise/fall time	t_r, t_f	-	-	10	ns
Chip select setup time	t_{CSS}	20	-	-	ns
Chip select hold time	t_{CSH}	50	-	-	ns
Input data setup time	t_{SDS}	20	-	-	ns
Input data hold time	t_{SDH}	20	-	-	ns
DCX to SCL Write setup time	tAST	20	-	-	ns
DCX to SCL Write hold time	tAHT	2	-	-	ns
Output data access time	t_{ACC}	-	-	120	ns
Output data hold time	t_{OH}	5	-	-	ns
Chip deselect "High" pulse width	t_{CHW}	40	-	-	ns

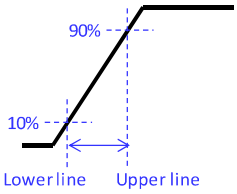
VCI = 2.5 V to 3.6V, VDDI = 1.65V to 3.6V (GRAM Write, refer to Figure 39)

Item	Symbol	Min.	Typ.	Max.	Unit
SCL clock cycle time Write (received)	t_{SCYCW}	16	-	20,000	ns
SCL clock cycle time Read (transmitted)	t_{SCYCR}	280	-	20,000	ns
SCL "High" pulse width Write (received)	t_{SHW}	8	-	-	ns
SCL "High" pulse width Read (transmitted)	t_{SHR}	140	-	-	ns
SCL "Low" pulse width Write (received)	t_{SLW}	8	-	-	ns
SCL "Low" pulse width Read (transmitted)	t_{SLR}	140	-	-	ns
SCL clock rise/fall time	t_r, t_f	-	-	10	ns
Chip select setup time	t_{CSS}	4	-	-	ns
Chip select hold time	t_{CSH}	12	-	-	ns
Input data setup time	t_{SDS}	5	-	-	ns
Input data hold time	t_{SDH}	5	-	-	ns
DCX to SCL Write setup time	tAST	20	-	-	ns
DCX to SCL Write hold time	tAHT	2	-	-	ns
Output data access time	t_{ACC}	-	-	120	ns
Output data hold time	t_{OH}	5	-	-	ns
Chip deselect "High" pulse width	t_{CHW}	8	-	-	ns

6. POWER SEQUENCE

6.1 POWER ON/OFF SEQUENCE





	Min	Typ	Max	unit
t1	0	–	–	ms
t2	10	–	–	ms
t3	10	50	–	ms
t4	0	5	–	ms
t9	–	–	2*	ms
t10	1	–	10	ms

	Min	Typ	Max	unit
t5	0	–	–	ms
t6	10	80	–	ms
t7	0	–	–	ms
t8	0	–	–	ms
t11	1	–	10	ms
t12	–	–	10	ms

Command (HEX)	Address (HEX)
Wait more than 10ms	
FF	E0
28	40
28	0
Wait more than 10ms	
FF	10

*If t9 over than 2ms, please add right command in front of "Initinal setting"

6.2 RESET TIMING CHARACTERISTICS

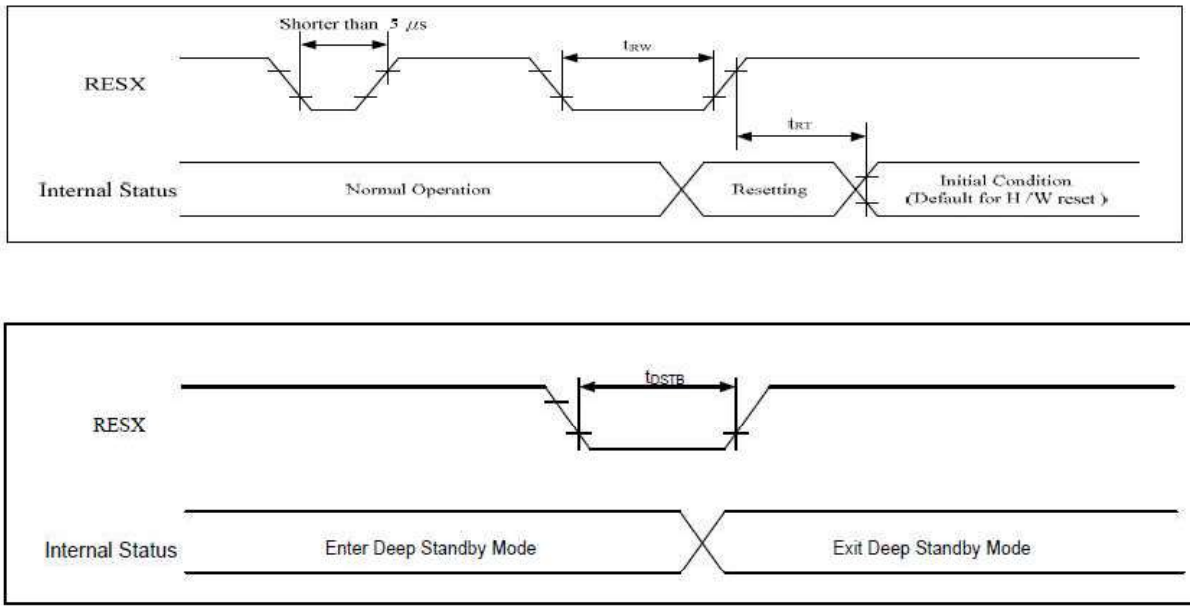


Figure 2. Reset Operation

Table 7.3.4 Reset Timing Characteristics VCI=2.5~4.8V, VDDI=1.65~3.6V, VDDAM=1.65~3.6V

Signal	Symbol	Parameter	Min.	Max.	Unit
RESX	t_{RW}	Reset pulse duration	10		us
	t_{RT}	Reset cancel	-	10 (Note 5)	ms
			-	120 (Note 6)	ms
	tDSTB	Reset pulse duration	3	-	ms

Note :

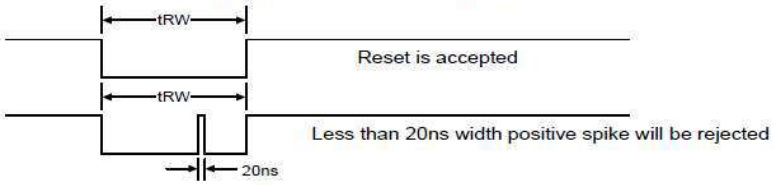
-1. The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 10ms after a rising edge of RESX.

-2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below :

RESX	Pulse Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset Starts

-3. During the Resetting period, the display will be blanked(The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts at Sleep-Out status. The display remains the blank state in Sleep-In mode). Then return to Default condition for Hardware Reset.

-4. Spike Rejection also applies during a valid reset pulse as shown below :

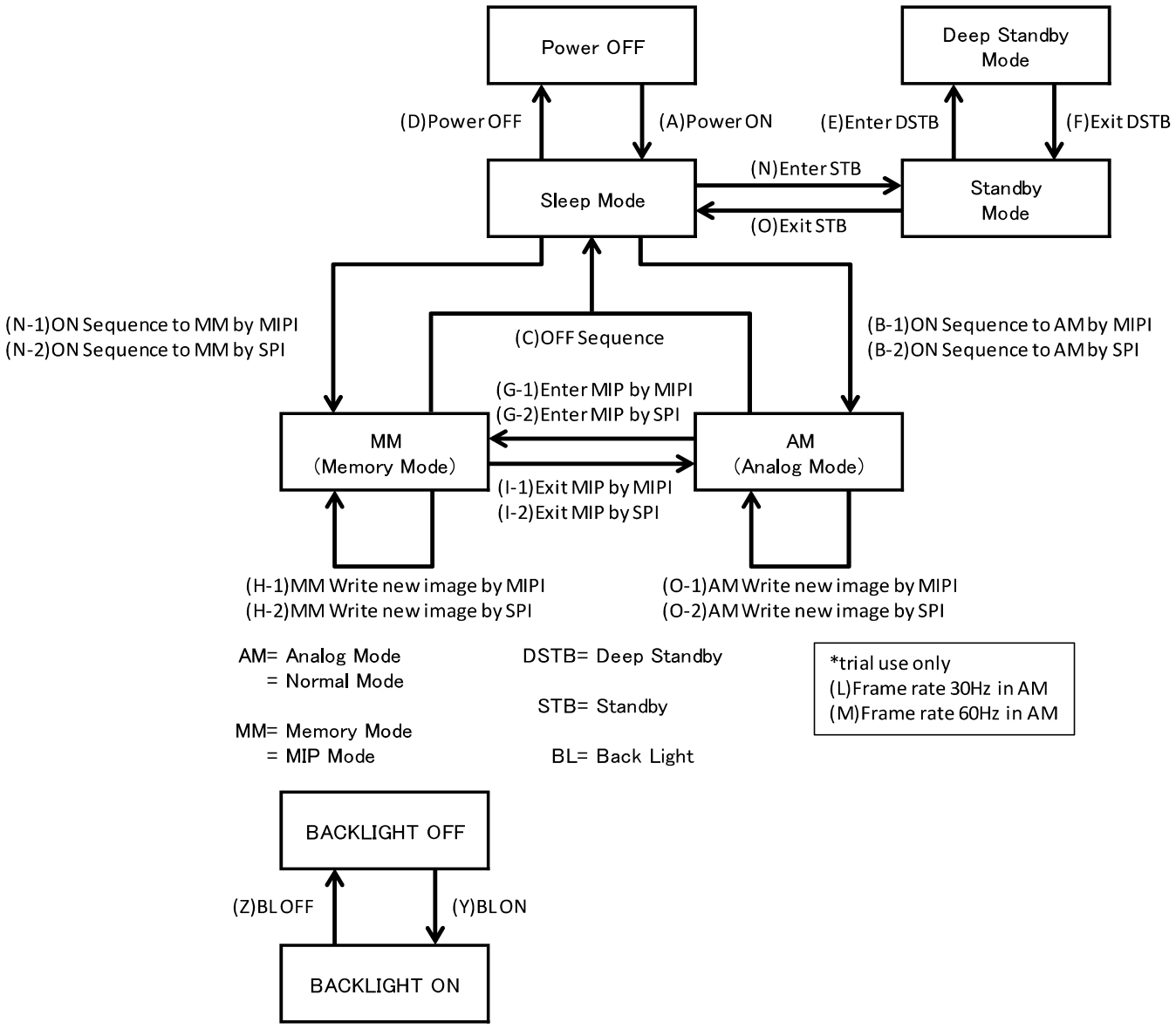


-5. When Reset applied during Sleep-In Mode.

-6. When Reset applied during Sleep-Out Mode.

7. CHANGE STATUS

7.1 STATUS FLOW



7.2 SEAQUENCE

(A)Power ON

Write/ Read	DCS/ Generic	Data Type (HEX)	Para. Num. (DEC)	Command address (HEX)	Parameter value (HEX)	Description
Pwer OFF						
Power supply on VDDI						DSI input should be at GND level while VDDI/VCI off.
Wait more than 0ms						
Power supply on VCI						DSI input should be at GND level while VDDI/VCI off.
Wait more than 5ms						
Set MIPI-DSI to LP-11, SPI to halt state						Refer to "Power ON_OFF sequence"
Wait more than 10ms						
Hard Reset L=>H						
Wait more than 50ms						
Sleep Mode						

(B-1)ON Sequence to AM by MIPI

Write/ Read	DCS/ Generic	Data Type (HEX)	Para. Num. (DEC)	Command address (HEX)	Parameter value (HEX)	Description
Sleep Mode						
Write	DCS	05	-	01	-	Soft reset
Wait more than 10ms						
Write	DCS	15	1	B3	02	
Write	DCS	15	1	BB	10	
Write	xx	xx	xx	xx	xx	Optional setting (Refer to "Register list")
Write	DCS	15	1	3A	06	Set the color format (18bit:06h 16bit:05h)
Write	DCS	05	-	11	-	Sleep out
Wait more than 10ms						
Write	DCS	39	-	2C/3C	-	Transfer image data ※note1
Wait more than 120ms						
Write	DCS	05	-	29	-	Display On ※note2
Analog Mode						

(B-2)ON Sequence to AM by SPI

Write/ Read	DCS/ Generic	Data Type (HEX)	Para. Num. (DEC)	Command address (HEX)	Parameter value (HEX)	Description
Sleep Mode						
Write	-	-	-	01	-	Soft reset
Wait more than 10ms						
Write	-	-	-	B3	02	
Write	-	-	-	BB	10	
Write	-	-	-	F3	02	SPI GRAM access enable
Write	xx	xx	xx	xx	xx	Optional setting (Refer to "Register list")
Write	-	-	-	3A	06	Set the color format (18bit:06h 16bit:05h)
Write	-	-	-	11	-	Sleep out
Wait more than 10ms						
Write	DCS	39	-	2C/3C	-	Transfer image data ※note1
Wait more than 120ms						
Write	DCS	05	-	29	-	Display On ※note2
Analog Mode						

(N-1)ON Sequence to MM by MIPI

Write/ Read	DCS/ Generic	Data Type (HEX)	Para. Num. (DEC)	Command address (HEX)	Parameter value (HEX)	Description
Sleep Mode						
Write	DCS	05	-	01	-	Soft reset
Wait more than 10ms						
Write	DCS	15	1	B3	15	
Write	DCS	15	1	BB	10	
Write	xx	xx	xx	xx	xx	Optional setting (Refer to "Register list")
Write	DCS	15	1	3A	06	Set the color format (18bit:06h 16bit:05h)
Write	DCS	05	-	11	-	Sleep out
Wait more than 10ms						
Write	DCS	05	-	29	-	Display On ※note2
Write	DCS	39	-	2C/3C	-	Transfer image data ※note1
Wait more than 120ms						
Write	DCS	15	1	BB	00	
Write	DCS	15	1	B3	35	
Write	GenericSP	23	1	FF	20	
Write	GenericSP	23	1	0B	00	
Write	GenericSP	23	1	6D	74	
Memory Mode						

(N-2)ON Sequence to MM by SPI

Write/ Read	DCS/ Generic	Data Type (HEX)	Para. Num. (DEC)	Command address (HEX)	Parameter value (HEX)	Description
Sleep Mode						
Write	-	-	-	01	-	Soft reset
Wait more than 10ms						
Write	-	-	-	B3	15	
Write	-	-	-	BB	10	
Write	-	-	-	F3	02	SPI GRAM access enable
Write	-	-	-	xx	xx	Optional setting (Refer to "Register list")
Write	-	-	-	3A	06	Set the color format (18bit:06h 16bit:05h 3bit_Type1:01h 3bit_Type2:08h , Refer to "JD35350 Draft Spec")
Write	-	-	-	11	-	Sleep out
Wait more than 100ms						
Write	-	-	-	29	-	Display On ※note2
Write	-	-	-	2C/3C	-	Transfer image data ※note1
Wait more than 10ms						
Write	-	-	-	BB	00	
Write	-	-	-	B3	35	
Write	-	-	-	FF	20	
Write	-	-	-	0B	00	
Write	-	-	-	6D	74	
Memory Mode						

(C)OFF Sequence

Write/ Read	DCS/ Generic	Data Type (HEX)	Para. Num. (DEC)	Command address (HEX)	Parameter value (HEX)	Description
Analog Mode						
Write	-	-	-	FF	10	Select CMD1 (If already setted CMD1, skip this command)
Write	DCS	05	-	28	-	Display Off
Wait more than 20ms						
Write	DCS	05	-	10	-	Sleep In
Wait more than 100ms						
Sleep Mode						

(D)Power OFF

Write/ Read	DCS/ Generic	Data Type (HEX)	Para. Num. (DEC)	Command address (HEX)	Parameter value (HEX)	Description
Sleep Mode						
Hard Reset H=>L						
Power supply off VCI						
Power supply off VDDI						DSI input should be at GND level while VDDI off.
Pwer OFF						

(E)Enter DSTB

Write/ Read	DCS/ Generic	Data Type (HEX)	Para. Num. (DEC)	Command address (HEX)	Parameter value (HEX)	Description
Sleep Mode						
Write	DCS	15	1	4F	01	Enter DSTB
Set MIPI-DSI to ULPM, SPI to halt state						
Deep Standby Mode						

(F)Exit DSTB

Write/ Read	DCS/ Generic	Data Type (HEX)	Para. Num. (DEC)	Command address (HEX)	Parameter value (HEX)	Description
Deep Standby Mode						
Wait more than 10ms						
Hard Reset H=>L						
Wait more than 3ms						
Hard Reset L=>H						
Wait more than 50ms						
Set MIPI-DSI to LP-11, SPI to halt state						
Sleep Mode						

(L)Frame rate 30Hz

Write/ Read	DCS/ Generic	Data Type (HEX)	Para. Num. (DEC)	Command address (HEX)	Parameter value (HEX)	Description
Analog Mode						
Write	GenericSP	23	1	FF	24	
Write	GenericSP	23	1	D8	C1	
Write	GenericSP	23	1	D9	3E	
Analog Mode						

(M)Frame rate 60Hz

Write/ Read	DCS/ Generic	Data Type (HEX)	Para. Num. (DEC)	Command address (HEX)	Parameter value (HEX)	Description
Analog Mode						
Write	GenericSP	23	1	FF	24	
Write	GenericSP	23	1	D8	41	
Write	GenericSP	23	1	D9	1E	
Analog Mode						

(N)Enter STB

Write/ Read	DCS/ Generic	Data Type (HEX)	Para. Num. (DEC)	Command address (HEX)	Parameter value (HEX)	Description
Sleep Mode						
Power supply off VCI						
Standby Mode						

(O)Exit STB

Write/ Read	DCS/ Generic	Data Type (HEX)	Para. Num. (DEC)	Command address (HEX)	Parameter value (HEX)	Description
Standby Mode						
Power supply on VCI						
Sleep Mode						

(Y)BL ON

Write/ Read	DCS/ Generic	Data Type (HEX)	Para. Num. (DEC)	Command address (HEX)	Parameter value (HEX)	Description
Analog Mode						
Write	DCS	15	1	FF	10	Select CMD1 (If already setted CMD1, skip this command)
Write	DCS	15	1	53	24	BACKLIGHT ON
Write	DCS	15	1	51	xx	LEDPWMduty setting(00h:0% ~ FFh:100%)

(Z)BL OFF

Write/ Read	DCS/ Generic	Data Type (HEX)	Para. Num. (DEC)	Command address (HEX)	Parameter value (HEX)	Description
Analog Mode						
Write	DCS	15	1	FF	10	Select CMD1 (If already setted CMD1, skip this command)
Write	DCS	15	1	53	00	BACKLIGHT OFF

(G-1)Enter MIP by MIPI

Write/ Read	DCS/ Generic	Data Type (HEX)	Para. Num. (DEC)	Command address (HEX)	Parameter value (HEX)	Description
Analog Mode						
Write	DCS	15	1	FF	10	Select CMD1 (If already setted CMD1, skip this command)
Write	DCS	15	1	B3	17	
Write	DCS	15	1	BB	10	
Write	DCS	15	1	F3	00	MIPI GRAM access enable
Write	DCS	15	1	3A	06	Set the color format (18bit:06h 16bit:05h)
Write	DCS	39	1	2A	00	Set X-direction display address
			2		00	
			3		01	
			4		3F	
Write	DCS	39	1	2B	00	Set Y-direction display address
			2		00	
			3		01	
			4		2B	
Write	DCS	39	-	2C/3C	-	Transfer image data ※note1
Write	DCS	15	1	BB	00	
Write	DCS	15	1	B3	35	
Write	GenericSP	23	1	FF	20	
Write	GenericSP	23	1	0B	00	
Write	GenericSP	23	1	6D	74	
Memory Mode						

It can set the range of partial update area.

(G-2)Enter MIP by SPI

Write/ Read	DCS/ Generic	Data Type (HEX)	Para. Num. (DEC)	Command address (HEX)	Parameter value (HEX)	Description
Analog Mode						
Write	-	-	-	FF	10	Select CMD1 (If already setted CMD1, skip this command)
Write	-	-	-	B3	17	
Write	-	-	-	F3	02	SPI GRAM access enable
Write	-	-	-	BB	10	
Write	-	-	-	3A	09	Set the color format (18bit:06h 16bit:05h 3bit Type1:01h 3bit Type2:08h , Refer to "JD35350 Draft Spec")
Write	-	-	-	2A	00	Set X-direction display address
					00	
					01	
					3F	
Write	-	-	-	2B	00	Set Y-direction display address
					00	
					01	
					2B	
Write	-	-	-	2C/3C	-	Transfer image data ※note1
Write	-	-	-	BB	00	RM=0, DM[1:0]=0
Write	-	-	-	B3	35	
Write	-	-	-	FF	20	
Write	-	-	-	0B	00	
Write	-	-	-	6D	74	
Memory Mode						

It can set the range of partial update area.

(O-1)AM Write new image by MIPI

Write/ Read	DCS/ Generic	Data Type (HEX)	Para. Num. (DEC)	Command address (HEX)	Parameter value (HEX)	Description
Analog Mode						
Write	DCS	15	1	FF	10	Select CMD1 (If already setted CMD1, skip this command)
Write	DCS	15	1	3A	06	Set the color format (18bit:06h 16bit:05h)
Write	DCS	39	1	2A	00	Set X-direction display address
			2		00	
			3		01	
			4		3F	
Write	DCS	39	1	2B	00	Set Y-direction display address
			2		00	
			3		01	
			4		2B	
Write	DCS	39	-	2C/3C	-	Transfer image data ※note1
Analog Mode						

It can set the range of partial update area.

(O-2)AM Write new image by SPI

Write/ Read	DCS/ Generic	Data Type (HEX)	Para. Num. (DEC)	Command address (HEX)	Parameter value (HEX)	Description
Analog Mode						
Write	-	-	-	FF	10	Select CMD1 (If already setted CMD1, skip this command)
Write	-	-	-	BB	10	
Write	-	-	-	F3	02	SPI GRAM access enable
Write	-	-	-	3A	06	Set the color format (18bit:06h 16bit:05h)
Write	-	-	-	2A	00	Set X-direction display address
					00	
					01	
					3F	
Write	-	-	-	2B	00	Set Y-direction display address
					00	
					01	
					2B	
Write	-	-	-	2C/3C	-	Transfer image data ※note1
Write	-	-	-	BB	00	
Analog Mode						

It can set the range of partial update area.

note1 : If the communication is interrupted during transmission of the 2Ch/3Ch command, please re-send 2Ch/3Ch command from the beginning of the frame.

【example】

・18bit/16bit mode

2Ch(ADD), xxh(data),…,xxh(data) ⇒ Data is transmitted for 320 pixels. (1st line)

3Ch(ADD), xxh(data),…,xxh(data) ⇒ Data is transmitted for 320 pixels. (2nd line)

(repeat 3Ch command)

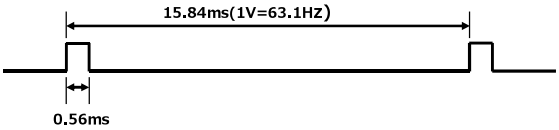
3Ch(ADD), xxh(data),…,xxh(data) ⇒ Data is transmitted for 320 pixels. (320th line)

・RGB1-1-1 mode (RGB 1-1-1-bits is only supported on 3-Wire mode 9-bit SPI interface,)

2Ch(ADD), xxh(data),…,xxh(data) ⇒ Data is transmitted for 320 x 320 pixels. (1frame data)

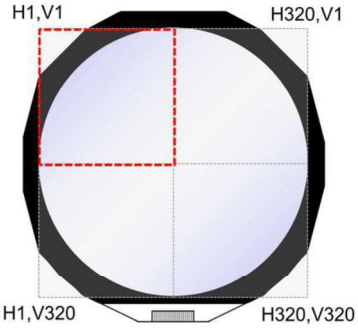
note2 : After Display on, TE signal is output. Timing is as belows.

TE : Frequency 15.84ms(1V=63.1Hz)、H width 0.56ms



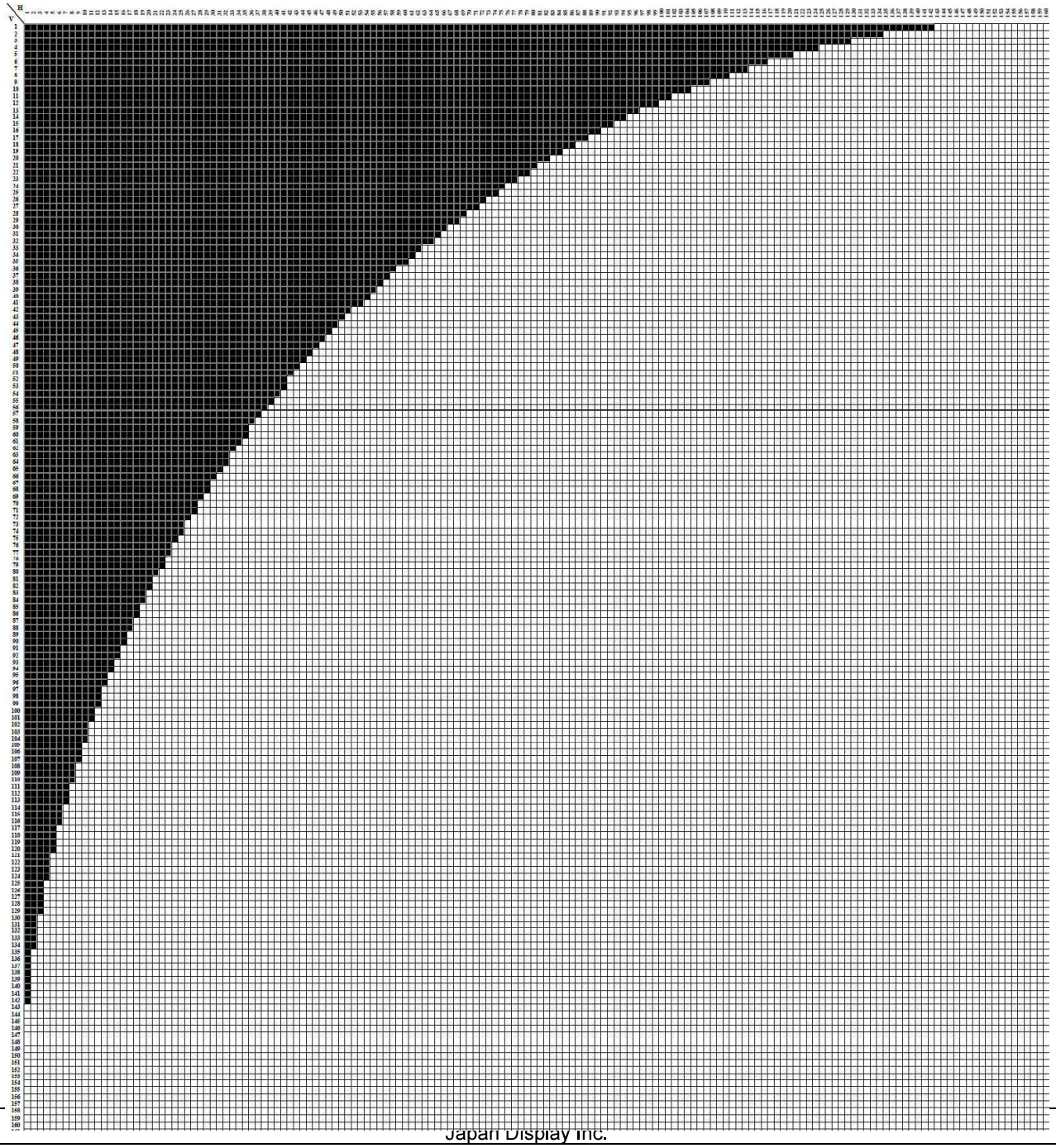
8. DISPLAY ADDRESS MAP

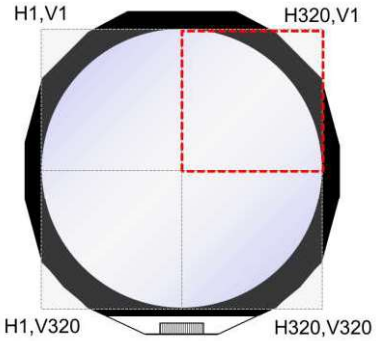
8.1 DISPLAY ADDRESS MAP AND PIXEL LAYOUT

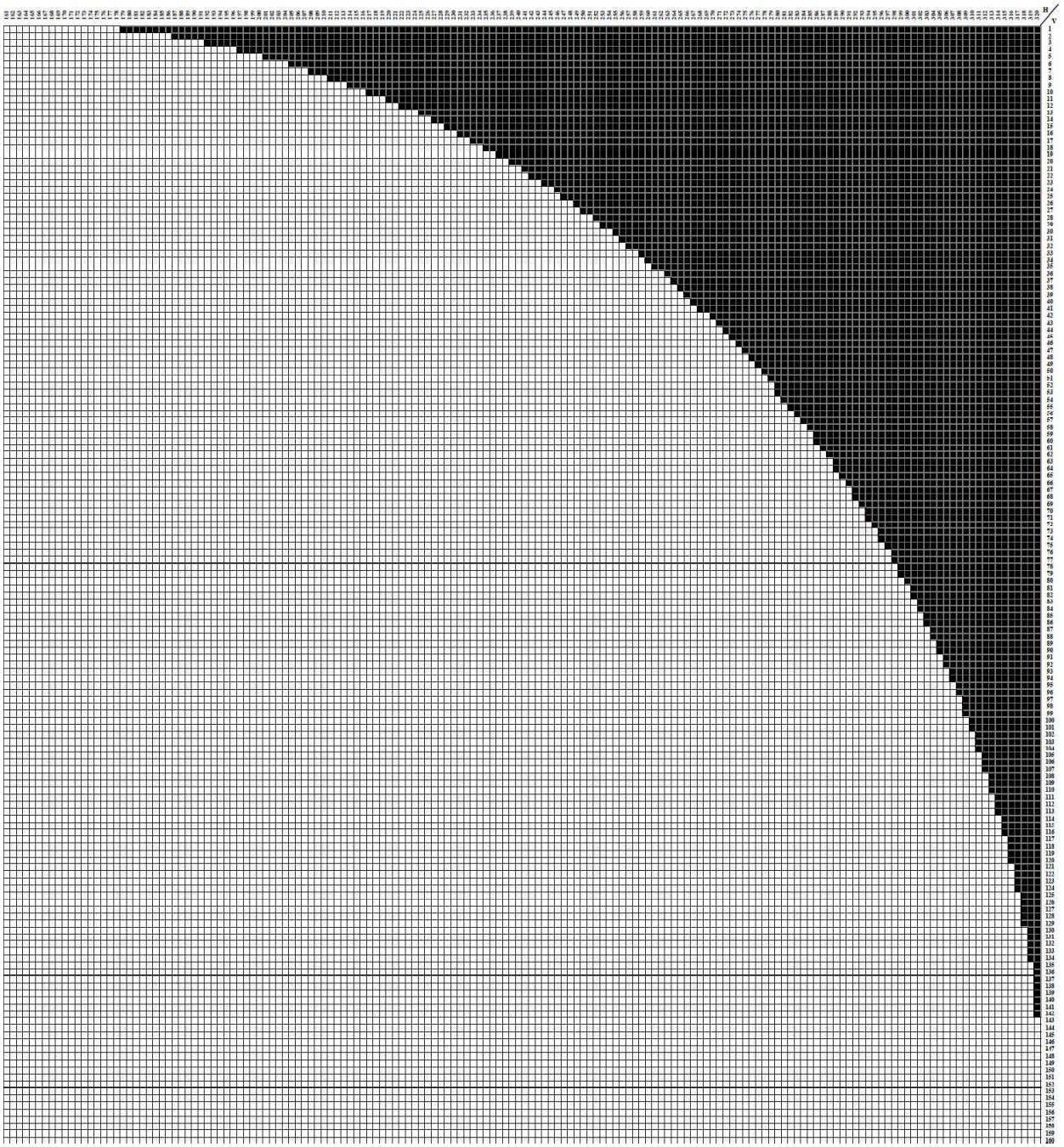


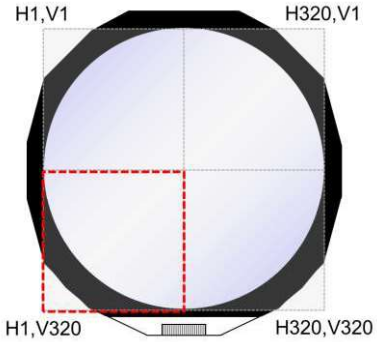
Pixels indicated “RGB” are displayed

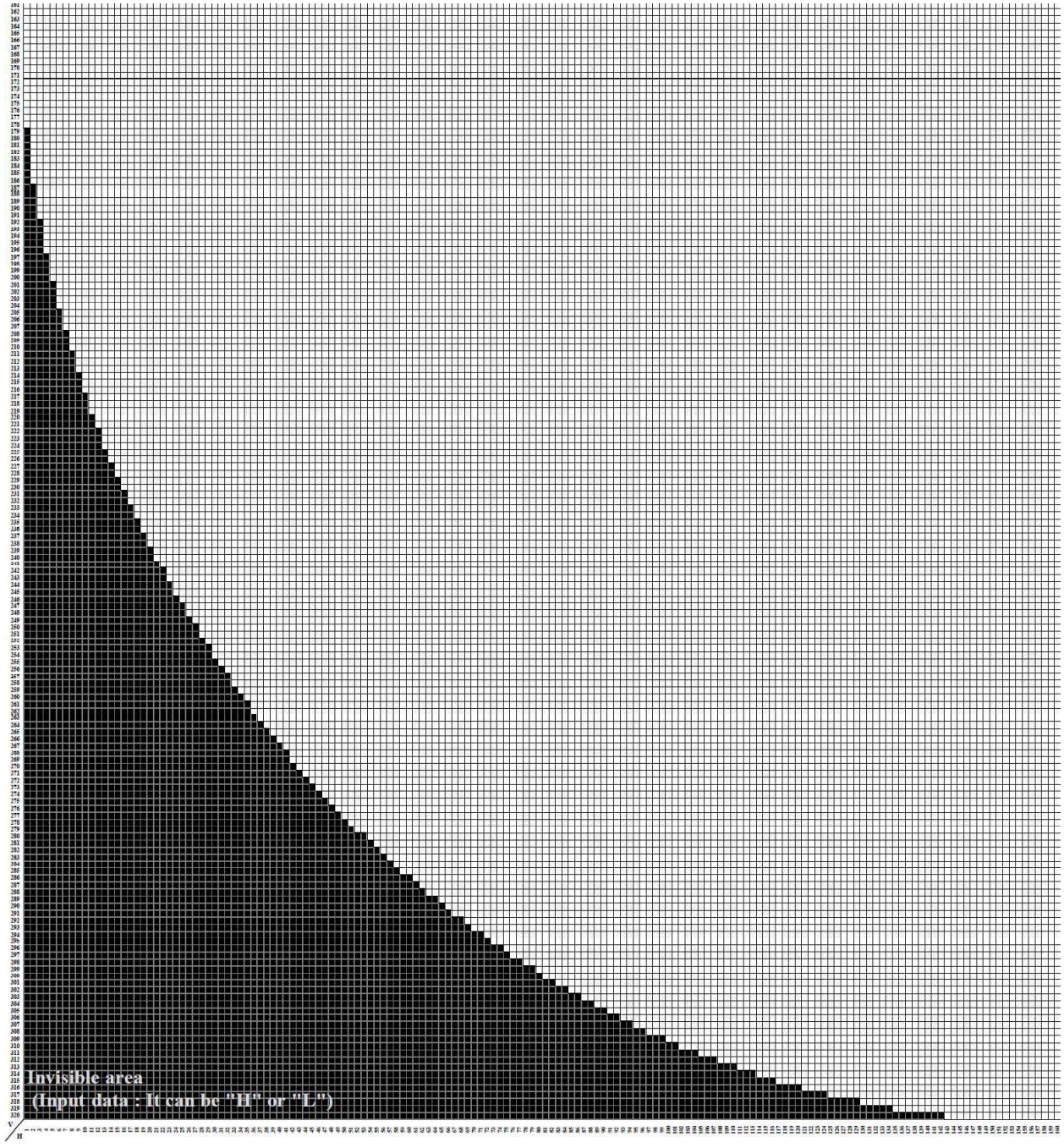
(Viewing in front of an LCD panel)

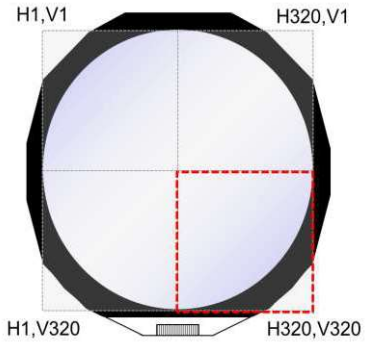


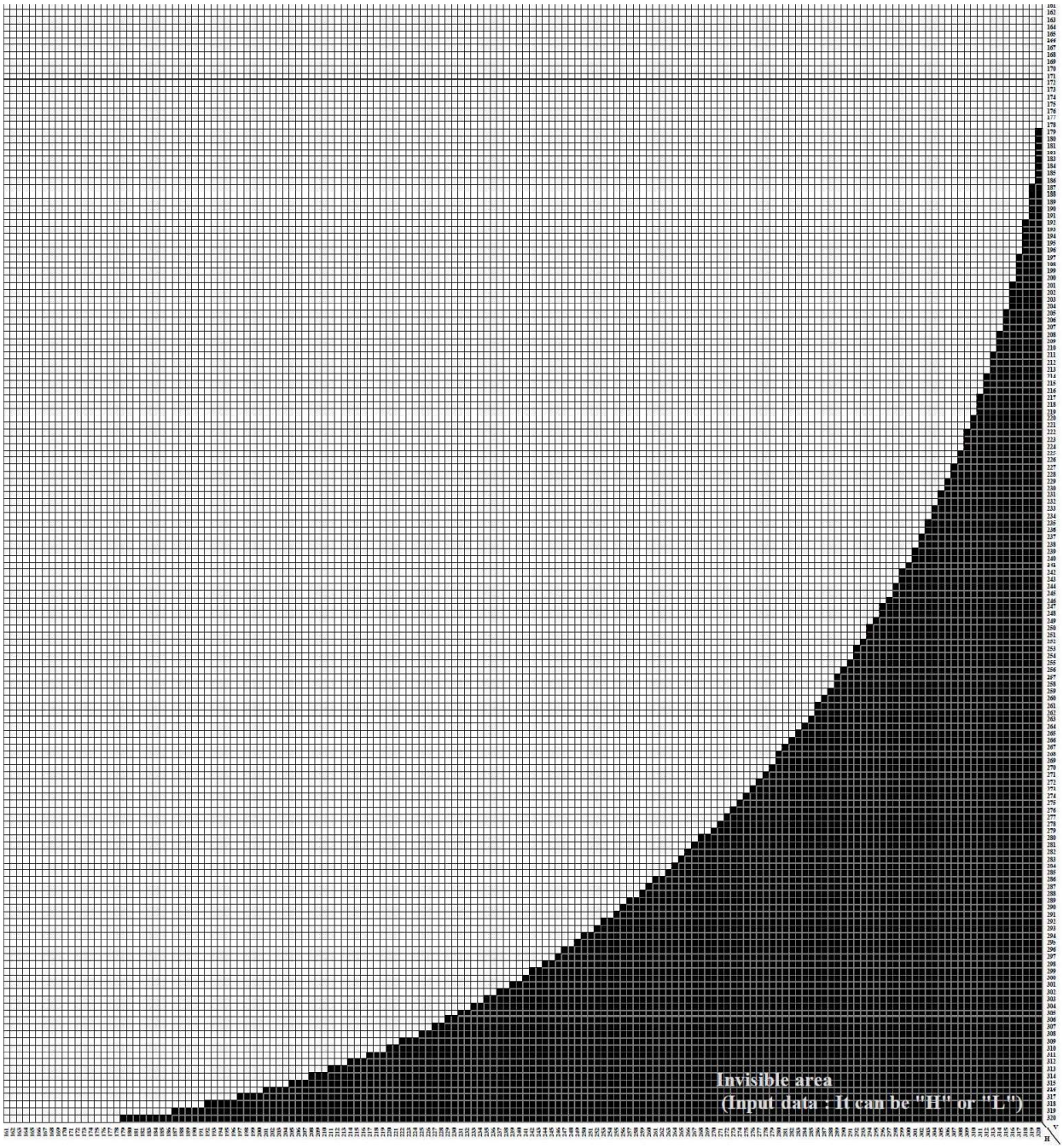

H1,V1
H320,V1
H1,V320
H320,V320




H1,V1
H320,V1
H1,V320
H320,V320


Invisible area
(Input data : It can be "H" or "L")


H1,V1
H320,V1
H1,V320
H320,V320


Invisible area
(Input data : It can be "H" or "L")

9. OPTICAL SPECIFICATION

9.1 OPTICAL CHARACTERISTICS

9.1.1 REFLECTIVE MODE

* Ta=25ºC VCI=3.1V, VDDI=1.8V, Analog(Normal) driving mode

Item	Symbol	Temp. (°C)	Rating			Unit	Definition (Measurement setup)	Remark
			Min.	Typ.	Max.			
Contrast	*CR*	25	10	25	-	-	1	
Response	*tr*	25	-	3	6	ms	2	Black → White
	tf		-	6	10			White → Black
Color coordinates	*Rx*	25	-	0.505	-	-	3	*Reference value
	Ry		-	0.315	-			
	Gx		-	0.300	-			
	Gy		-	0.445	-			
	Bx		-	0.170	-			
	By		-	0.175	-			
	Wx		-	0.315	-			
	Wy		-	0.335	-			
NTSC ratio	-	25	-	23	-	%	4	
Reflectance	-	25	-	24	-	%	Basic measurement condition & Measurement system	
Viewing Angle (CR>2)	θL	25	50	60	-	°	5	Horizontal
	θR		50	65	-			
	θT		50	65	-			Vertical
	θB		50	60	-			
Flicker	-	25	-	-	5	%	6	50% Gray
Crosstalk	-	25	-	-	3	%	7	Black / 50% Gray

9.1.2 TRANSMISSIVE MODE

* VCI=3.1V / VDDI=1.8V / ILED=19mA

* Analog (Normal) driving mode White laster

Item	Symbol	Temp. (°C)	Rating			Unit	Remark
			Min.	Typ.	Max.		
Brightness	*B*	25		(10)	-	Cd/m2	

9.2 DEFINITION AND CONDITION OF OPTICAL CHARACTERISTICS

9.2.1 DEFINITIONS OF OPTICAL CHARACTERISTICS

Definition 1

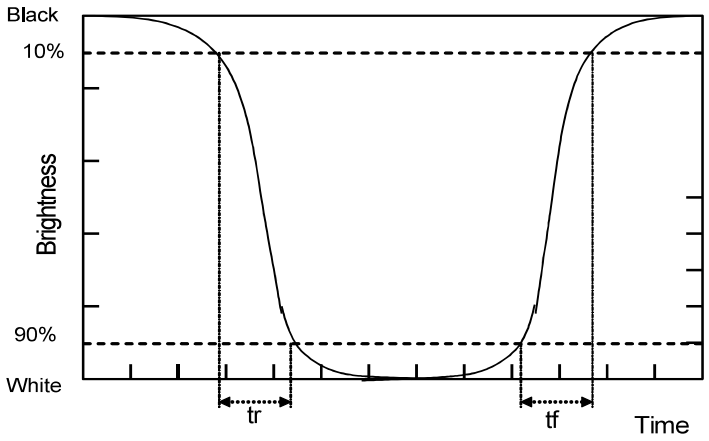
This is a ratio between the screen surface reflectance of the white raster and the black raster

$$\text{Contrast ratio (CR)} = \frac{\text{Reflection intensity on all pixels White}}{\text{Reflection intensity on all pixels Black}}$$

Definition 2

The response time is defined as the following figure and shall be measured by matching the input signal for “Black” and “White”.

▪ Normally Black mode



tr : Response time from Black to White

tf : Response time from White to Black

Definition 3

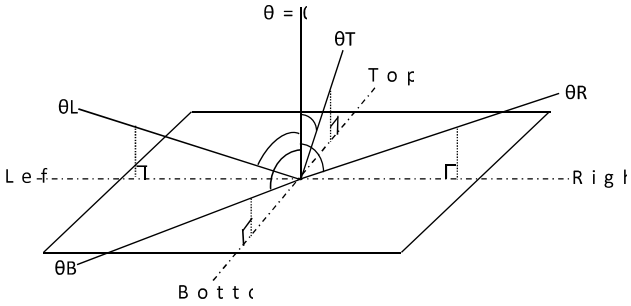
This is the x-y coordinate of Red, Green, Blue and White colors specified on the CIE1931 chromaticity diagram. (* It is not a guaranteed value) *D65 / 2 degree viewing angle

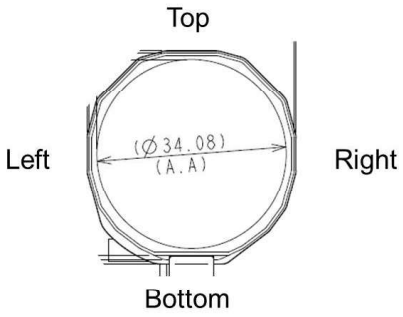
Definition 4

This is an area of a triangle shaped by R, G and B coordinates on the CIE1931 chromaticity diagram.

Definition 5

This is a maximum angle θ from the normal direction that keeps having the contrast more than 2.





Definition 6

Flicker is measured by color analyzer(Gray 50%).

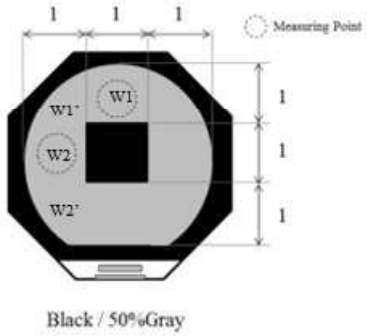
Definition 7

Gray 50% and black window display.

Crosstalk is measured by Each 2 points luminance difference.

$$\text{Crosstalk} = \left| \frac{Wi' - Wi}{Wi} \right| \times 100(\%)$$

i=1or2



Black / 50%Gray

< Basic measurement conditions >

a) Driving voltage

VCI=3.1V

VDDI = 1.8V

b) Measurement temperature

25°C unless otherwise specified

c) Measurement point

Center of the Active area (one point) unless otherwise specified

d) Measurement equipment

Reflective mode: LCD-5200 (Otsuka Electronics) or similar instrument

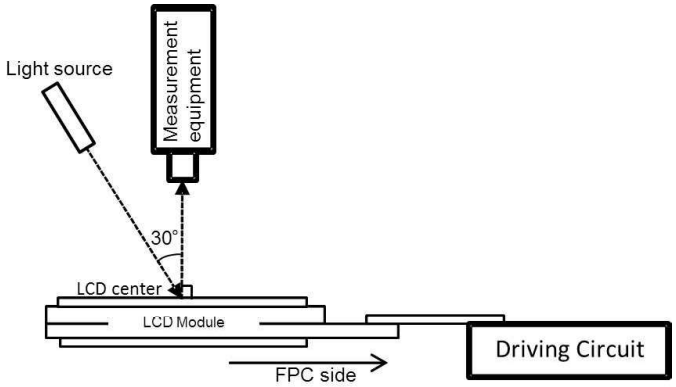
Transmissive mode: CS-2000A or similar instrument

e) Light source

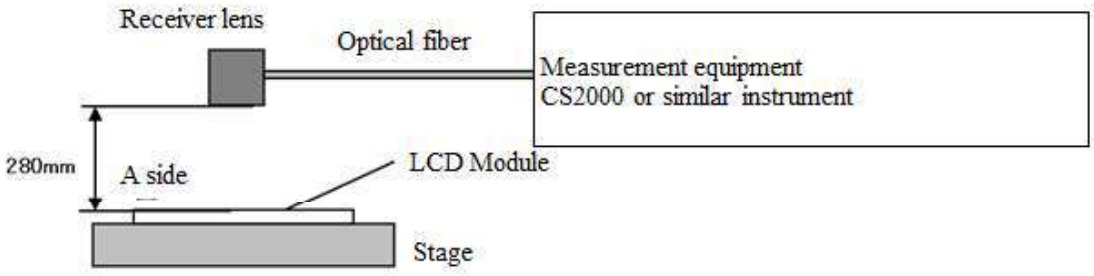
Parallel light source

- Light source input direction: form Top side (30°)
- Light source receive direction: at LCD center (0°)

< Measurement system- Ⅰ for reflective mode>



< Measurement system- Ⅱ for transmissive mode >



10. INSPECTION

10.1 QUALITY STANDARD

10.1.1 INSPECTION CONDITION

(1) Ambient Conditions

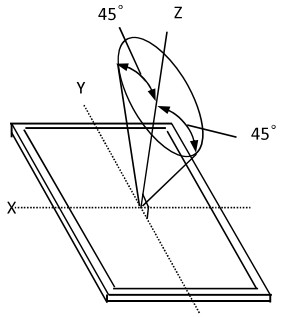
Temperature	: 25 ℃ (±5℃)
Humidity	: 60% (±20%)
Ambient Luminance	: 1000 – 2000 lux
Supply Voltage	: VDDI=1.8V, VCI=3.1V

(2) Viewing Distance

The distance between the LCD and the inspector's eyes should be 30cm (±10cm).

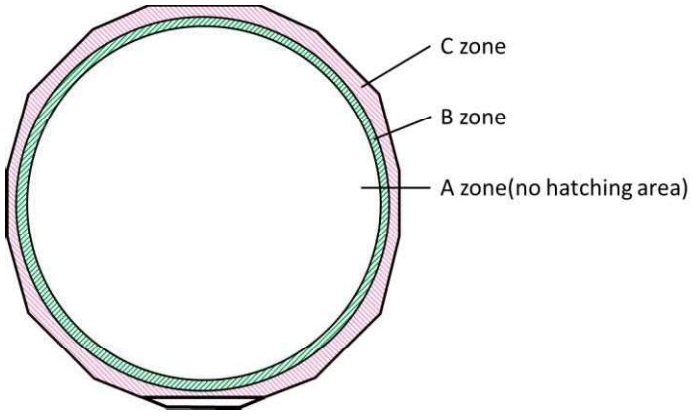
(3) Viewing Angle

Viewing angle shall be ±45 degrees from the vertical direction as shown below.



10.1.2. ZONE DEFINITION

A zone	: Active area
B zone	: Viewing area(AA+0.4mm)
C zone	: Except A and B zone



*For detail dimensions refer to outline drawing.

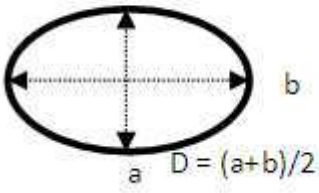
10.1.3 TREATMENT OF PROBLEMS

If there are any troubles which are concerned with our products assembled at your company's manufacturing processes, both companies shall jointly investigate and resolve the cause.

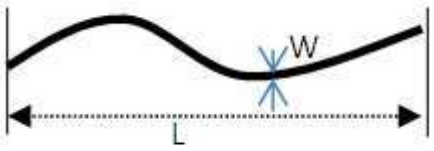
10.2 DISPLAY APPEARANCE STANDARDS

Item		Zone	Criteria		Remark
Name	Cause		Size(mm)	N.	
Dot type defect	B/W spot (Dent in glass or Upper polarizer, Particle, Swell) Bright/Dark dot defect	A	D≦0.15	Ignore	
			0.15＜D≦0.25	2	Keep two defect distance more than 5mm
			0.25＜D	0	
		B	D≦0.25	Ignore	
			0.25＜D≦0.3	3	Keep two defect distance more than 5mm
			0.3＜D	0	
		C	Ignore		
Line type defect	Scratch on polarizer or Foreign material between Upper polarizer and glass	A	W≦0.03	Ignore	
			0.03＜W≦0.08 , L≦2	2	Keep two defect distance more than 5mm
			0.08＜W or 2＜L	0	
		B	W≦0.10 , L≦3	3	
			0.10＜W or 3＜L	0	
		C	Ignore		
Air bubble	Air bubble (Not panel)	A	D2≦0.25	2	
			D1≦0.20	2	
			0.5＜D1+D2	0	
		B	Ignore		
		C	Ignore		

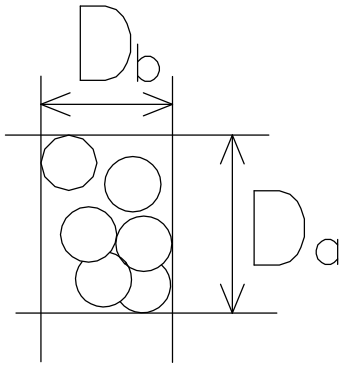
Dot type defect



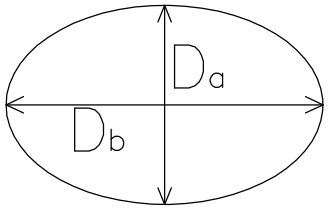
Line type defect



Aggregate of small air bubbles



Big air bubble



*When there is an agreement limit samples, Item is judged according to the limit sample.

Total defect quantity: A zone (N≦3) each inspection(lighting / appearance) , B zone (N≦5)

*Other items are to be decided by agreement between both parties.

*Aggregate of small air bubbles: The longer one is defined as D1 among Da and Db.

*Big air bubble: The longer one is defined as D2 among Da and Db.

* Count defects separately in reflective mode and transmissive mode. Individual values are not summed up.

10.3 EXTERNAL APPEARANCE STANDARDS

Item	Criteria		Remarks
	Size(mm)	Number	
Chipping	(A) W≦3 , L≦0.2 , T=1/2t	Ignore	Fig.1
	(B) W≦3 , L≦0.6 , T<1/2t	Ignore	Fig.2
	Except (A) & (B)	0	
Chipping on the corner	Showing on below figure		Fig.3 & Fig.7
Projection	W≦0.3 , L≦5.0	Ignore	Fig.4
	0.3<W or 5.0<L	0	
Corner burr	W≦0.5 , L≦5.0	Ignore	Fig.5
	0.5<W or 5.0<L	0	
Crack (*6-1)	W≦3 , L≦0.5	Ignore	V-shaped chipping included , Fig.6
	3<W or 0.5<L	0	

Note) (*6-1)"Crack" means the one which would progress further.

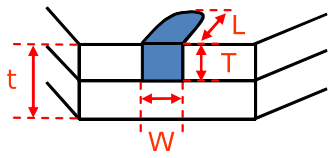


Fig.1

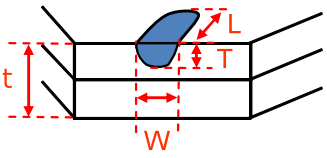


Fig.2

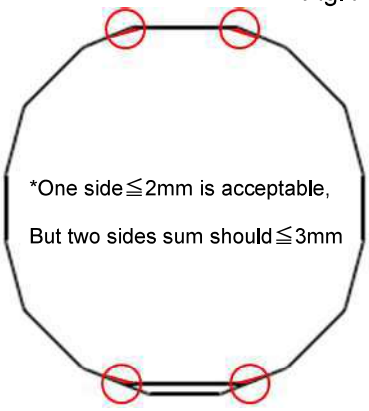


Fig.3

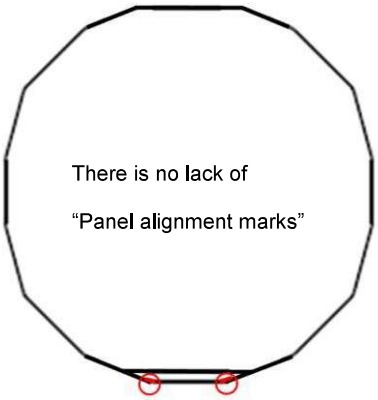


Fig.7

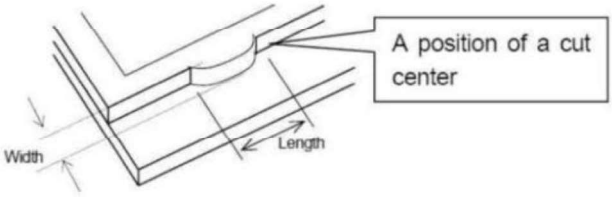


Fig.4

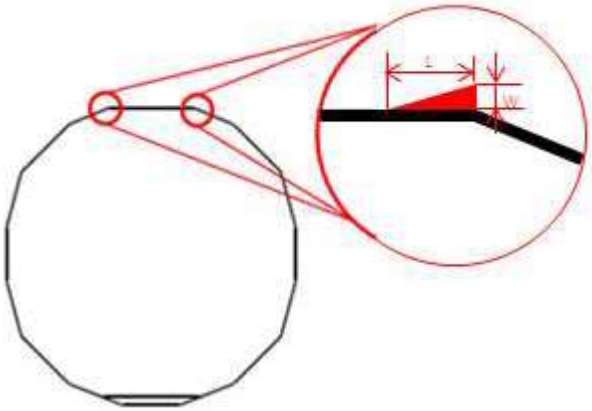


Fig.5

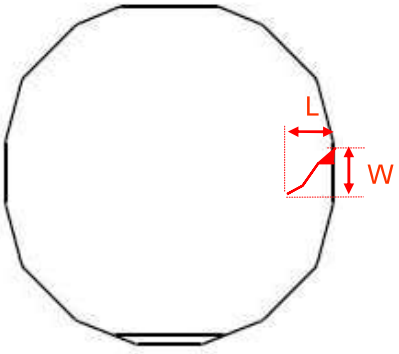


Fig.6

11. RELIABILITY SPECIFICATION

11.1 CONDITIONS OF RELIABILITY AND MECHANICAL TEST

No.	TEST ITEM	CONDITION		REMARK
1	High Temperature Storage	Ta=80°C	240h	
2	Low Temperature Storage	Ta=-30°C	240h	
3	High Temperature & High Humidity Storage	Ta=60°C／90%RH (No condensation)	240h	
4	High Temperature & High Humidity Operation	Ta=60°C／90%RH (No condensation)	240h	
5	High Temperature Operation	Ta=70°C	240h	
6	Low Temperature Operation	Ta=-20°C	240h	
7	Thermal shock (non-operating)	Ta=-30°C to 80°C (30min each)	100cycles	
8	ESD	HBM IEC 61340-3-1, ESD STM5.1 V = ±1.0kV (Contact) R = 1.5kΩ, C = 100pF	1 time each terminal	
		Contact discharge(Power off) C=150pF, R=330Ω V=+/-4kV	-	
9	Shock	100G, 6ms, ±X, ±Y, ±X	3 times each direction	
10	Packing Vibration	Random Vibration 5～500Hz	101min Direction Z	(*11-1)
11	Packing Drop	Height 60cm, 1 corner 3 edges, 6 surfaces	1 time Each direction	(*11-1)

Note)

(*11-1) Tests are conducted package.

Above test evaluate for development. It is not guaranteed value for lot acceptance.

If a nonconformance is found, both parties will have a discussion to solve it.

11.2 CRITERIA FOR JUDGEMENT

After the above tests, return samples to the normal temperature and moisture environment in the thermostat chamber room over 30 minutes not to condense. Inspect samples kept for more than 1 hour after pulling them out of the thermostat chamber room.

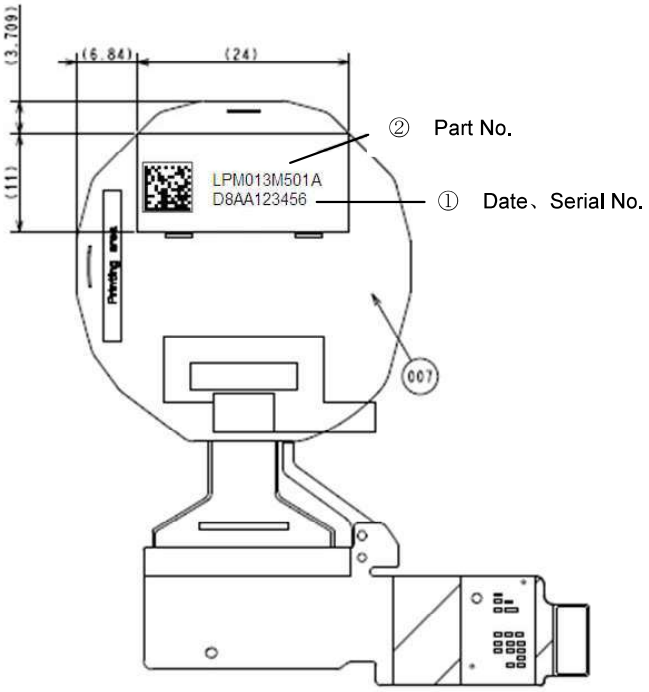
(1) There shall be no abnormality in the functions (Ex. No display, abnormal display, line defects).

(2) There shall be no serious degradation.(Ex. Brightness uniformity, reversible changes, optical changes due to polarizer are ignored.)

12. DESIGNATION OF LOT MARK

12.1 LOT MARK

Mark	digit	Item	Note
①	11	Part No.	LPM013M501A
②	10	Date、Serial No.(Decimal)	1st digit:productionsite D:DPTE
			2nd digit:Last digit of year
			3rd digit:Month Jan~Sep = 1~9 A=Oct B=Nov C=Dec
			4th digit:Rev.(Example A B C D……)
			5th digit:Serial No.(Normal lot=000001~999999)

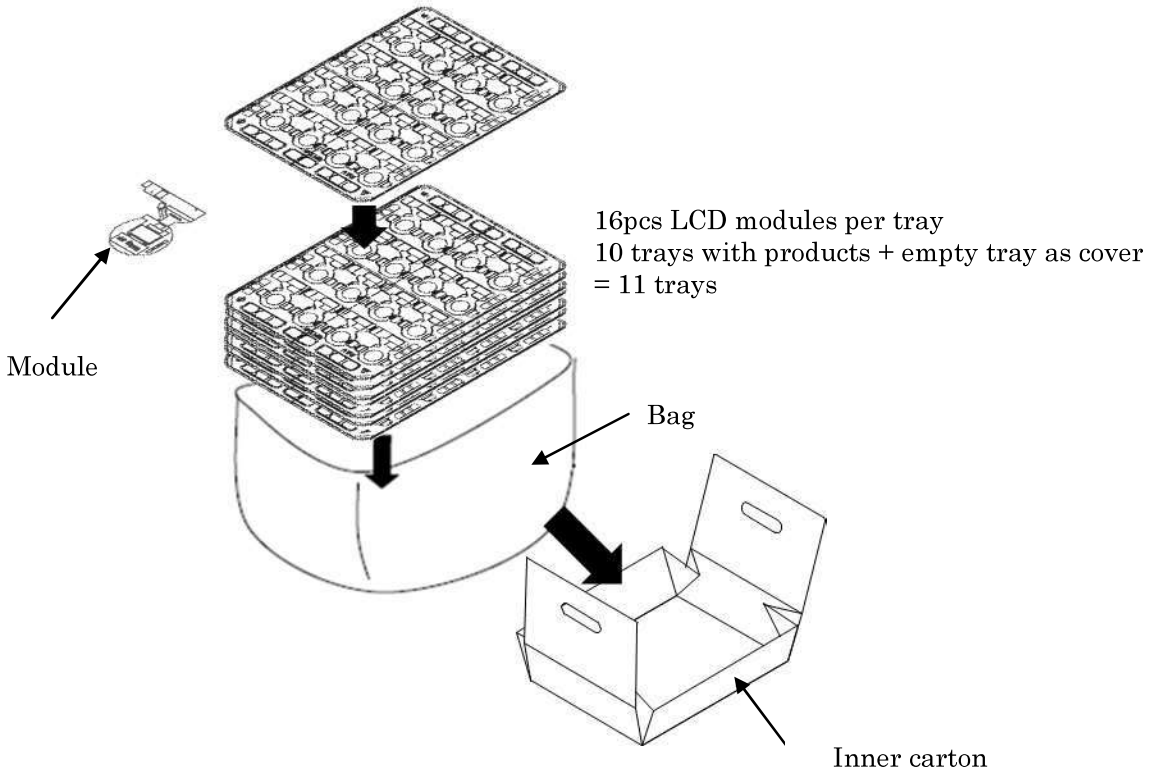


13. PACKING SPECIFICATIONS

13.1 INNER CARTON

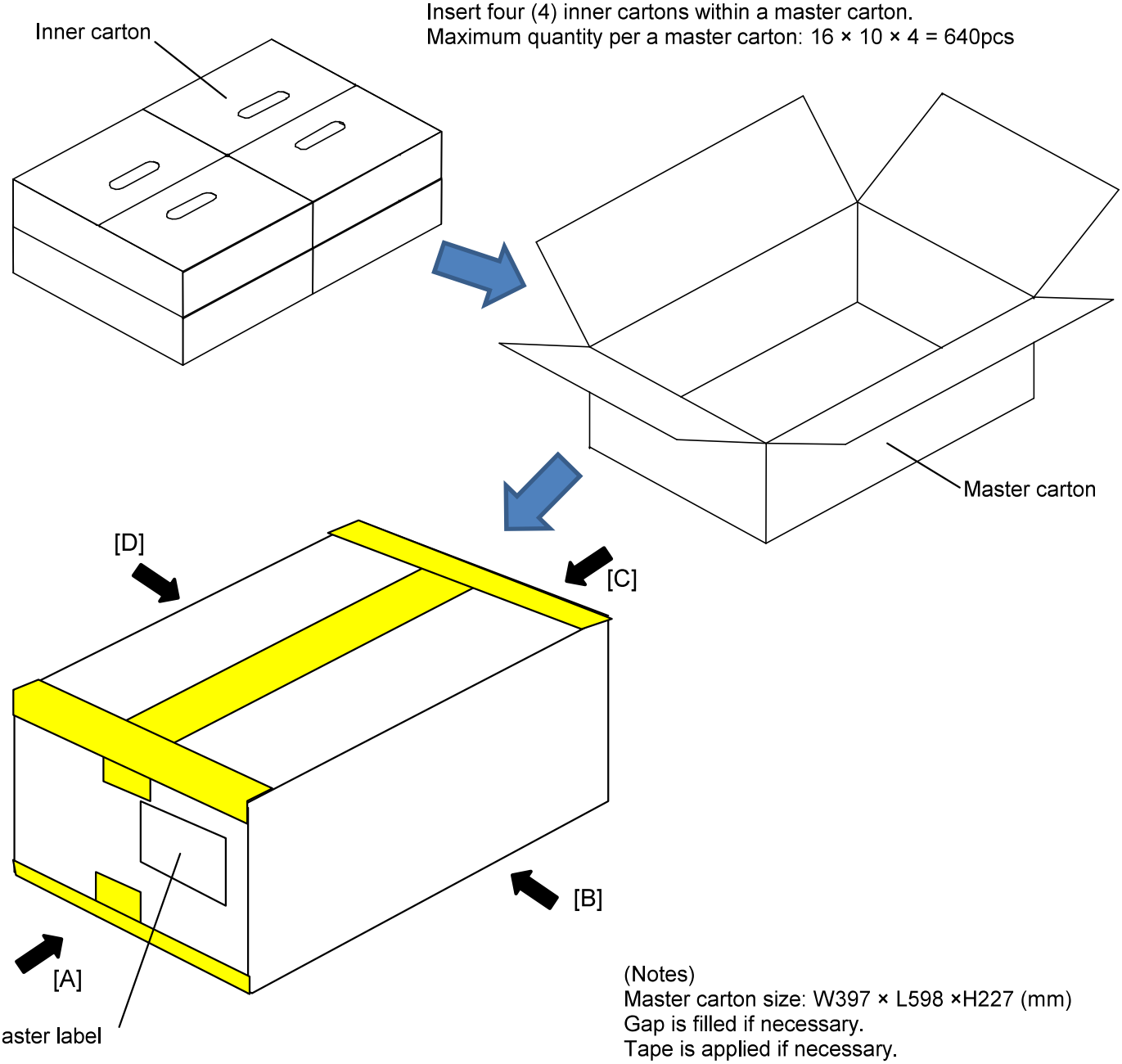
16pcs LCD modules per tray.
10 trays with products + empty tray as cover=11 trays

Note)
Tray orientation must be kept its original direction.
If you do not stack trays alternately, it will lead to panel damaged.



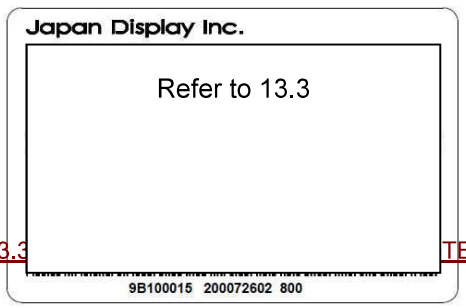
13.2 MASTER CARTON

Insert four (4) inner cartons within a master carton.
Maximum quantity per a master carton: 16 × 10 × 4 = 640pcs

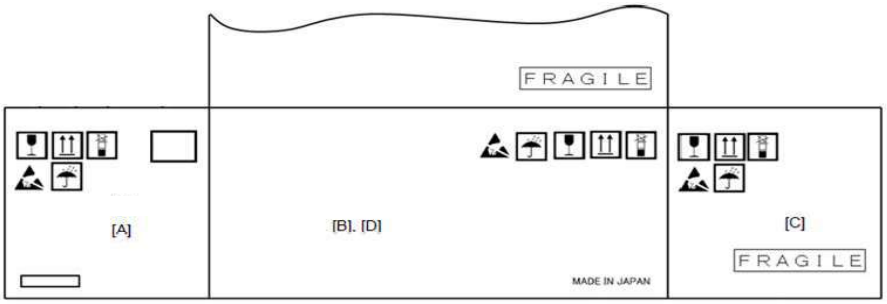


(Notes)
Master carton size: W397 × L598 ×H227 (mm)
Gap is filled if necessary.
Tape is applied if necessary.
Tied if necessary

Contents of master label



Indication onto [A] [B] [C] [D] on master carton are shown as below



13.3 TER

LABEL EXAMPLE

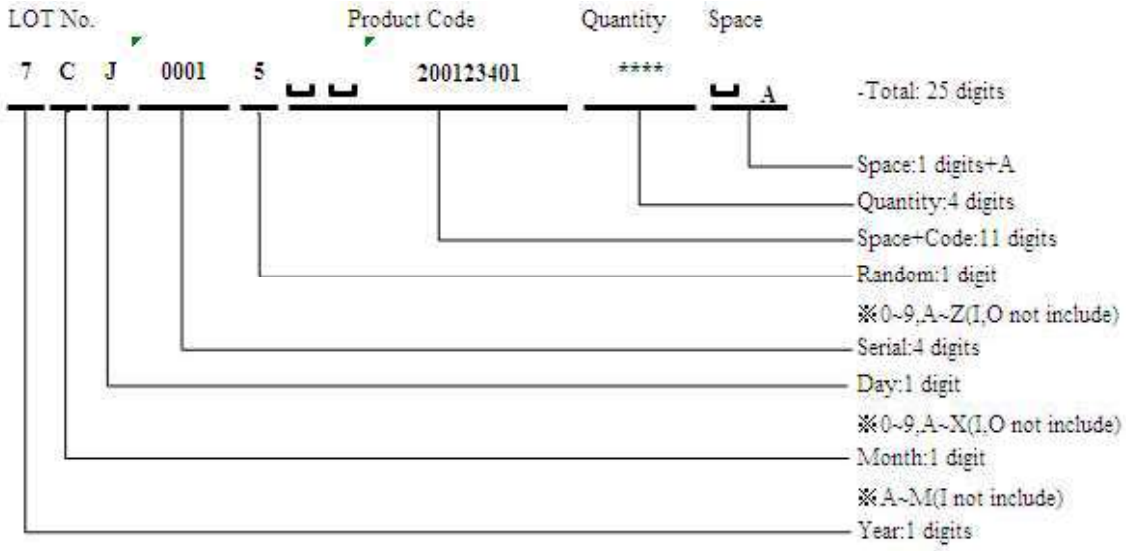
Detail of Label

	Items	Detail of print
1	Product Code	200123401
2	Product Name	LPM013M501A
3	Quantity	640pcs
4	Date Code	"Year-Month-day"、End"-0000"fixed
5	RMK	-
6	Producing country	MADE IN CHINA
7	LOT No.	Bar code (LOT No.) *detail as below

Detail of Barcode

	Items	Detail of Print
8	LOT No.	LOT No.(8 digits) + Space(2 digits) +Product Code(9digits) + Quantity(4 digits) + Space(1 digits)+A(1 digits)

Detail of Barcode



14. LCD MODULE USAGE AND PRECAUTIONS

14.1 HANDLING

(1) The display panel is made of glass. Do not subject it to mechanical shock such as dropping it from a high position, etc.
(2) If the display panel is damaged and internal liquid crystal substance leaks out, be sure not to inhale or consume it. If the internal liquid crystal substance comes into contact with skin or clothing, promptly wash it off using soap and running water.
(3) Do not apply excessive force on the surface, perimeter or adjoining areas of LCD module since this may cause display panel color tone to vary.
(4) The polarizer covering the display panel surface of the LCD module is soft and can be easily scratched or dented. Handle this polarizer carefully.
(5) If the surface polarizer becomes contaminated, use the following recommended or equivalent adhesive tape for contaminants removal.
• Scotch-brand mending tape (No. 810)
(6) Do not breathe on the display surface or use Ethyl Alcohol solvent for contaminant removal as polarizer discoloration may occur. Furthermore, solvent other than mentioned above may also damage the polarizer. Especially, do not use the followings.
• Water
• Ketones
• Aromatic solvents
(7) When mounting the LCD Module, be sure that it is free from twisting, warping, or distortion. Any stress can have great influence to the display quality. Also, in cases where outer case or frame is included, be sure to secure sufficient stiffness on the outer case or frame for a robust design.
(8) Do not apply pressure at or around the FPC bonding area and the surrounding area.
(9) Do not attempt to disassemble or rework the LCD module.
(10) To prevent destruction of the elements by static electricity, be careful to maintain an optimum working environment.
• Be sure to ground your body before handling the LCD module.
• Make sure that solder guns and all other tools required for assembly have been grounded.
• To reduce occurrence of static electricity, avoid using this product in dry environments.
• A protective film has been attached to the surface of the LCD panel. When peeling off the protective film, be careful to prevent electrostatic discharges.
(11) To minimize performance degradation of the LCD module caused by destructive forces such as static electricity, etc., avoid direct contact to the following sections when handling the LCD module.
• terminal electrodes of connector
• wiring pattern on FPC
(12) LCD Panel surface is protected by a protective film layer. This protective film must be removed before final product installation. After removal of protective film layer, some adhesive residues maybe left on the LCD panel, especially after long storage period, please refer to section 5) listed above for proper contaminant removal procedure.
(13) Take precaution to minimize corrosion of electrodes. Corrosion of electrodes is accelerated by moisture, condensation or a current flow in a high-humidity environment.
(14) Do not apply excessive pressure to the FPC part. Force type such as twist, warp, etc., may damage FCP patterning traces.
(15) Do not use sharp, pointy or rigid tools when handing LCD panels. These objects can scratch or nick the glass panel which can cause it to crack.
(16) Do not touch or handle the LCD module directly with bare hands. Residue of dirt, oil or water may have the possibility to cause corrosion. Be sure to wear finger sacks or gloves when handling LCD modules. When holding an LCD panel module, carefully hold the panel by the edges of the glass plate.
(17) Avoid using LCD module under condensation or high humidity environment because polarizer etc. maybe damaged in these conditions.
(18) Trays are used to package LCD modules for shipment. If LCD modules scratch the tray during shipment, material of the scratched tray may be left on LCD modules. In such case, clean up LCD modules after removal from trays.
(19) When installing LCD module, don't apply excess stress of bending or stretching to the input cable

(20) Keep NC terminal open electrically.
(21) After storage under high humidity or condensation environment, keep LCD module under room temperature more than 30 minutes before operation.
(22) Take precautions to handling LCD module because the glass plate has very keen edges.

14.2 DESIGN OF APPLICATION

(1) The absolute maximum ratings represent the rated values which LCD module cannot exceed. When LCD modules are used beyond this rated value, the operating characteristics may be adversely affected.
(2) To prevent the occurrence of erroneous operation caused by noise, special attention on satisfying VIL, VIH specified values is required. This includes taking the precautionary measures of using short cables for signal transferring.
(3) An inherent characteristic of liquid crystal display is its temperature dependency. Be sure to use the LCD modules within the specified operating temperature range, as recognition of the display becomes difficult when the LCD module is used outside its range. Also, keep in mind that the voltage levels necessary for clear display images will vary according to temperature.
(4) It is recommended that power supply lines to include current surge protection. (Fuse etc. recommend value: 0.5A)
(5) Note the peripheral devices can cause mutual noise interference with LCD modules. Especially, input devices such as Touch Panel, etc., may output operational level by radiation noise even when these devices are not in operation. Actual performance confirmation and verification under actual usage environment by actual final product is highly recommended.
(6) To avoid EMI, preventive measures should be implemented in the final product.
(7) Display abnormality may occur with sudden removal of power supply such as device battery. Sudden removal of power supply shall be avoided at all time. LCD module quality cannot be guaranteed under such condition.
(8) Ensure sufficient light shading measures during design phase and when assemble the LCD module.
(9) Ensure sufficient light shading measures in the inspection process.
(10) Similar to general electronic components, ESD may cause LCD IC to malfunction. ESD preventive measures should be considered around the LCD module.
(11) While display data may be kept, data can be easily changed by external noise. Noise shall be minimized at device or system level.
(12) As unexpected noise may occur, periodic refresh operation such as resend the command and display data is highly recommended as part of the software routine.
(13) When logic circuit power is off, do not apply any signals to the input terminals.
(14) Do not use other components such as FPC or other features to fix the LCD module position, as pressure/tension may produce undesired result such as FPC trace crack.

14.3 DISPLAY CHARACTERISTICS

(1) Because the optimum LCD driving voltage depends on the ambient temperature, display may slightly flicker at the environment of high temperature.
(2) One of the special characteristics of liquid crystal is that it freezes when stored at the temperature below the storage temperature range. Such freezing may cause orientation defects or bubbles (black or white) to appear in the LCD panel. Bubbles may also occur if the panel receives an impact in a low-temperature environment.
(3) If the LCD module is left operating for a long time with the same display showing, the displayed pattern may leave traces on the screen or the contrast may become inconsistent.

14.4 KEEPING THE PRODUCTS

(1) When keeping LCD modules, avoid the following condition or environment.
• Exposure to direct sunlight or fluorescent lamps lightings.
• High-temperature/high-humidity or very low-temperature (below 0°C) environments.
• Exposure to water droplets, condensation, etc.
Furthermore, keep LCD modules in anti-static bags to prevent static electricity charge ups. Whenever possible, LCD modules should be stored in the same conditions in which they were shipped from Japan Display Inc.
(2) Take precaution to minimize corrosion of electrodes. Corrosion of electrodes is accelerated by moisture, condensation or a current flow in a high-humidity environment.
(3) Recommended keeping conditions.
• Keeping environment : +15°C to 35°C, less than 65%RH
• Duration: up to 2 months after shipping date
(4) The shipping carton must not be stacked up over 1.5m in height.

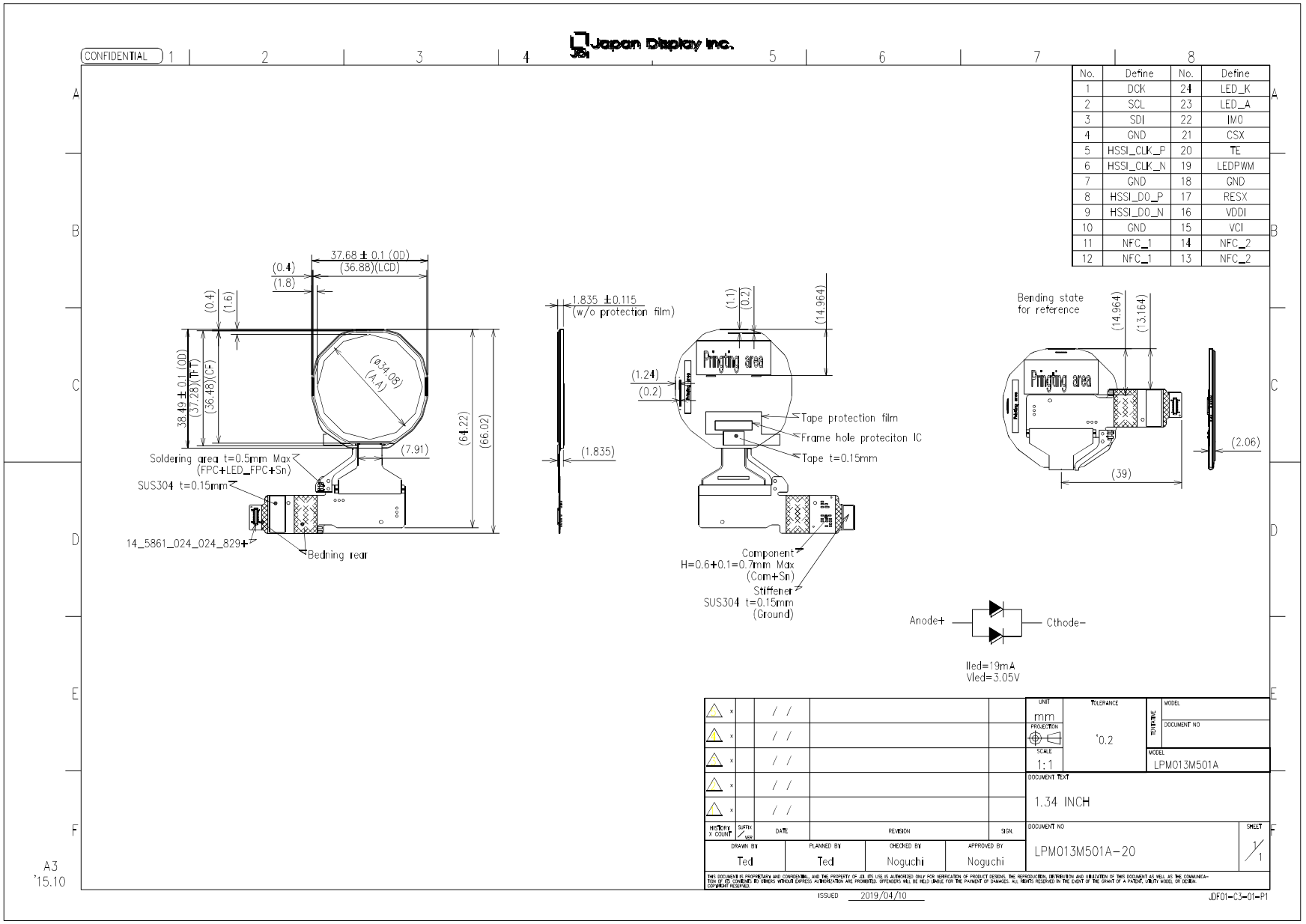
14.5 DISPOSAL

(1) When disposing LCD modules, consult company specialized in industrial waste treatment which is permitted by the government or local authority. When incineration is the method of LCD module disposal, law of environmental hygienic must be obeyed.

14.6 OTHERS

(1) This product is designed to be used in ordinary electronic devices. Do not use this product in other applications, especially in devices that may cause direct bodily damage to end users (such as aerospace equipment, traffic control equipment, medical equipment, life-support system equipment, or safety equipment).
(2) Japan Display Inc. shall not be responsible for defects that occur in this product or in equipment connected to this product if the product is used in an environment that exceeds the ranges specified in this document, or in an environment not described in this document.

15. DRAWING


Japan Display Inc.
CONFIDENTIAL
No. Define No. Define
1 DCK 24 LED_K
2 SCL 23 LED_A
3 SDI 22 IM0
4 GND 21 CSX
5 HSSI_CLK_P 20 TE
6 HSSI_CLK_N 19 LEDPWM
7 GND 18 GND
8 HSSI_D0_P 17 RESX
9 HSSI_D0_N 16 VDDI
10 GND 15 VCI
11 NFC_1 14 NFC_2
12 NFC_1 13 NFC_2
37.68 ± 0.1 (OD)
(36.88)(LCD)
(0.4)
(1.8)
(0.4)
(1.6)
38.48 ± 0.1 (OD)
(37.28)(T-T)
(36.48)(C-)
(ø34.08)
(A.A)
(7.91)
(64.22)
(66.02)
Soldering area t=0.5mm Max
(FPC+LED_FPC+Sn)
SUS304 t=0.15mm
14_5861_024_024_829+
Bedning rear
1.835 ±0.115
(w/o protection film)
(1.835)
(1.1)
(0.2)
(14.964)
Pimgting area
(1.24)
(0.2)
Tape protection film
Frame hole proteciton IC
Tape t=0.15mm
Component
H=0.6+0.1=0.7mm Max
(Com+Sn)
Stiffener
SUS304 t=0.15mm
(Ground)
Bending state
for reference
(14.964)
(13.164)
Pimgting area
(2.06)
(39)
Anode+
Cthode-
Iled=19mA
Vled=3.05V
UNIT mm
TOLERANCE ±0.2
PROJECTION
SCALE 1:1
MODEL LPM013M501A
DOCUMENT TEXT 1.34 INCH
DOCUMENT NO LPM013M501A-20
SHEET 1/1
DRAWN BY Ted
PLANNED BY Ted
CHECKED BY Noguchi
APPROVED BY Noguchi
ISSUED 2019/04/10
JDF01-C3-01-P1
A3
'15.10