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SHARP

No.	**LD-25453F**
DATE	6th. Jan. 2014

TECHNICAL LITERATURE

FOR

TFT - LCD module

These parts have corresponded with the RoHS directive.

MODEL No. LQ070M1SX01

The technical literature is subject to change without notice. So, please contact SHARP or its representative before designing your product based on this literature.

DEVELOPMENT DEPARTMENT II
DISPLAY DEVICE UNIT II
DISPLAY DEVICE BUSINESS DIVISION
SHARP CORPORATION

Records of Revision

Model Name:LQ070M1SX01

Spec No.	Date	Revised No.	Summary		Note
			Page		
LD-25453	2013/04/19				First Issue
LD-25453A	2013/06/19	△1	4 9	Overview, Features Chart 7-1, Chart 8-1	
LD-25453B	2013/07/12	△2	4 9	Overview, Features Chart 7-1, Chart 8-1	
LD-25453C	2013/10/07	△3	All 4 8 9 9-10 10-14 15 16 17-19 20 21	Model Name Updated. Mechanical Specifications Updated. LED_FPC PIN Assignments Updated. Chart 7-1 Corrected. DC Characteristics Updated 8.MIPI Updated 9. Power Sequence Updated 10. External Circuitry Updated 11.Optical Specification Updated Reliability Test Items Updated Fig. 5-1 Outline Dimensions Updated	
LD-25453D	2013/11/20	△4	9 15 16 16-17 18	LED forward current：Condition Updated 9-1 Power On Sequence Updated 9-2 Power Off Sequence Updated 9-3 ON and Off Power Sequence C20 ：2.2uF→4.7uF	
LD-25453E	2013/11/22	△5	17 19	chart9-3 Power Sequence (t17) Updated Contrast ratio Updated	
LD-25453F	2014/1/6	△6	6-8 10 15-16 17 20 25	Update pin assignment Chart 8-2-1 DC Characteristics2 Updated MIPI video input timing Updated On Sequence updated External Circuitry Updated Note of protection film Updated	

Table of contents

1.Application

This technical literature applies to a color TFT-LCD module, LQ070M1SX01.

2.Overview △1

This module is a color active matrix LCD module incorporating TFT (Thin Film Transistor) and Oxide Semiconductor(IGZO).

Graphics and texts can be displayed on a 1200×3×1920 dots panel (323 ppi) with (16,777,216) colors by using MIPI (Mobile Industry Processor Interface) ,

This LCD module adopt the driver ICs(HX5263A:Himax Technologies,Inc.)

Information about the specifications of the driver IC, please refer to the data sheet of the driver IC.

3.Features

Display

- High-definition image achieved by 7.02 inch screen, vertical stripe WUXGA(1200xRGBx1920dots) .
- High grade display quality achieved by high aperture ratio panel, transparent color filter, transparent polarizer and high efficiency thin Backlight(with white LED) .
-Wide viewing angle and High-contrast achieved by ASV panel.
-Lightweight, thin-screen and compact form achieved by COG.
- MIPI Dual 2Lanes DSI is adopted. (SPI I/F is available when sending control commands.)

4.Mechanical Specifications

Chart 4-1 Mechanical Specifications △3

Parameter	Specifications	Unit
Display size (diagonal)	17.83 (7.02")	cm
Active area	94.5(H)x151.2(V)	mm
Pixel format	1200(H)xRGBx1920(V)	dot
Pixel pitch	0.02625(H) x 0.07875(V)	mm
Pixel configuration	Red, Green, Blue vertical stripe	-
Unit outline dimentions(projection portion not included)	99.7(W)×159.85(H)×1.725(D)(Note)	mm
Mass	(41 Typ)	g
Surface treatment	Clear hard coating	

(Note) Outline dimentions is shown in Fig.5-1

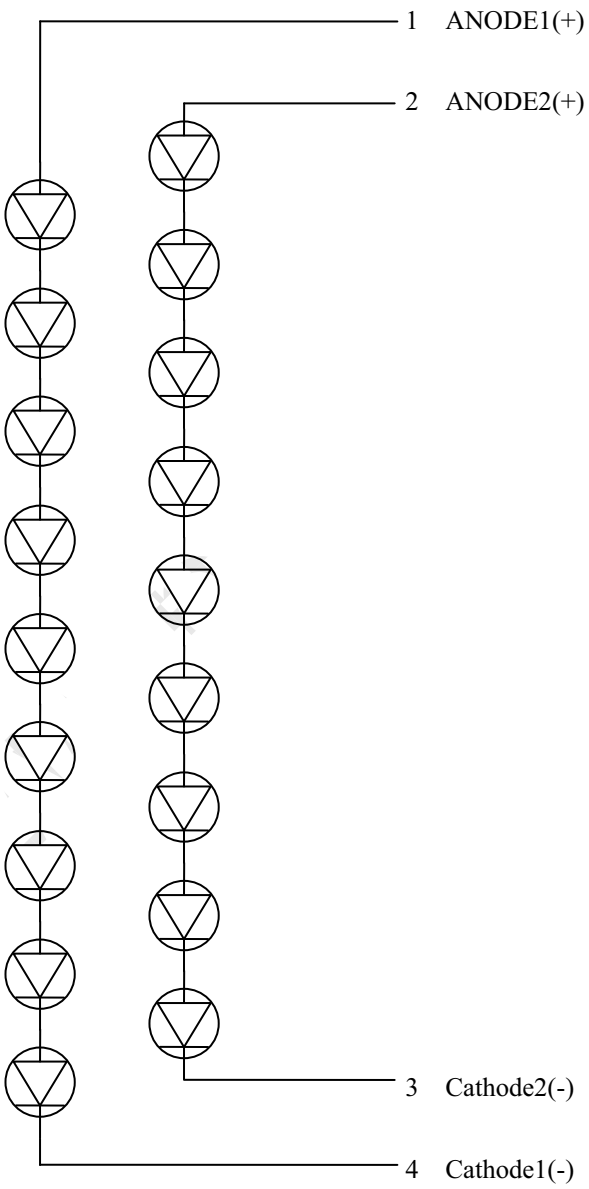
5.Structure

5-1 Contexture

This LCD module build up with TFT-LCD panel,FPC(TFT-LCD side), polarizer(CF front/ TFT back), control circuit insides LCD driver IC,white LED Backlight and LED-FPC.
Outline dimentions is shown in Fig. 5-1.

5-2 LED-FPC △2

LED-FPC Circuit



6.Input Terminals △6

Chart 6-1 TFT-LCD input terminal symbol

No.	Name	I/O	Description
1	VSN	P	input power (-5.5V ~ -6V)
2	VSN	P	
3	VSN	P	
4	DRVL_1	O	VGL Charge Pump controlled signal (VSSA ~ VSP)
5	DRVL_2	O	VGL Charge Pump controlled signal (VSSA ~ VSP)
6	DRVL_3	O	VGL Charge Pump controlled signal (VSSA ~ VSP)
7	VGL	P	Charge Pump input power (-16V ~ -6.5V)
8	VSP	P	input power (5.5V ~ 6V)
9	VSP	P	
10	VSP	P	
11	VSPO	O	VSP output voltage (5.5V ~ 6V)
12	VSPO	O	
13	DRVH_1	O	VGH Charge Pump controlled signal (VSSA ~ VSP)
14	DRVH_2	O	VGH Charge Pump controlled signal (VSSA ~ VSP)
15	DRVH_3	O	VGH Charge Pump controlled signal (VSSA ~ VSP)
16	VGH2O	O	VGH2 output voltage (Voltage equal to VGH2)
17	VGH2	P	Charge Pump input power (10V ~ 20V)
18	VGH1O	O	VGH1 output voltage (Voltage equal to VGH1)
19	VGH1	P	Charge Pump input power (10V ~ 20V)
20	AGND	P	Analog circuit ground (0V)
21	AGND	P	
22	AGND	P	
23	GPO1	O	General Purpose Output pin. .if don't use , keep this pin open.
24	DGND	P	MIPI circuit ground (0V)
25	CLKAP	I	MIPI clock lane port 1
26	CLKAN	I	MIPI clock lane port 1
27	DGND	P	MIPI circuit ground (0V)
28	DATAA1P	I	MIPI data lane 1 port 1
29	DATAA1N	I	MIPI data lane 1 port 1
30	DGND	P	MIPI circuit ground (0V)
31	DATAA0P	I	MIPI data lane 0 port 1
32	DATAA0N	I	MIPI data lane 0 port 1
33	SDO	O	SPI data output (VSSD ~ VDDIO) .if don't use , keep this pin open.
34	SCS1	I	SPI enable (VSSD ~ VDDIO). if don't use , keep this pin VDDIO.

No.	Name	I/O	Description
35	RESET	I	Global Reset. Keep VDDIO during operation. Normally pull high (VSSD ~ VDDIO)
36	VCCIF	P	Power supply for MIPI, it can connect to VCORE. (1.4V ~ 1.6V)
37	VCCIF	P	Power supply for MIPI, it can connect to VCORE. (1.4V ~ 1.6V)
38	V1P2	O	Regulator output for MIPI LP mode. (1.2V)
39	TEST1	I	Connect to VDDIO
40	TEST2	I	Connect to VDDIO
41	VDDIO	P	Power supply for Image I/F input circuit (1.65V ~ 3.6V)
42	TEST3	I	Connect to GND
43	TEST4	I	NC
44	VDD	P	Power supply for LCD power circuit (2.65V ~ 3.6V)
45	VDD	P	Power supply for LCD power circuit (2.65V ~ 3.6V)
46	VCORE	O	Regulator output voltage for logic circuit (1.5V)
47	VCORE	O	Regulator output voltage for logic circuit (1.5V)
48	VGAMPL	O	Regulator low voltage for positive gamma (0.2V ~ 0.9V)
49	VGAMPH	O	Regulator high voltage for positive gamma (3.7V ~ 5.2V)
50	VGAMNL	O	Regulator low voltage for negative gamma (-0.2V ~ -0.9V)
51	VGAMNH	O	Regulator high voltage for negative gamma (-3.7V ~ -5.2V)
52	GPO2	O	General Purpose Output pin. .if don't use , keep this pin open.
53	DGND	P	MIPI circuit ground (0V)
54	CLKBP	I	MIPI clock lane port 1
55	CLKBN	I	MIPI clock lane port 1
56	DGND	P	MIPI circuit ground (0V)
57	DATAB1P	I	MIPI data lane 1 port 1
58	DATAB1N	I	MIPI data lane 1 port 1
59	DGND	P	MIPI circuit ground (0V)
60	DATAB0P	I	MIPI data lane 0 port 1
61	DATAB0N	I	MIPI data lane 0 port 1
62	AGND	P	Analog circuit ground (0V)
63	AGND	P	
64	AGND	P	
65	SCS2	I	SPI enable (VSSD ~ VDDIO) . if don't use , keep this pin VDDIO.
66	TEST5	I	Connect to GND
67	SCK	I	SPI clock (VSSD ~ VDDIO) . if don't use , keep this pin GND.
68	SDI	I	SPI data input (VSSD ~ VDDIO) . if don't use , keep this pin GND.
69	VCCN	O	Regulator output voltage for negative level shift (-3V)

No.	Name	I/O	Description
70	VCOM	O	Regulator output voltage. (-0.3V ~ -4V)
71	VCOM	O	

*Matching connector : 71FVXL-RSM1-GAN-ETF(HF) (JST)

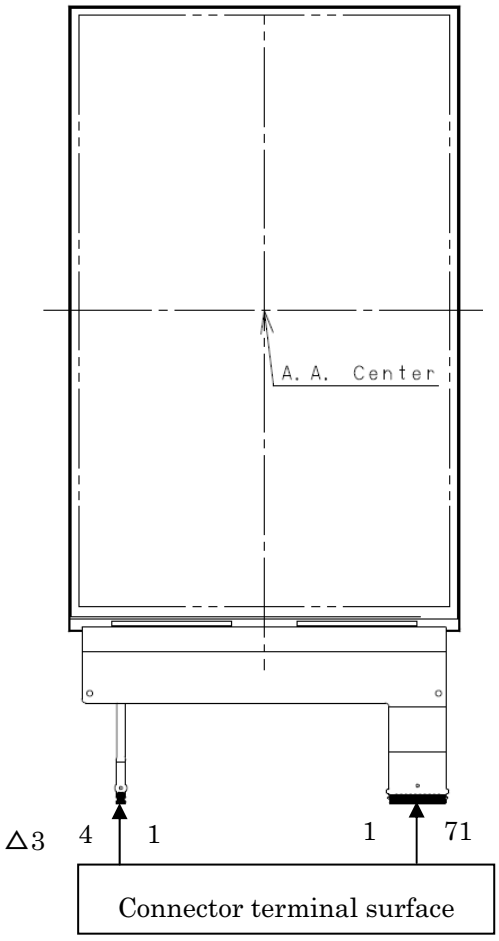


Chart 6-2 LED Input terminal Symbol

No.	Symbol	I/O	Symbolic name	No.	Symbol	I/O	Symbolic name
1	ANODE1	I	Anode	3	CATHODE2	I	Cathode
2	ANODE2	I	Anode	4	CATHODE1	I	Cathode

*Matching connector :59453-041110EDHLF (FCI)

7.Absolute Maximum Ratings

Chart 7-1 LCD Module Input Absolute Maximum Ratings △1

Parameter	Place	Symbol	Ratings	Unit	Remark
Power-supply voltage	LCD module	VDDIO	-0.3 ~ +3.96	V	Digital source
		VDD	-0.3 ~ +3.96	V	Analog source
		VSP	-0.3 ~ +6.0	V	Analog source
		VSN	-6.0 ~ +0.3	V	Analog source
Input voltage	LCD module	V_{IN}	-0.3 ~ VDDIO + 0.3 △3	V	Digital terminal input
LEDbackward voltage	B/L	VR(LED)	(5)	Vmax	
LEDforward current		I(LED)	(35)	mAmax	
LED loss		PD(LED)	(112)	mWmax	Per 1 LED
Operating temperature (panel temperature)	LCD module	Topr_lcd	-10 ~ +60	deg.	(*1)(*2)
Storage temperature	Common for every part	Tstg	-20 ~ +70	deg.	(*1)

(*1)No condensation.

(*2)Entire panel surface area.

8.Electricity Sepcification

8-1 Recommended Operating Range △1△3△4

Chart 8-1 Recommended Operating Range (Ta=-10~60deg.,GND=0V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Remark
Digital power-supply voltage	VDDIO		1.65	1.80	1.95	V	
Analog power-supply voltage	VDD		2.85	3.00	3.15	V	
Analog power-supply voltage (P)	VSP		5.30	5.50	5.70	V	
Analog power-supply voltage (N)	VSN		-5.70	-5.50	-5.30	V	
LED forward current	I(LED)	Vf=2.9V(typ) 9 Serials × 2 strings	(13.6)	(14.3)	(15.0)	mA	for each string

8-2 DC Characteristics△1

Chart 8-2-1 DC Characteristics1 △3

(Ta=-10 ~ 60deg.、VDDIO=1.65 ~ 3.6V、VDD =2.9 ~ 3.1V、VSP=5.3 ~ 5.7V、VSN=-5.7 ~ -5.3V、GND=0V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Remark
Input high level voltage	VIL1		0	-	0.2 × VDDIO	V	
input low level voltage	VIH1		0.8 × VDDIO	-	VDDIO	V	
output high level voltage	VOL1		0	-	0.2 × VDDIO	V	
output low level voltage	VOH1		0.8 × VDDIO	-	VDDIO	V	

Chart 8-2-1 DC Characteristics2 △3△6

(Ta=-10～60deg.、VDDIO=1.65～3.6V、VDD =2.9～3.1V、VSP=5.3～5.7V、VSN=-5.7～-5.3V、GND=0V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Remark
Current consumption(1)	I_{OPE1}	60Hz(*1)	-	(0.03)	(0.3)	mA	VDDIO
	I_{OPE2}	60Hz(*1)	-	(40.5)	(52)	mA	VDD
	I_{OPE3}	60Hz(*1)	-	(29)	(37.5)	mA	VSP
	I_{OPE4}	60Hz(*1)	-	(16)	(20.5)	mA	VSN
Current consumption(2)	I_{OPE1}	60Hz(*2)	-	(0.03)	(0.3)	mA	VDDIO
	I_{OPE2}	60Hz(*2)	-	(40.5)	(52)	mA	VDD
	I_{OPE3}	60Hz(*2)	-	(54)	(T.B.D.)	mA	VSP
	I_{OPE4}	60Hz(*2)	-	(40)	(T.B.D.)	mA	VSN
Current consumption(3)	I_{STBY1}	(*3)		(30)	(300)	μA	VDDIO
	I_{STBY1}	(*3)	-	(130)	(400)	μA	VDD

(*1) Horizontal gray scale pattern, VSP=5.5V、VSN=-5.5V、VDD=3V

(*2) Horizontal stripes pattern, VSP=5.5V、VSN=-5.5V、VDD=3V

(*3) Deep standby mode state, VSP=0V, VSN=0V,EXCK=0V

8-3 MIPI △1

8-3-1 DC Characteristics △3

Chart 8-3-1-1 DC Characteristics for MIPI LP mode

Parameter	Symbol	Min.	Typ	Max.	Unit	Note
Logic 1 input voltage	VIH	880	–	–	mV	
Logic 0 input voltage	VIL	0	–	550	mV	
Logic 1 output voltage	Voh	1.1	1.2	1.3	V	
Logic 0 output voltage	Vol	−50	–	50	mV	

Chart 8-3-1-2 DC Characteristics for MIPI HS mode △3

Parameter	Symbol	Min.	Typ	Max.	Unit	Note
Common-mode voltage HS Receive mode	VCMRXDC	70		330	mV	
*Differential input high threshold	VIDTH			(120)	mV	
*Differential input low threshold	VIDTL	(-120)			mV	
Single-ended input high voltage	VIHHS			460	mV	
Single-ended input low voltage	VILHS	-40			mV	
Differential input impedance	ZID	80	100	125	Ω	
HS transmit differential voltage (VDP-VDN)	|VOD|	140	200	270	mV	

Note: VIDTH and VIDTL only for reference, related to power and ground noise, this spec need to check on panel performance to fine tune

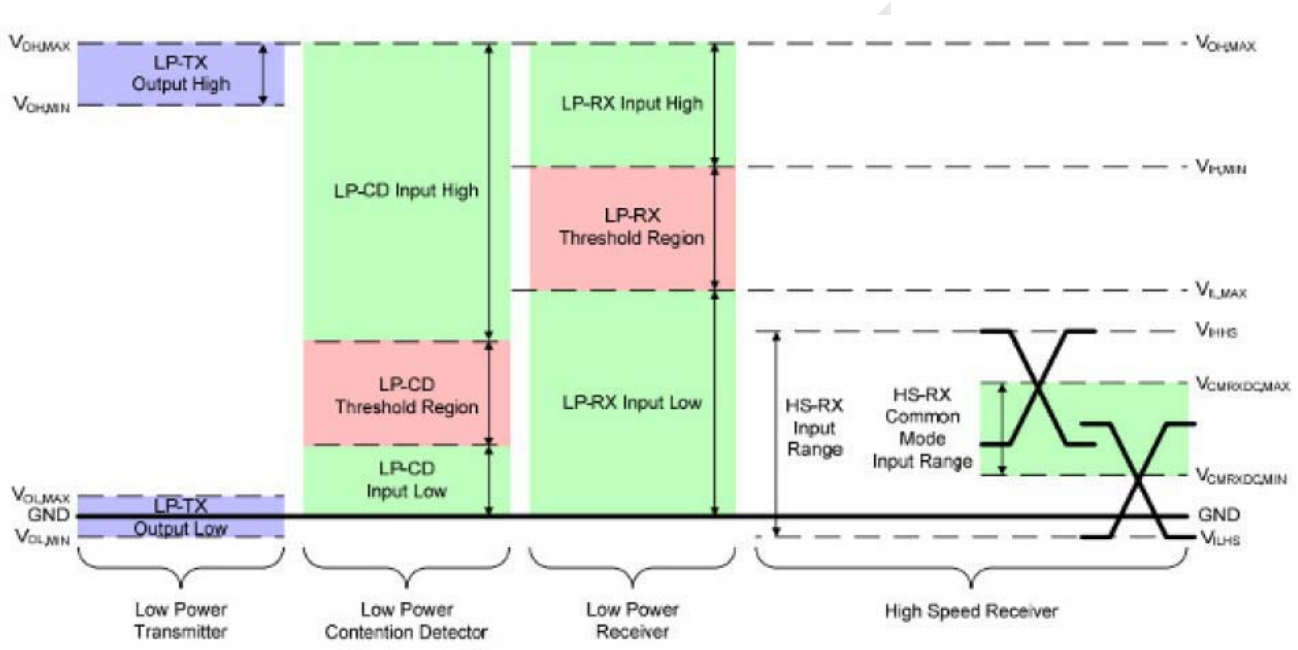


Fig.8-3-1

8-3-2 AC Characteristics

Chart 8-3-2 AC Characteristics △3

(Ta=-10～60deg.、VDDIO=1.65～3.6V、VDD =2.9～3.1V、VSP=5.3～5.7V、VSN=-5.7～-5.3V、GND=0V)

Description	Symbol	Min.	Typ	Max.	Unit	Note
30%-85% rise time and fall time	T_{REOT}			35	ns	
Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.	$T_{CLK-MISS}$			60	ns	
Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of $T_{CLK-TRAIL}$.	$T_{CLK-POST}$*1	60 ns + 52*UI (For DCS)			ns	
Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	$T_{CLK-PRE}$	8			ns	
Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of $T_{CLK-PRE}$.	$T_{CLK-SETTLE}$	95		300	ns	
Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $VIL_{,MAX}$.	$T_{CLK-TERM-EN}$	Time for Dn to reach $V_{TERM-EN}$		38	ns	
Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $T_{HSPREPARE}$.	$T_{HS-SETTLE}$	85 ns + 6*UI		145 ns + 10*UI	ns	
Time from start of THS-TRAIL or TCLK-TRAIL period to start of LP-11 state	T_{EOT}			105ns+48*UI		
time to drive LP-11 after HS burst	$T_{HS-EXIT(1)}$	100			ns	
Time to drive LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40ns + 4*UI		85ns+6*UI		
$T_{HS-PREPARE}$ + Time to drive HS-0 before the Sync sequence	$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	145ns + 10*UI			ns	
Time-out at RX to ignore transition period of EoT	$T_{HS-SKIP}$	40		55ns+4*UI	ns	
Time to drive flipped differential state after last payload data bit of a HS transmission burst	$T_{HS-TRAIL}$	60			ns	
Length of any Low-Power state period	T_{LPX}	50			ns	
Ratio of $T_{LPX(MASTER)}$/$T_{LPS(SLAVE)}$ between Master and Slave side	Ratio T_{LPX}	2/3		3/2		
Time to drive LP-00 by new TX	T_{TA-GET}	$5*T_{LPX}$			ns	
Time to drive LP-00 after Turnaround Request	T_{TA-GO}	$4*T_{LPX}$			ns	
Time-out before new TX side starts driving	$T_{TA-SURE}$	T_{LPX}		$2*T_{LPX}$	ns	

Note1: For image transmission:

$T_{CLK-POST}$ min value =164 when MIPI max frequency per lane = 0.53Gbps.

$T_{CLK-POST}$ min value =112 when MIPI max frequency per lane = 1Gbps

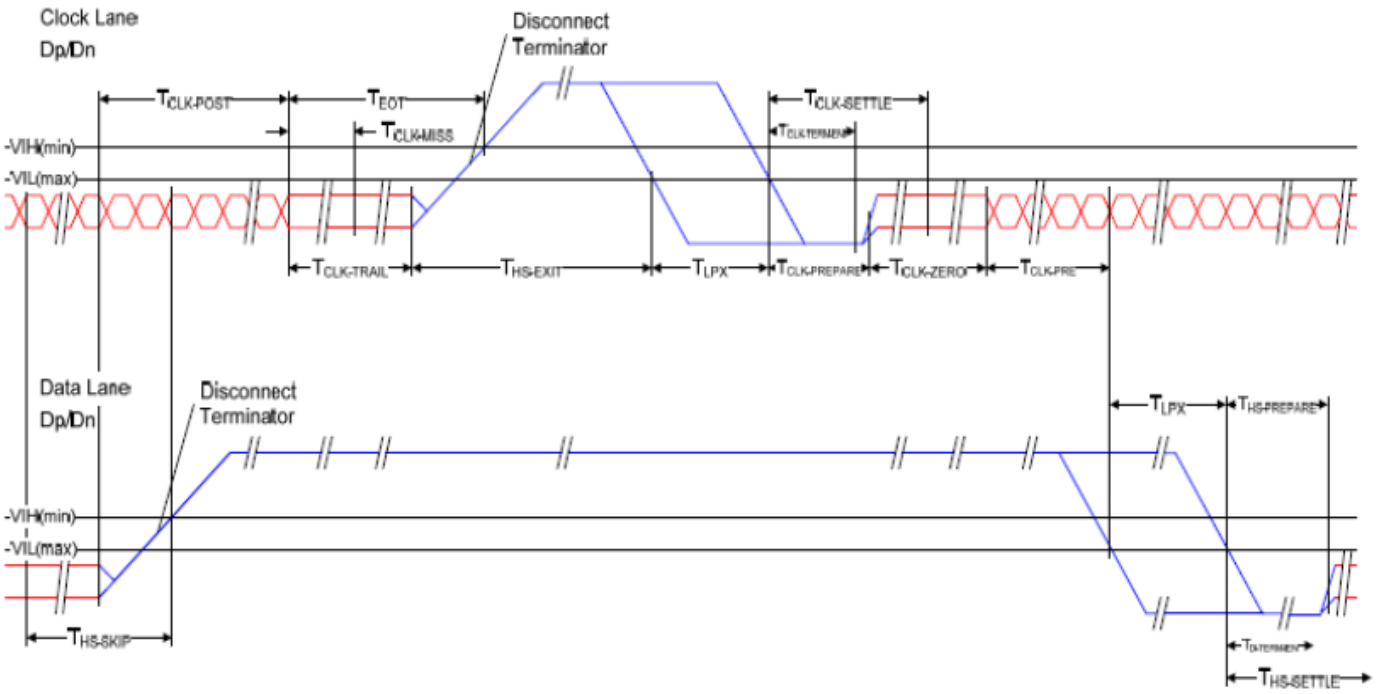


Fig.8-3-2

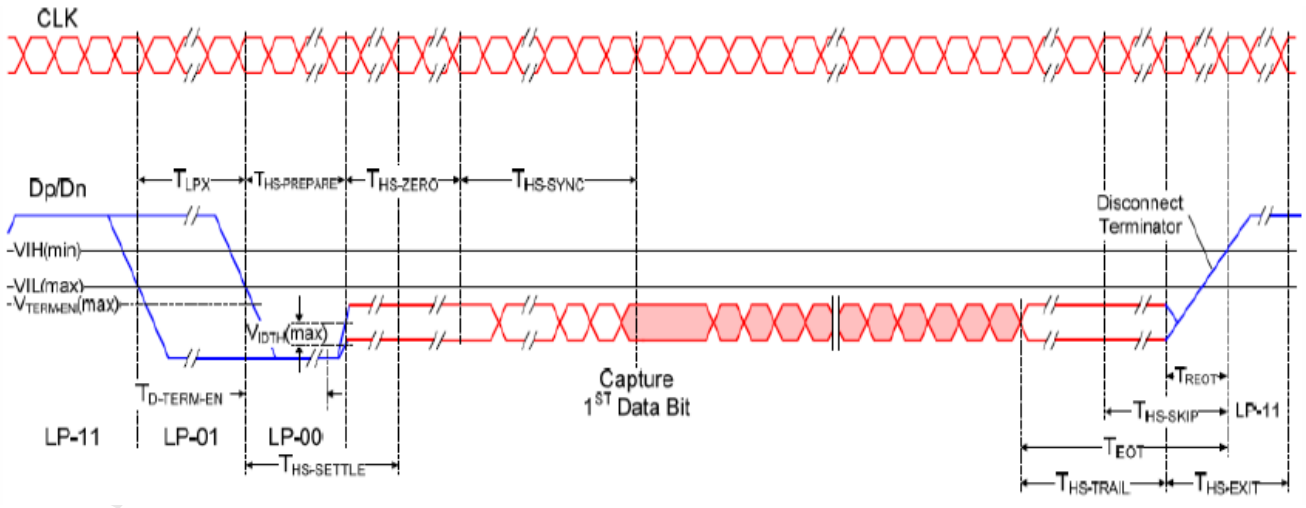


Fig.8-3-3

8-3-3 MIPI Data-Clock Timing Specification△３

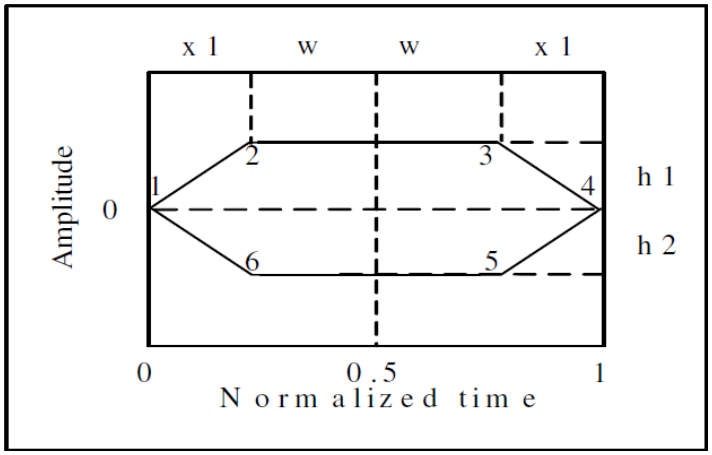


Fig. 8-3-4

Chart 8-3-3

Symbol	Time(UI)	Voltage
1	0	0
2	0.2	+70mV(min)
3	0.8	+70mV(min)
4	1	0
5	0.8	−70mV(min)
6	0.2	−70mV(min)

Chart 8-3-4

Symbol	Unit
× 1	0.2UI
W	0.3UI
h1/h2	+/− 70mV (min)

8-4 Reset Timing Characteristics

Chart 8-4-1 Reset Timing Characteristics

（Test condition: VDDIO=1.65V～3.6V, Ta=−30℃ ～+85℃）

Item	Symbol	Condition	Min.	Typ	Max.	Unit	Note
Reset “L” period	trst	—	20	-	-	μs	

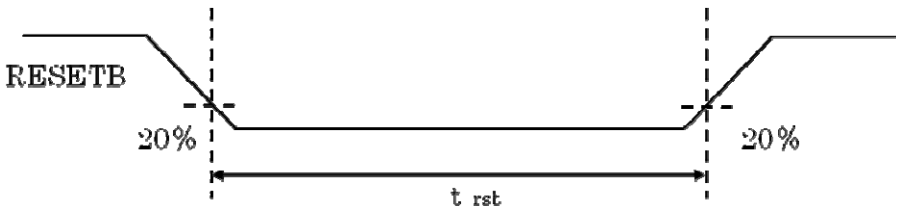
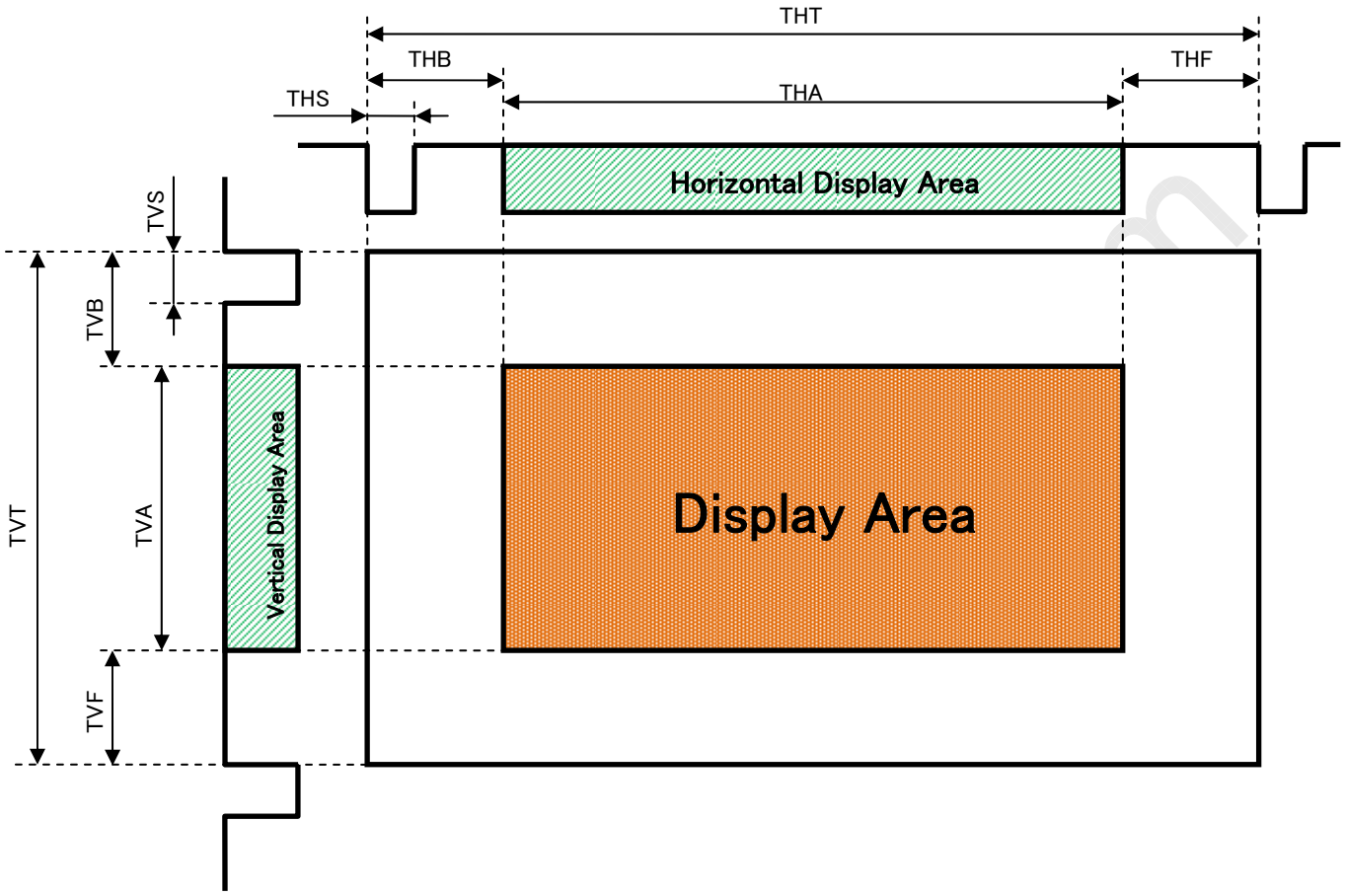


Fig. 8-4-1

8-5 MIPI video input timing △6



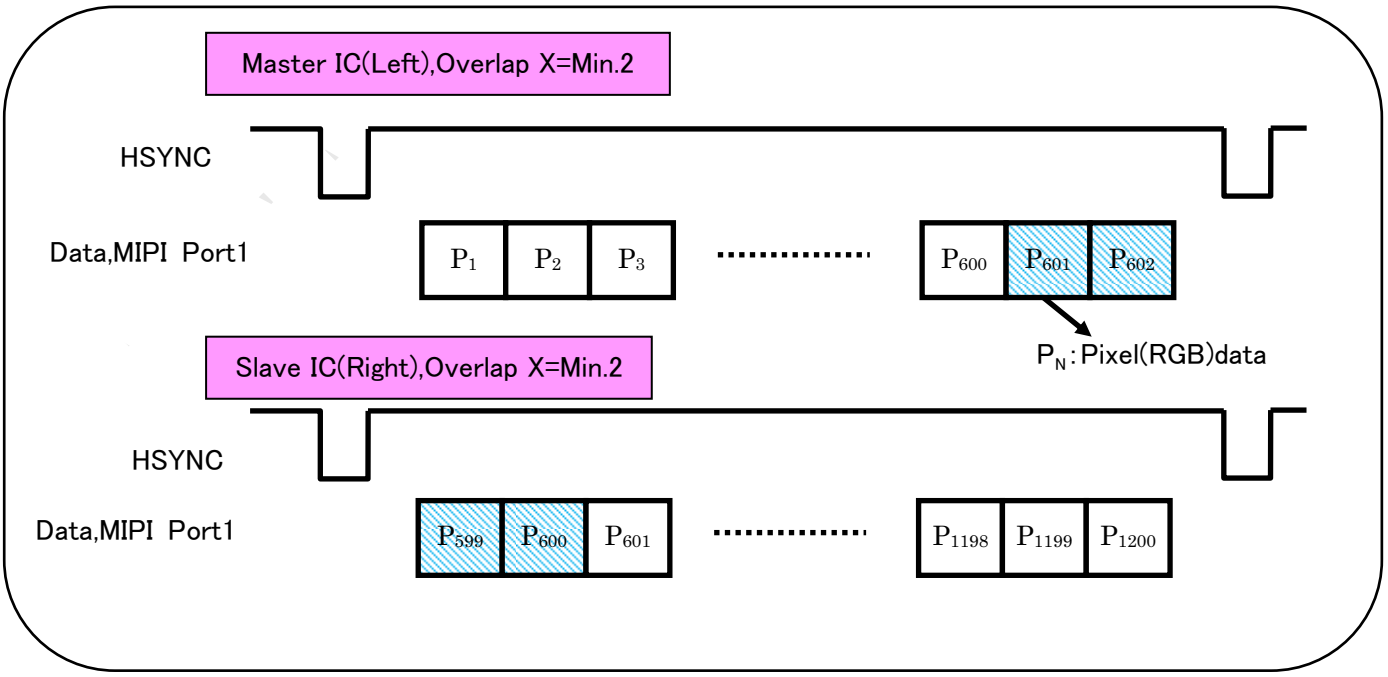


Fig. 8-5-1

Chart 8-5-1 Input Timing △6

Input Timing	Symbol	Min.	Typ.	Max.	Unit
Vertical Frequency	-		60	(61)	Hz
Vertical Total	TVT		1940		THT
Vertical Synchronization	TVS		2		THT
Vertical Back Porch	TVB	8	8	8	THT
Vertical Address	TVA	1920	1920	1920	THT
Vertical Front Porch	TVF	12	12		THT
Horizontal Total	THT	(682)	704		PCLKCYC
Horizontal Synchronization	THS	10	20		PCLKCYC
Horizontal Back Porch	THB	10	20		PCLKCYC
Horizontal Address	THA	602	602	602	PCLKCYC
Horizontal Front Porch	THF	(70)	82		PCLKCYC
Horizontal Overlap Pixel	X	2	2	2	PCLKCYC
MIPI Port 1 & 2 Skew	SKEW	-1	0	1	THT
PCLK Frequency	-	(79.385)	81.946		MHz

※ Above timing is for each LINK.

9. Power Sequence

9-1 Power On Sequence △3△6

Chart 9-1 Power On Sequence

	Function	Value	Note
	VDDIOPowerON	PowerON (VDDIO)	
	VDDPowerON	PowerON (VDD)	
	VSPPowerON	PowerON (VSP)	
	VSNPowerON	PowerON (VSN)	
	Wait	Wait	
	Reset control	Reset (L→H)	

△4 Please input the sequence of ① or ② for both LINK.

	Function	Register	Value	Write Data type	read Data type	Note
①	Switch to Page 0	B0h	00h	23h or 15h	24h or 06h	
	MIPI Video data input start	MIPI Video data input start				
	Sleep Out command	11h		05h	–	Sleep Out
	Wait	Wait				
	Setting command					If need to change setting, Please send command.
	Wait	Wait				
	Display On command	29h		05h	–	Display On
②	Display On command	29h		05h	–	※Display On and Sleep Out may be interchanged.
	Sleep Out command	11h		05h	–	
	Setting command					If need to change setting, Please send command.
	MIPI Video data input start	MIPI Video data input start				※Video data is Sleep Out command input Enter beginning after 60ms or less.

9-2 Power Off Sequence △3

Chart 9-2 Power Off Sequence

	Function	Register	Value	Write Data type	read Data type	Note
	Display OFF command	28h		05h	–	
	Wait	Wait	1Frame			
	Sleep In Command	10h		05h	–	
	Wait	Wait	6Frame			
	MIPI Video dataOFF	MIPI Video data OFF				
	Reset Control	Reset (H→L)				
	VSN Power OFF	PowerOFF (VSN)				
	VSP Power OFF	PowerOFF (VSP)				
	VDD Power OFF	PowerOFF (VDD)				
	VDDIO Power OFF	PowerOFF (VDDIO)				

9-3 ON and Off Power Sequence △4

9-3-1 ON Sequence

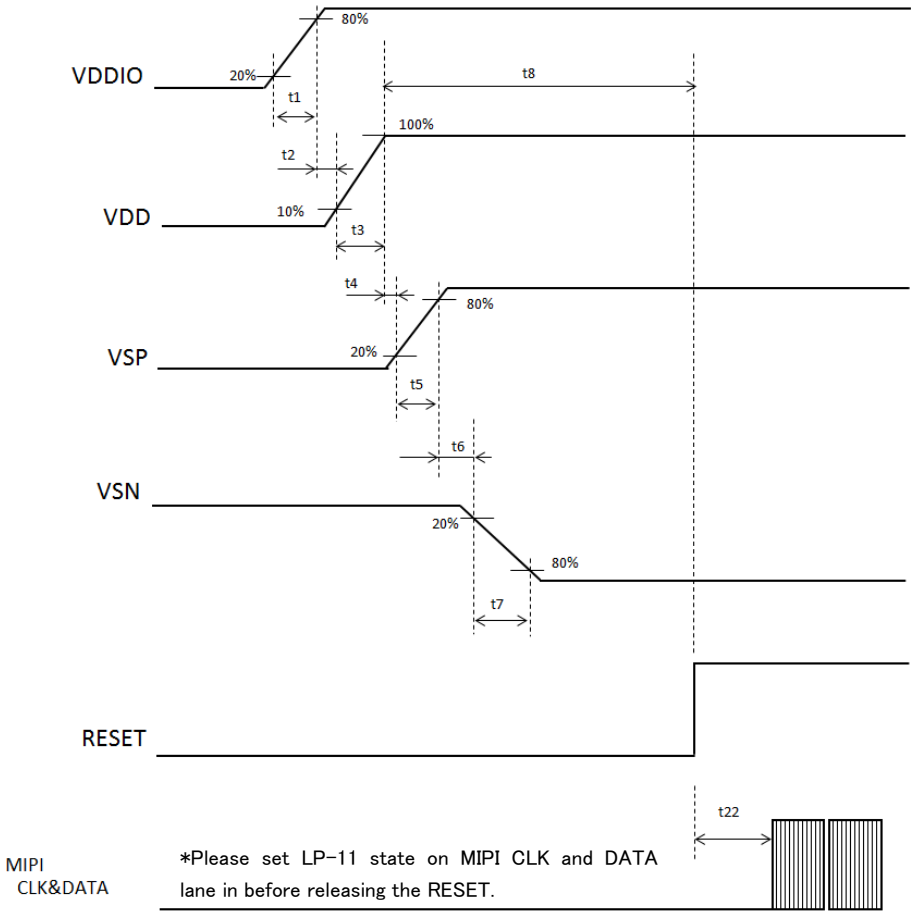


Fig.9-3-1 ON Sequence

9-3-2 OFF Sequence △4

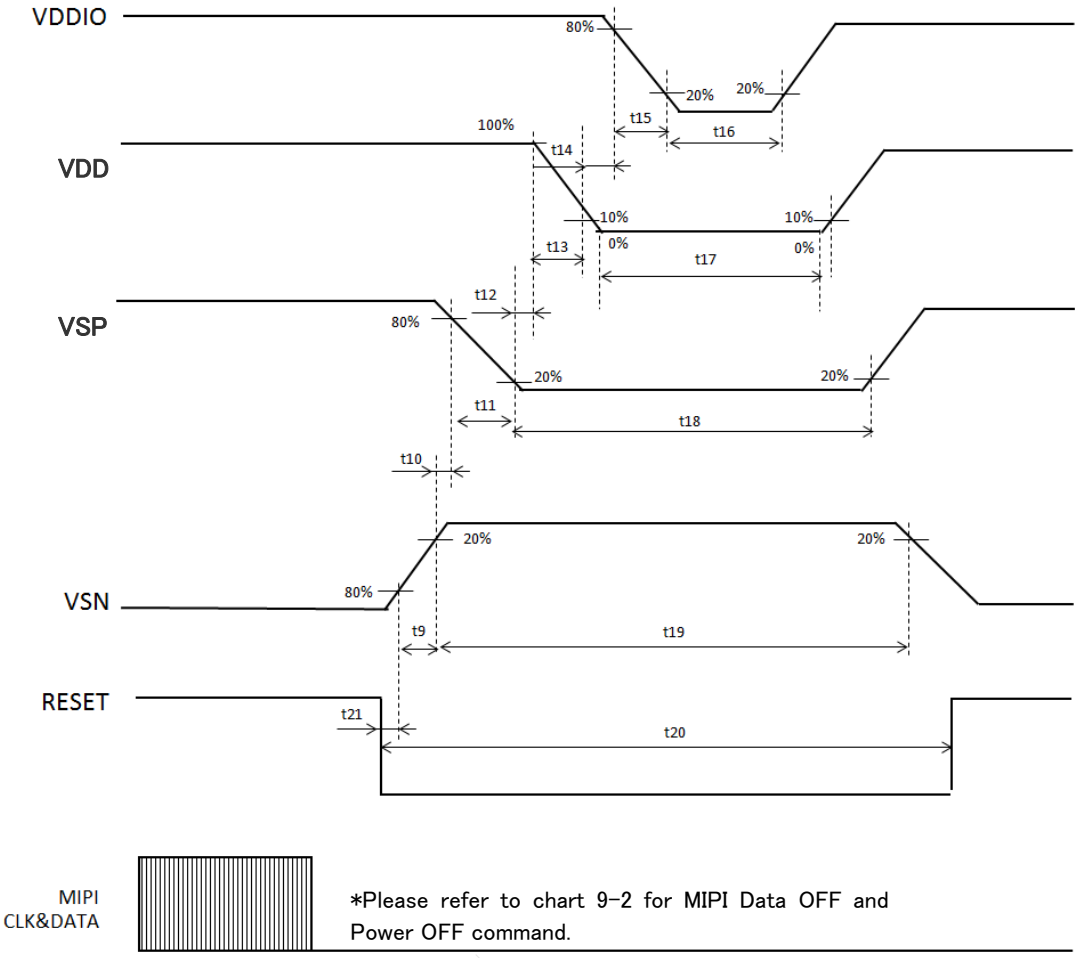


Fig.9-3-2 OFF Sequence

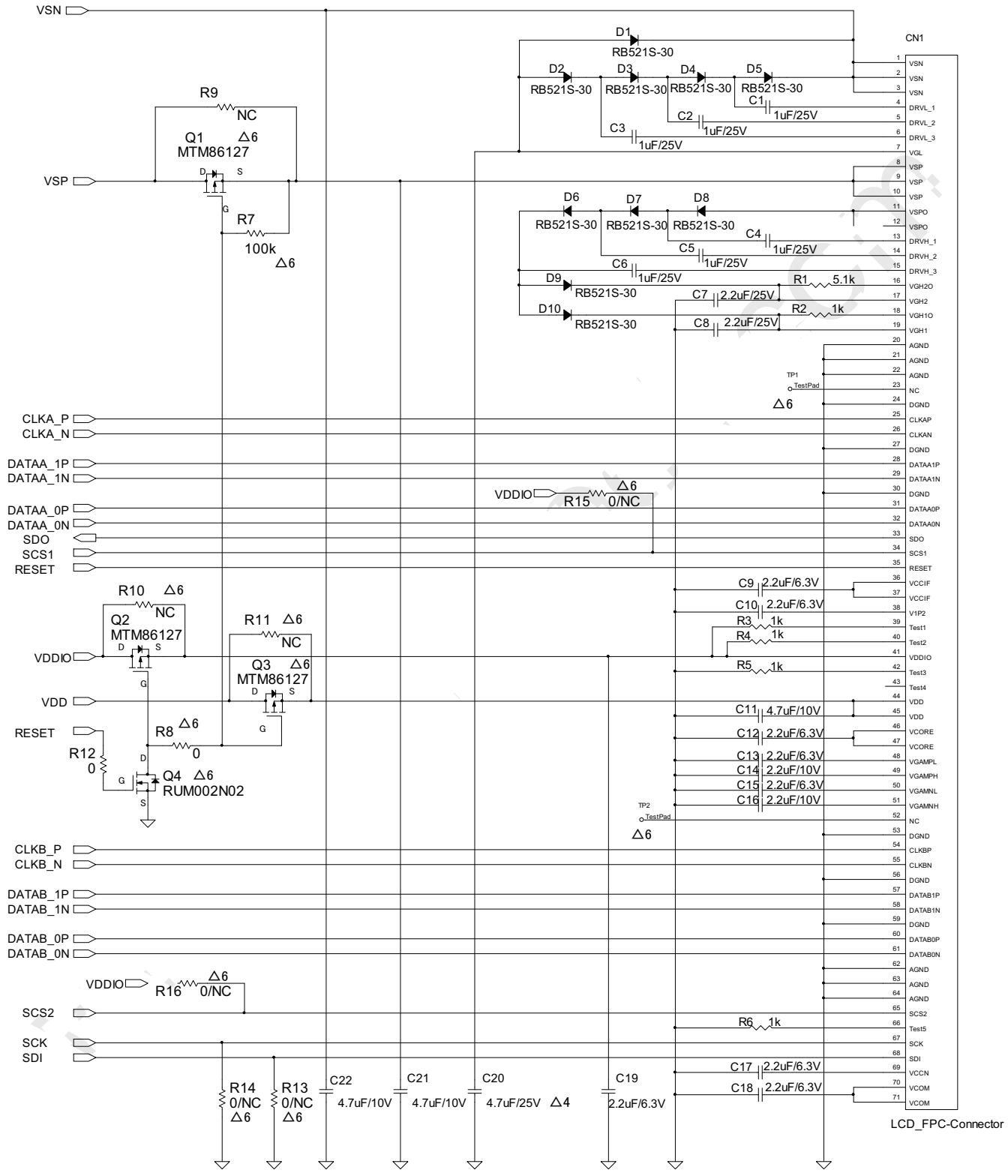
Chart 9-3 Power Sequence △5

Item		Min	Typ	Max	Unit
VDDIO 20%→80%	t1	0.2	1	–	ms
VDDIO ↑ (80%) → VDD ↑ (10%)	t2	0	1	–	ms
VDD 10%→100%	t3	0.2	1	80	ms
VDD ↑ (100%) → VSP ↑ (20%)	t4	0.2	1	–	ms
VSP 20%→80%	t5	0.2	1	–	ms
VSP ↑ (80%) → VSN ↓ (20%)	t6	0	1	–	ms
VSN 20%→80%	t7	0.2	1	–	ms
VDD ↑ (100%) → RESETB ↑	t8	1	1	–	ms
VSN 80%→20%	t9	0.2	1	–	ms
VSN ↑ (20%) → VSP ↓ (80%)	t10	0	1	–	ms
VSP 80%→20%	t11	0.2	1	–	ms
VSP ↓ (20%) → VDD ↓ (100%)	t12	0.2	1	–	ms

Item		Min	Typ	Max	Unit
VDD 100%→10%	t13	0.2	1	–	ms
VDD ↓ (10%) → VDDIO ↓ (80%)	t14	0	1	–	ms
VDDIO 80%→20%	t15	0.2	1	–	ms
VDDIO ↓ 20%→VDDIO ↑ 20%	t16	0.2	–	–	ms
VDD ↓ 0%→VDD ↑ 0%	t17	20	–	–	ms
VSP ↓ 20%→VSP ↑ 20%	t18	0.2	–	–	ms
VSN ↑ 20%→VSN ↓ 20%	t19	0.2	–	–	ms
RESET ↓ →RESET ↑	t20	(*) 1	–	–	ms
RESET ↓ →VSN ↑ 80%	t21	0.2	–	–	ms
RESETB ↑ →Command Input	t22	2	–	–	ms

(*) If Reset = Lo → HI of the periods indicated, Wait of MIN140ms is needed.

10. External Circuitry △3△4△6



As for the circuit and components are recommended.

When using this product, evaluate the integrity of your system to design.

(condenser pressure enabled larger than above list value)

If don't use SPI I/F, keep SCS1 & SCS2 pin's voltage to VDDIO voltage and SCK & SDI pin's voltage to GND.

Fig.9-1 External Circuitry(recommended)

11.Optical Specification △3△5

11-1 Optical Characteristics

Chart 11-1-1 Optical Characteristics (Ta = 25deg., B/L-LED impressed current IF=14.3mA)

Parameter		Symbol	Condition	Min.	Typ.	Max	Unit	Remark
Brightness			θ=0°	T.B.D	400	-	cd/m^2	[Note 11-4]
Brightness uniformity			θ=0°	T.B.D	(80)		%	[Note 11-5]
Contrast ratio		CR	θ=0°	(1000)	(2000)	-	-	[Note 11-2]
Viewing angle range		θ11	CR>10	T.B.D	80	-	angle	[Note 11-1]
		θ12		T.B.D	80	-		
		θ21		T.B.D	80	-		
		θ22		T.B.D	80	-		
Response time	Start-up time	τr	θ=0°	-	(9)	(20)	ms	[Note 11-3]
	Fall time	τd		-	(13)	(30)		
Chromaticity	white	Wx	θ=0°	-	(0.310)	-	-	[Note 11-4]
		Wy		-	(0.321)	-		
NTSC ratio (x,y)			θ=0°	-	50	-	%	[Note 11-4]

*※ The measurement shall be taken 30 minutes after lighting the module at the following rating:

Condition: PWM Duty = 100%

The optical characteristics shall be measured in a dark room or equivalent. (Refer to Fig.11-1 and Fig.11-2)

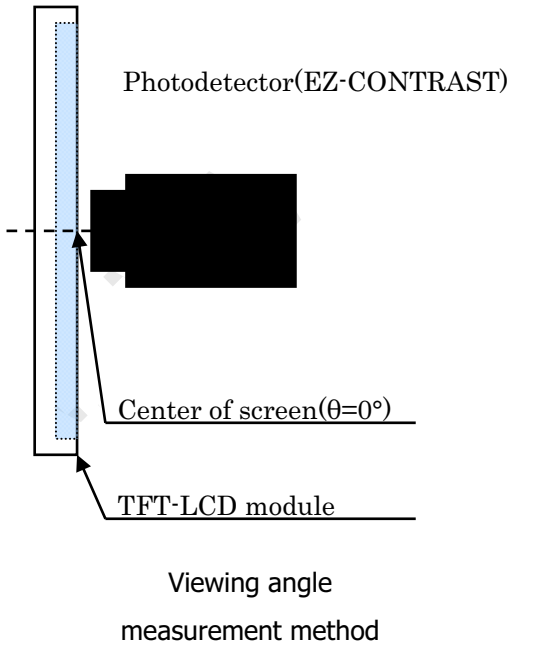


Fig11-1 Photodetector(EZ-CONTRAST)

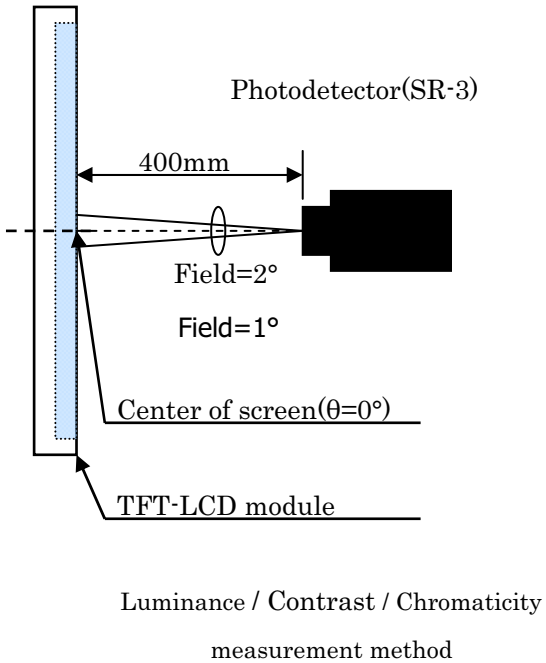


Fig11-2 Photodetector(SR-3)

[Note 11-1] Viewing angle range is defined as Fig10-3.

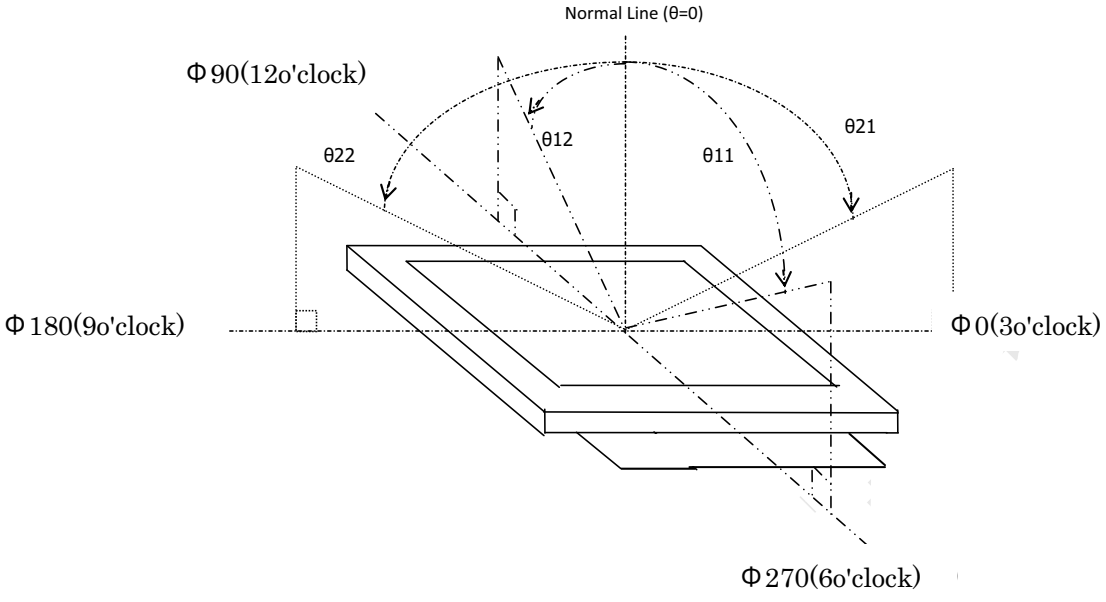


Fig11-3 Viewing angle range

[Note 11-2] Contrast ratio is defined as follows:

$$\text{Contrast ratio(CR)} = \frac{\text{Photo detector output with LCD being "white(GS255)"}}{\text{Photo detector output with LCD being "black(GS0)"}}$$

[Note 11-3] Response time is defined as follows:

Response time is obtained by measuring the transition time of photo detector output, when input signals are applied so as to make the area "black" to and from "white".

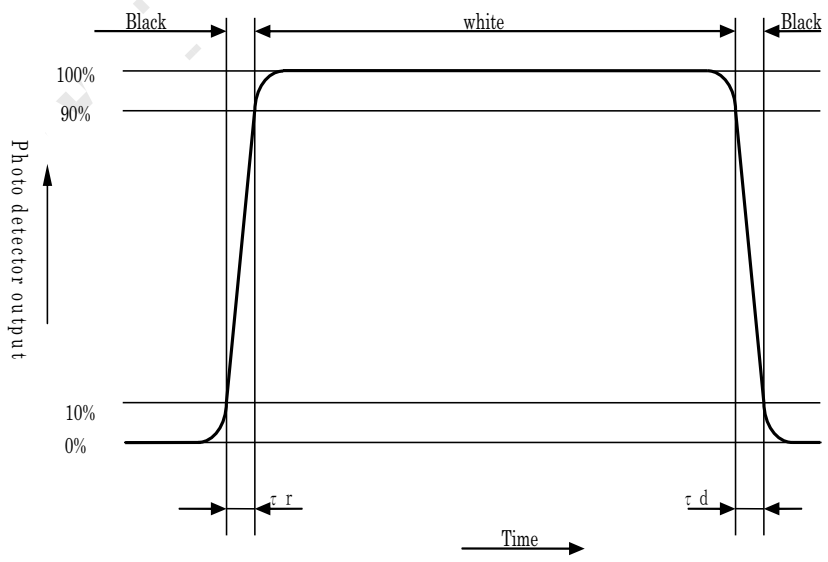


Fig11-4 Response time

[Note 11-4] Measured on the center area of the panel at a viewing cone 1-degree by luminancemeter SR-3.(After 30 minutes operation)

[Note 11-5] Definition of Uniformity

$$Uniformity = \frac{\text{Minimum Brightness}}{\text{Maximum Brightness}} \times 100\,(\%)$$

The brightness should be measured on the 9-point as shown in the figure below.

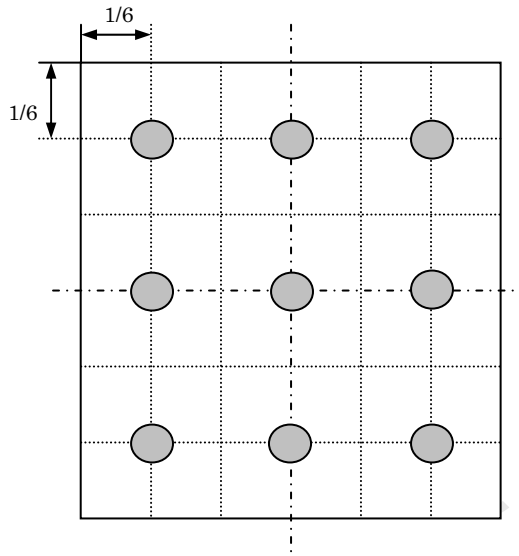


Fig11-5 Measurement of Uniformity

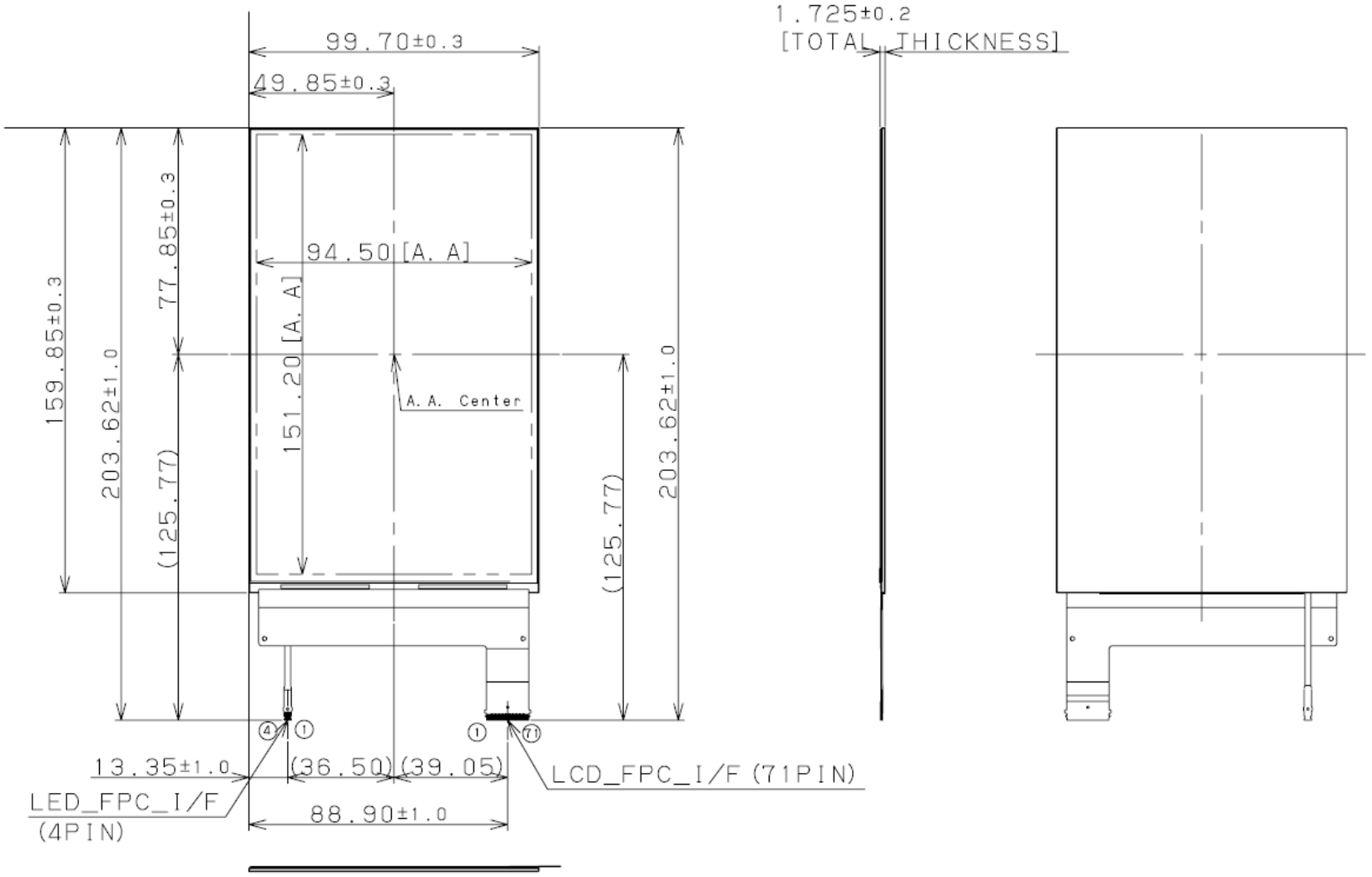
[Note11-6] The time at which the luminance of LED is diminished to half of the initial luminance. LED is to be operated with nothing but itself alone.

12. Reliability Test Items △3

Chart 12-1

No.	Test items	Test conditions
1	High temperature storage test	T.B.D.
2	Low temperature storage test	
3	High temperature operation test	
4	Low temperature operation test	
5	High temperature and high humidity operation test	
6	Heat shock test	

Ta = Ambient temperature Tp=Panel Surface temperature



NOTE
・GENERAL TOLERANCE IS ±0.5.
・WARP OR DEFORMATION OF MODULE IS EXCLUDED.

Fig. 5-1 Outline Dimensions △3

△6
Protective film is attached on the surface of LCD panel to prevent scratches or other damages. When removing this protective film, remove it slowly under proper anti-ESD control such as ion blower.