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SeeYA 0.72inch Micro-OLED（1920×1200RGB）

Specification

Model Name：SY072WCM06

Prepared by	Checked by	Approved by
Hu Boyu	Xu Zhigang	Tong Zheng

Customer approved by	
Title	
Name	
Date	

Revision

Version	Date	Description
V0.0	2022.8.23	Initial release
V0.1	2022.9.9	Correct pin description, correct module Diagram pin list.
V0.2	2022.10.18	Update pin description, Power Sequence.
V0.3	2023.1.29	Update the color coordinate of White, Green and Blue, power consumption value.
V0.4	2023.7.20	Correct Pin description，Update application Circuit.
V0.5	2023.7.25	Correct Pin description，Update application Circuit.
V1.0	2023.9.11	Add inspection criteria, update to V1.0

Contents

1. General Description

This display is a 0.72inch diagonal, 1920(RGB) × 1200 dots active-matrix color OLED panel module based on single-crystal silicon transistors. This panel integrates panel driver and logic driver, and realizes small size, light weight, low power consumption and high resolution.
Applications: View finders, Head mounted displays, etc.

- 1920 x 1200 Real RGB Resolution
- Frame rate: 1920 x 1200 up to 70Hz
- Normal operation supports full color mode: 16.7M colors (24-bit 8(R):8(G):8(B))
- Interface

  -- MIPI + I2C

  -- MIPI DSI (Display Serial Interface) with 4 lanes, 1.2Gbps/Lane

  -- Support MIPI DSI Video mode: non-burst mode with sync pulse and non-burst mode with sync event

  -- Support Multi resolution:1920x1200(16:10)，1920x1080(16:9)， 1600x1200(4:3)，1280x1024(5:4)，1280x720(16:9)，1024x768(4:3)
- Vertical/Horizontal scan direction control
- Orbit supported
- Wide range Brightness adjustment
- Normal/Rolling/Dimming mode
- 3 Power input: ELVDD(5.5v), ELVSS(-5v), VDDI(1.8v)

2. General Feature

Item	Specification
Resolution	1920(H) x 1200 (V)
Number of dots	6.912M (1920x1200x3)
Pixel Size	8.1μm x 8.1μm
Pixel Arrangement	RGB π type
Useable Display Area	15.552mm x 9.72mm / 0.72" diagonal
Luminance	2000
Contrast Ratio	100,000:1 typical
Uniformity	> 85%
Power Consumption	800mW
Gray Levels	256
Interface	MIPI (1port D-PHY)
Frame Rate	50Hz~70Hz
Weight	TBD
Operating Temperature	-20°C to +70°C
Storage Temperature	-40°C to +80°C

3. Optical Specification

Tpanel=30℃	Parameter	Min.	Typ.	Max.	Unit
Brightness		1600	2000	2400	cd/m2
CR	white to Black Contrast Ratio	50,000:1	100,000:1		
Uniformity	End to end large-area uniformity	85			%
CIE Red	CIE-x	0.620	0.650	0.680	
	CIE-y	0.300	0.330	0.360	
CIE Green	CIE-x	0.195	0.230	0.265	
	CIE-y	0.660	0.690	0.720	
CIE Blue	CIE-x	0.120	0.150	0.180	
	CIE-y	0.030	0.060	0.090	
CIE White	CIE-x	0.285	0.300	0.315	
	CIE-y	0.300	0.315	0.330	
DCI-P3			90%		
Frame rate		50		70	HZ
Power consumption			800	1000	mW

Note1: If there is no specified, the specification of optical is specified at 30 degrees Celsius.

Note2: Definition of optical measurement system.

The optical characteristics should be measured in dark room. Brightness is measured as peak luminance at full white pattern (Gray level=255 with 8bits color depth);

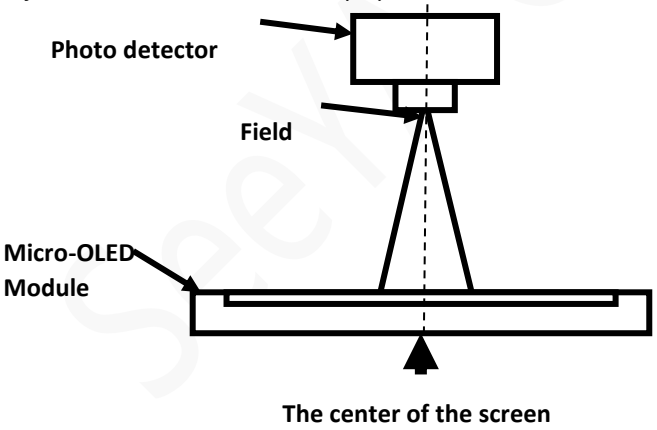


Fig.1

Note3: Definition of Uniformity at gray level255(8bits color depth) and 100%duty emission.

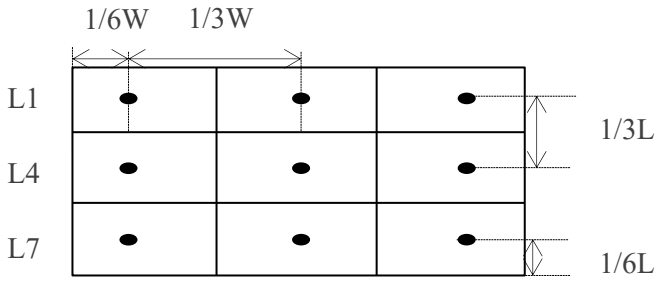
Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity (U) = Lmin/ Lmax

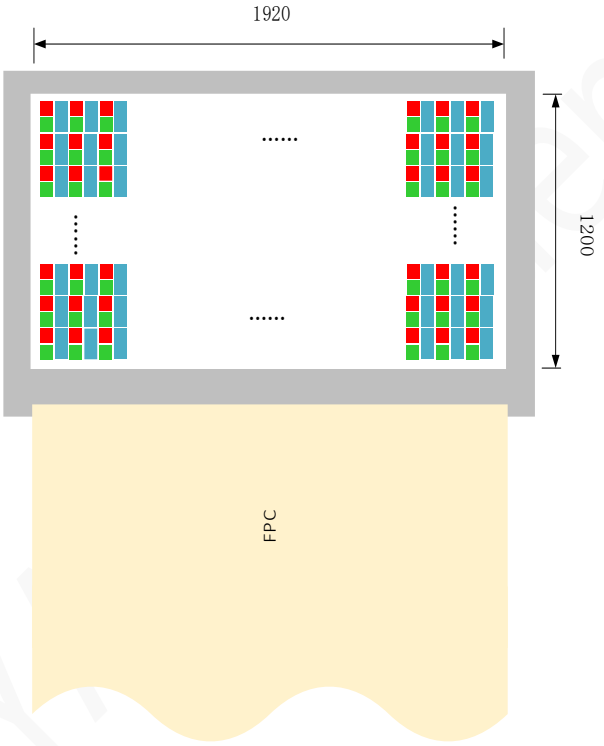
L-------Active area length; W----- Active area width

Lmax: The measured maximum luminance of all measurement position.

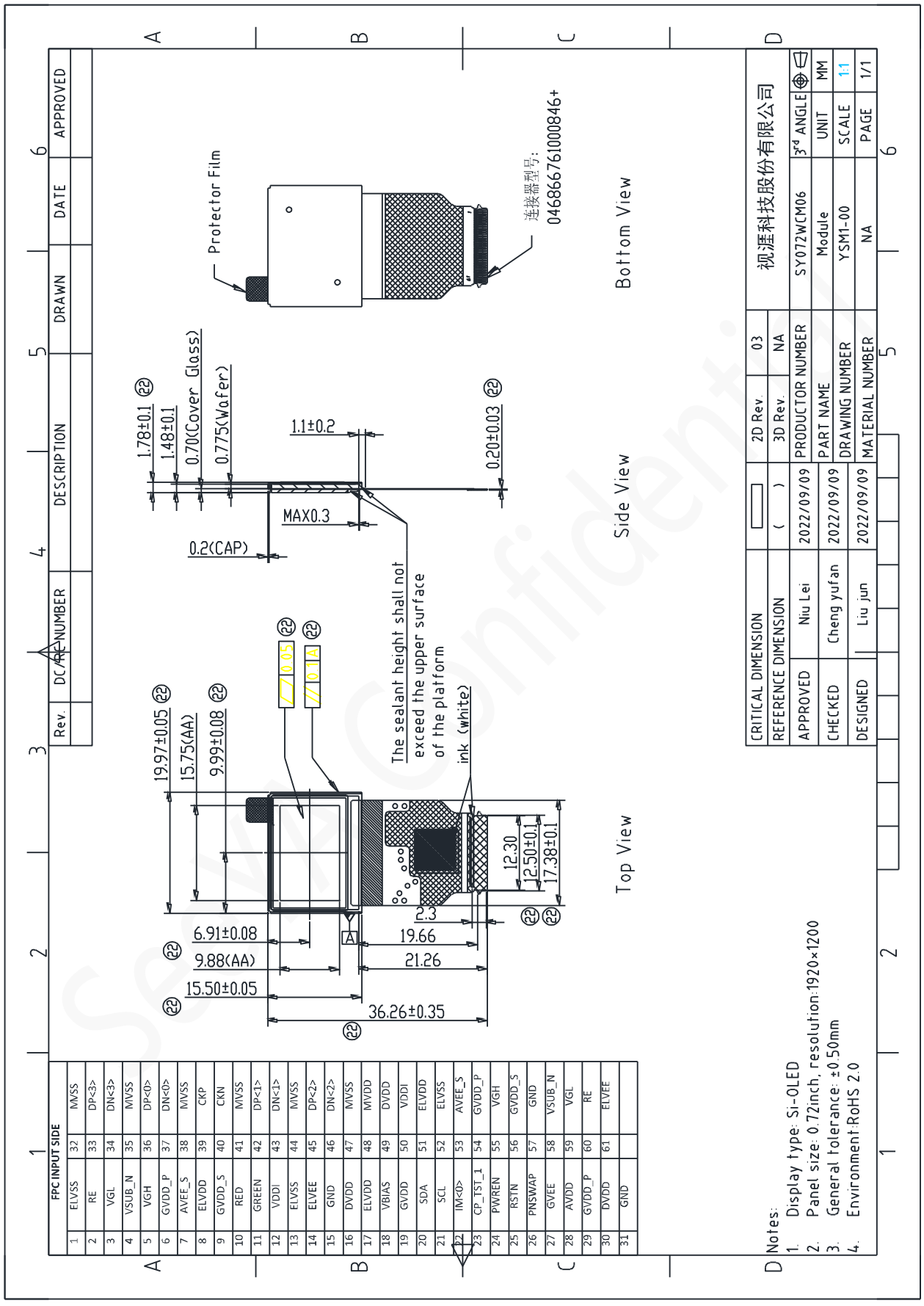
Lmin: The measured minimum luminance of all measurement position.



4. Pixel Array



6. Module Diagram



7. Pin Description

7.1 Pin Description

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>1</td><td>ELVSS</td><td>Power</td><td>Power supply for OLED cell. Connect a capacitor for stabilization. Connect a Schottky diode to GND． Connect all ELVSS together.</td></tr>
<tr><td>2</td><td>RE</td><td>Output</td><td>OLED Reset Power supply. Connect a capacitor for stabilization. Connect a Schottky diode to GND． Connect all RE together.</td></tr>
<tr><td>3</td><td>VGL</td><td>Output</td><td>Regulator for GOA. Connect a capacitor for stabilization. Connect a Schottky diode to GND． Connect all VGL together.</td></tr>
<tr><td>4</td><td>VSUB_N</td><td>Output</td><td>Regulator for pixel NMOS sub. Connect a capacitor for stabilization. Connect a Schottky diode to GND．</td></tr>
<tr><td>5</td><td>VGH</td><td>Output</td><td>Regulator for GOA. Connect a capacitor for stabilization. Connect all VGH together.</td></tr>
<tr><td>6</td><td>GVDD_P</td><td>Output</td><td>Regulator output for Pixel analog system positive power. Connect a capacitor for stabilization. Connect all GVDD_P together.</td></tr>
<tr><td>7</td><td>AVEE_S</td><td>Output</td><td>Regulator for source. Connect a capacitor for stabilization. Connect a Schottky diode to GND． Connect all AVEE_S together.</td></tr>
<tr><td>8</td><td>ELVDD</td><td>Power</td><td>Power supply for OLED cell. Connect a capacitor for stabilization. Connect all ELVDD together.</td></tr>
<tr><td>9</td><td>GVDD_S</td><td>Output</td><td>Regulator output for source analog system positive power. Connect a capacitor for stabilization. Connect all GVDD_S together.</td></tr>
<tr><td>10</td><td>RED</td><td>Output</td><td>Test pin, please Open.</td></tr>
<tr><td>11</td><td>GREEN</td><td>Output</td><td>Test pin, please Open.</td></tr>
<tr><td>12</td><td>VDDI</td><td>Power</td><td>Power supply for D-PHY, DSI and digital part. Connect a capacitor for stabilization. Connect all VDDI together.</td></tr>
<tr><td>13</td><td>ELVSS</td><td>Power</td><td>Power supply for OLED cell. Connect a Schottky diode to GND． Connect all ELVSS together.</td></tr>
<tr><td>14</td><td>ELVEE</td><td>Power</td><td>Power supply for OLED cell. Connect a capacitor for stabilization. Connect a Schottky diode to GND． Connect all ELVEE together.</td></tr>
<tr><td>15</td><td>GND</td><td>Power</td><td>System GND for internal digital/analog system.</td></tr>
<tr><td>16</td><td>DVDD</td><td>Output</td><td>Regulator output for logic digital system positive power. Connect a capacitor for stabilization. Connect all DVDD together.</td></tr>
<tr><td>17</td><td>ELVDD</td><td>Power</td><td>Power supply for OLED cell. Connect a capacitor for stabilization. Connect all ELVDD together.</td></tr>
<tr><td>18</td><td>VBIAS</td><td>Output</td><td>Connect a capacitor for stabilization.</td></tr>
<tr><td>19</td><td>GVDD</td><td>Output</td><td>Regulator output for GAMMA analog system positive power. Connect a capacitor for stabilization.</td></tr>
<tr><td>20</td><td>SDA/LSW<0></td><td>Input/Output</td><td>IM<0>=0, data input/output for I2C;
IM<0>=1, used as LSW<0></td></tr>
<tr><td>21</td><td>SCL/LSW<1></td><td>Input</td><td>IM<0>=0, serial clock for I2C;
IM<0>=1, used as LSW<1></td></tr>
<tr><td>22</td><td>IM<0></td><td>Input</td><td>Use to select the interface type
<table>
<tr><td>IM<0></td><td>Command</td><td>Display Data</td></tr>
<tr><td>0V</td><td>I2C</td><td>MIPI</td></tr>
<tr><td>1.8V</td><td>MIPI</td><td>MIPI</td></tr>
</table></td></tr>
<tr><td>23</td><td>CP_TST_1</td><td>Output</td><td>Test pin for debug signal.</td></tr>
<tr><td>24</td><td>PWREN</td><td>Output</td><td>Keep it open.</td></tr>
<tr><td>25</td><td>RSTN</td><td>Input</td><td>This signal will reset the device and must be applied to properly Initialize the chip. Signal is active low.</td></tr>
<tr><td>26</td><td>PNSWAP</td><td>Input</td><td>When use MIPI interface, it is used as MIPI lane P/N SWAP.
<table>
<tr><th>Pin Name</th><th>DP2</th><th>DN2</th><th>DP1</th><th>DN1</th><th>CKP</th><th>CKN</th><th>DP0</th><th>DN0</th><th>DP3</th><th>DN3</th></tr>
<tr><td>LSW<1:0>=00, PSW=1</td><td>D3+</td><td>D3-</td><td>D2+</td><td>D2-</td><td>CLK+</td><td>CLK-</td><td>D1+</td><td>D1-</td><td>D0+</td><td>D0-</td></tr>
<tr><td>LSW<1:0>=00, PSW=0</td><td>D3-</td><td>D3+</td><td>D2-</td><td>D2+</td><td>CLK-</td><td>CLK+</td><td>D1-</td><td>D1+</td><td>D0-</td><td>D0+</td></tr>
<tr><td>LSW<1:0>=01, PSW=1</td><td>D3+</td><td>D3-</td><td>D0+</td><td>D0-</td><td>CLK+</td><td>CLK-</td><td>D1+</td><td>D1-</td><td>D2+</td><td>D2-</td></tr>
<tr><td>LSW<1:0>=01, PSW=0</td><td>D3-</td><td>D3+</td><td>D0-</td><td>D0+</td><td>CLK-</td><td>CLK+</td><td>D1-</td><td>D1+</td><td>D2-</td><td>D2+</td></tr>
<tr><td>LSW<1:0>=10, PSW=1</td><td>D0+</td><td>D0-</td><td>D1+</td><td>D1-</td><td>CLK+</td><td>CLK-</td><td>D2+</td><td>D2-</td><td>D3+</td><td>D3-</td></tr>
<tr><td>LSW<1:0>=10, PSW=0</td><td>D0-</td><td>D0+</td><td>D1-</td><td>D1+</td><td>CLK-</td><td>CLK+</td><td>D2-</td><td>D2+</td><td>D3-</td><td>D3+</td></tr>
<tr><td>LSW<1:0>=11, PSW=1</td><td>D2+</td><td>D2-</td><td>D1+</td><td>D1-</td><td>CLK+</td><td>CLK-</td><td>D0+</td><td>D0-</td><td>D3+</td><td>D3-</td></tr>
</table>
When use IIC interface, it is used as device address select.
<table>
<tr><td>PNSWAP</td><td>IIC device address</td></tr>
<tr><td>0V</td><td>0x60</td></tr>
<tr><td>1.8V</td><td>0x62</td></tr>
</table></td></tr>
<tr><td>27</td><td>GVEE</td><td>Output</td><td>Regulator for gamma. Connect a capacitor for stabilization. Connect a Schottky diode to GND．</td></tr>
</table>

28	AVDD	Output	Regulator for reference. Connect a capacitor for stabilization.
29	GVDD_P	Output	Regulator output for GAMMA analog system positive power. Connect a capacitor for stabilization. Connect all GVDD_P together.
30	DVDD	Output	Regulator output for logic digital system positive power. Connect all DVDD together.
31	GND	Power	System GND for internal digital/analog system.
32	MVSS	Power	System GND for MIPI interface.
33	DP<3>	Input/Output	This pin is DSI D3+ signal if MIPI Port interface is used. DP3/N3 is differential small amplitude signals. If not used, keep it open.
34	DN<3>	Input/Output	This pin is DSI-D3- signal if MIPI Port interface is used. DP3/N3 is differential small amplitude signals. If not used, keep it open.
35	MVSS	Power	System GND for MIPI interface.
36	DP<0>	Input/Output	This pin is DSI D0+ signal if MIPI Port interface is used. DP0/N0 is differential small amplitude signals. If not used, keep it open.
37	DN<0>	Input/Output	This pin is DSI D0- signal if MIPI Port interface is used. DP0/N0 is differential small amplitude signals. If not used, keep it open.
38	MVSS	Power	System GND for MIPI interface.
39	CKP	Input	This pin is DSI CLK+ signal if MIPI Port interface is used. CKP/N is differential small amplitude signals. If not used, keep it open.
40	CKN	Input	This pin is DSI CLK- signal if MIPI Port interface is used. CKP/N is differential small amplitude signals. If not used, keep it open.
41	MVSS	Power	System GND for MIPI interface.
42	DP<1>	Input/Output	This pin is DSI D1+ signal if MIPI Port interface is used. DP1/N1 is differential small amplitude signals. If not used, keep it open.
43	DN<1>	Input/Output	This pin is DSI D1- signal if MIPI Port interface is used. DP1/N1 is differential small amplitude signals. If not used, keep it open.
44	MVSS	Power	System GND for MIPI interface.
45	DP<2>	Input/Output	This pin is DSI-D2+ differential clock signal if MIPI Port interface is used. DP2/N2 is differential small amplitude signals. If not used, keep it open.
46	DN<2>	Input/Output	This pin is DSI D2- differential clock signal if MIPI Port interface is used. DP2/N2 is differential small amplitude signals. If not used, keep it open.
47	MVSS	Power	System GND for MIPI interface.
48	MVDD	Output	Regulator output for MIPI analog system positive power. Connect a capacitor for stabilization.
49	DVDD	Output	Regulator output for logic digital system positive power. Connect a capacitor for stabilization. Connect all DVDD together.
50	VDDI	Power	Power supply for D-PHY, DSI and digital part. Connect a capacitor for stabilization. Connect all VDDI together.
51	ELVDD	Power	Power supply for OLED cell. Connect all ELVDD together.
52	ELVSS	Power	Power supply for OLED cell. Connect all ELVSS together.
53	AVEE_S	Output	Regulator for source. Connect all AVEE_S together.
54	GVDD_P	Output	Regulator output for Pixel analog system positive power. Connect all GVDD_P together.
55	VGH	Output	power supply for interface system except for MIPI interface. Connect all VGH together.
56	GVDD_S	Output	Regulator output for source analog system positive power. Connect all GVDD_S together.
57	GND	Power	System GND for internal digital/analog system.
58	VSUB_N	Output	Regulator for pixel NMOS sub. Connect a capacitor for stabilization. Connect a Schottky diode to GND.
59	VGL	Output	Regulator for GOA. Connect all VGL together.
60	RE	Output	OLED Reset Power supply. Connect all RE together.
61	ELVEE	Output	Power supply for OLED cell. Connect all ELVEE together.

12. Reliability

No.	Item	Condition	Judgement Criterion
1	High Temperature Storage	80℃ 240hrs	After testing 1.No clearly visible defects or remarkable deterioration of display quality. 2.No function-related abnormalities *The results must be checked after 2hours later under room temperature
2	High Temperature Operating	70℃ 240hrs	
3	Low Temperature Storage	-40℃ 240hrs	
4	Low Temperature Operating	-20℃ 240hrs	
5	High Temperature / Humidity Storage	60℃/90%RH 240hrs	
6	High Temperature / Humidity Operating	60℃/90%RH 240hrs	
7	Thermal Shock	-30℃ ←→ 80℃, 0.5hr, Change time <1min, 100cycles	
8	ESD	Air discharge ±2kv Contact discharge ±1kv	After testing 1.Hard defect should not happen 2.If it would be recovered to normal state after resetting, it would be judged as a good state.