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SeeYA 1.03” SY103WAM19（2560×2560RGB）Specification

Model Name：SY103WAM19

Prepared by	Checked by	Approved by
Hu Boyu		Tong Zheng

Customer approved by	
Title	
Name	
Date	

Revision

Version	Date	Description
V1.0	2025.9.12	Initial Release
V1.1	2025.9.18	Update optical specification; (Page 6) Update 2D drawing（FPC EMI layer location，test point location， side view of the display）; (Page 10)

Contents

1 General Description

This display is a 1.03inch diagonal, 2560(RGB) × 2560 dots active-matrix color OLED module, based on single-crystal silicon backplate. This module integrates display driver and pixel driver circuit, and realizes small size, light weight, low power consumption and high resolution.

- 2560 x 2560 Real RGB Resolution
- AP Operated Resolution

  -- Maximum resolution: 2560 x 2560. When DSC on，the horizontal resolution should be multiple of 48.

  --Case1: Without scaling up support (16*M, M=80~160) x RGB x (8*N, N=90~320)

  --Case2: With scaling up 1.33x support (48*M, M=20~40) x RGB x (6*N, N=90~320)

  --Case3: With scaling up 2x support (16*M, M=40~80) x RGB x (4*N, N=90~320)
- Frame rate:

  -- 1920 x1920 input, x1.33scaling up to 2560 x2560, VESA DSC on, maximum 90Hz

  -- 2544 x2544 input, no scaling, VESA DSC on, maximum 75Hz
- Normal operation supports full color mode: 16.7M colors or 1G colors (Only DSC on)
- Interface

  -- MIPII + I2C

  -- MIPI DPHY v1.2 with one / two port (4 / 8 lanes), Maximum data rate is 1.0Gbps/Lane

  -- MIPI DSI v1.01 R11 Video mode

  -- Support VESA-DSC v1.1 in-chip decoder (3x compression ratio)

  -- Support scaling up 1.33x (1920x1920 to 2560 x 2560) and 2x (1280x1280 to 2560 x 2560)
- Scan direction selection, up or down and right or left
- Orbit supported
- Wide range Brightness adjustment
- Temperature compensation
- Power Requirement：VDDI 1.65~1.95V; ripple ≤100mV

  AVDD 5. 8~6.0V; ripple ≤100mV

  AVEE-4.8~-5.1V; ripple ≤100mV

2 General Feature

Parameter	Specification
Resolution	2560(H) x 2560 (V)
Number of dots	19.66M (2560x2560x3)
Pixel Size	7.2μm x 7.2μm
Pixel Arrangement	RGB π type
Active Area Size	18.432mm x 18.432mm / 1.03" diagonal
Luminance	Maximum 1000nits
Contrast Ratio	＞100,000
Uniformity	> 85%
Operating Voltage	VDDI=1.8V AVDD=5. 8V~6V AVEE=-4.8V~-5.1V
Power Consumption (Full white, 1000nits,1920*1920input, 1.33scaling up to 2560*2560, 90Hz, DSC on)	800mW
Gray Levels	256 or 1024 (Only DSC on)
Interface	MIPI (1 or 2-port D-PHY)
Frame Rate	Maximum 90Hz
Weight	2g
Operating Temperature	-20°C to +70°C
Storage Temperature	-30°C to +80°C

3 Optical Specification

Item	Description	Min.	Typ.	Max.	Unit
Brightness	Tpanel=15℃~70℃, at 100%duty setting	750	1000	1250	cd/m2
CR	White to Black Contrast Ratio	100,000:1			
Brightness Uniformity	9 points	85			%
CIE Red (9 points)	CIE-x	0.640	0.660	0.680	
	CIE-y	0.298	0.318	0.338	
CIE Green (9 points)	CIE-x	0.242	0.277	0.312	
	CIE-y	0.653	0.683	0.713	
CIE Blue (9 points)	CIE-x	0.120	0.140	0.160	
	CIE-y	0.039	0.059	0.079	
CIE White (Center)	CIE-x	0.298	0.313	0.328	
	CIE-y	0.314	0.329	0.344	
Color Gamut	DCI-P3	85%	90%		
View angle (White)	Brightness decay to 50%	28°			
Frame rate				90	Hz
Power consumption	Full white, 1000nits,1920*1920input, 1.33scaling up to 2560*2560, DSC on, 90Hz		800	960	mW

Note1: If there is no specified, the specification of optical is specified at 30 degrees Celsius.

Note2: Definition of optical measurement system.

The optical characteristics should be measured in dark room. Brightness is measured as peak luminance at full white pattern (Gray level=255);

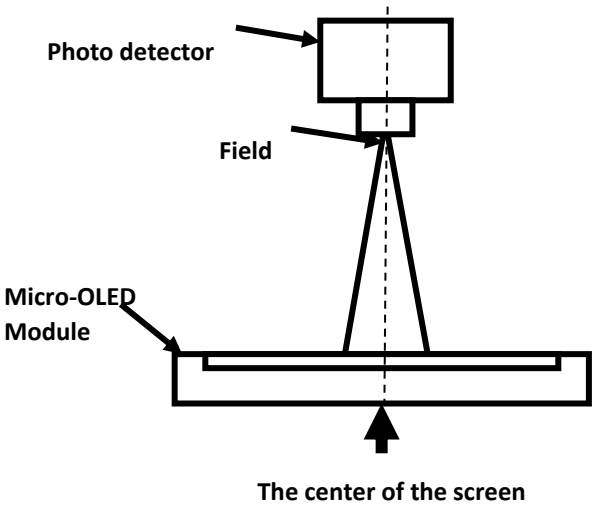


Fig. 2

Note3: Definition of Uniformity at highest gray level (255) and 70%duty emission.

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity (U) = Lmin/ Lmax

L-------Active area length; W----- Active area width

Lmax: The measured maximum luminance of all measurement position.

Lmin: The measured minimum luminance of all measurement position.

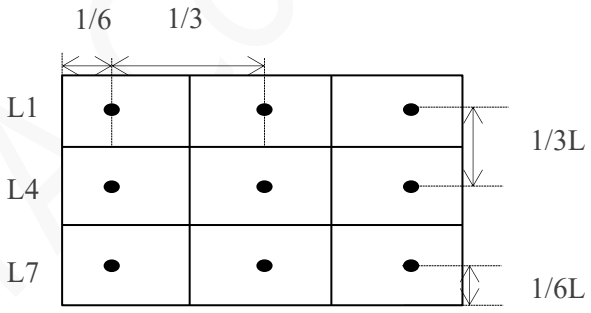
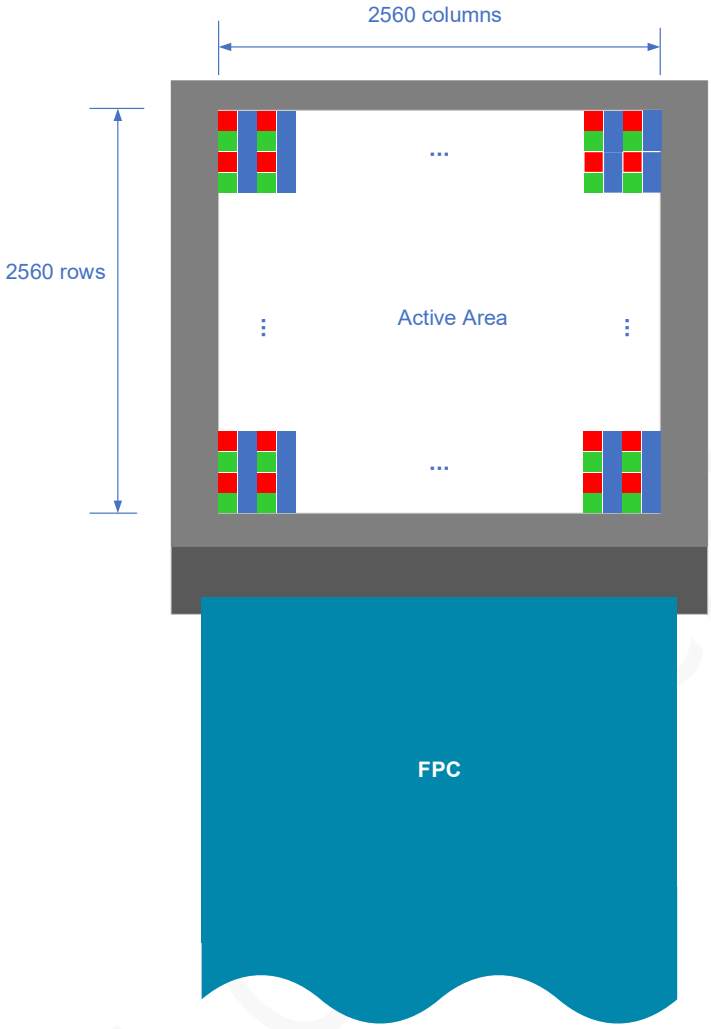
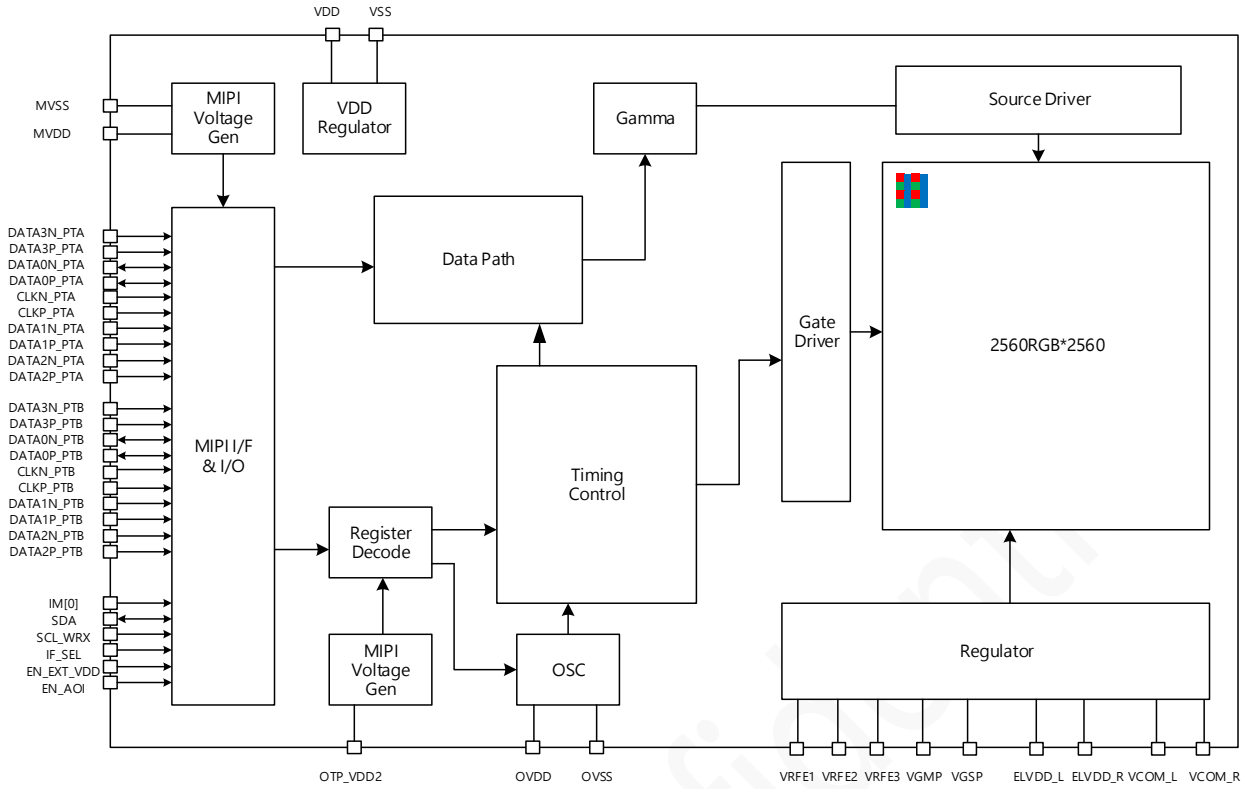


Fig. 2

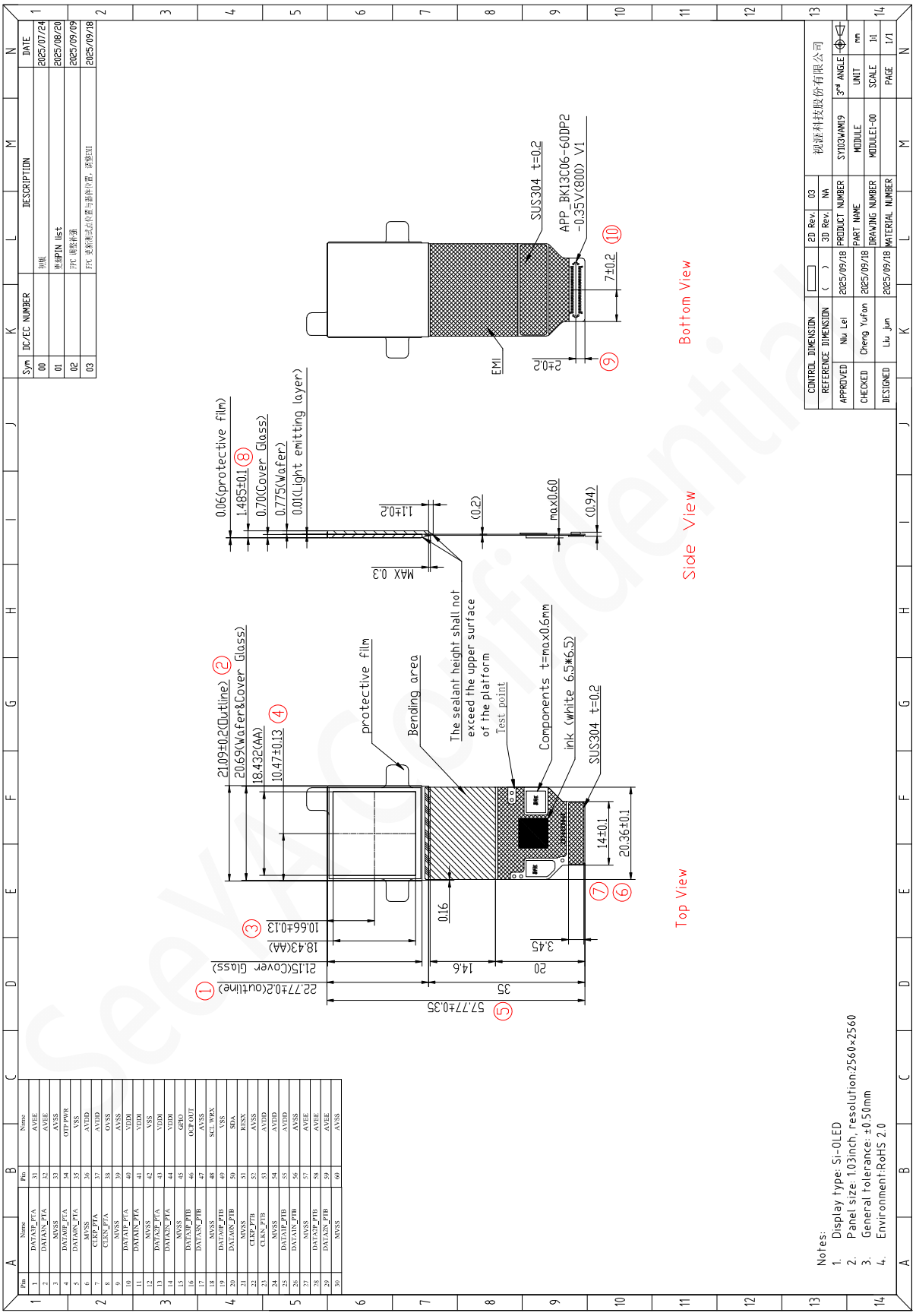
4 Pixel Arrangement



5 System block



6 Module Diagram



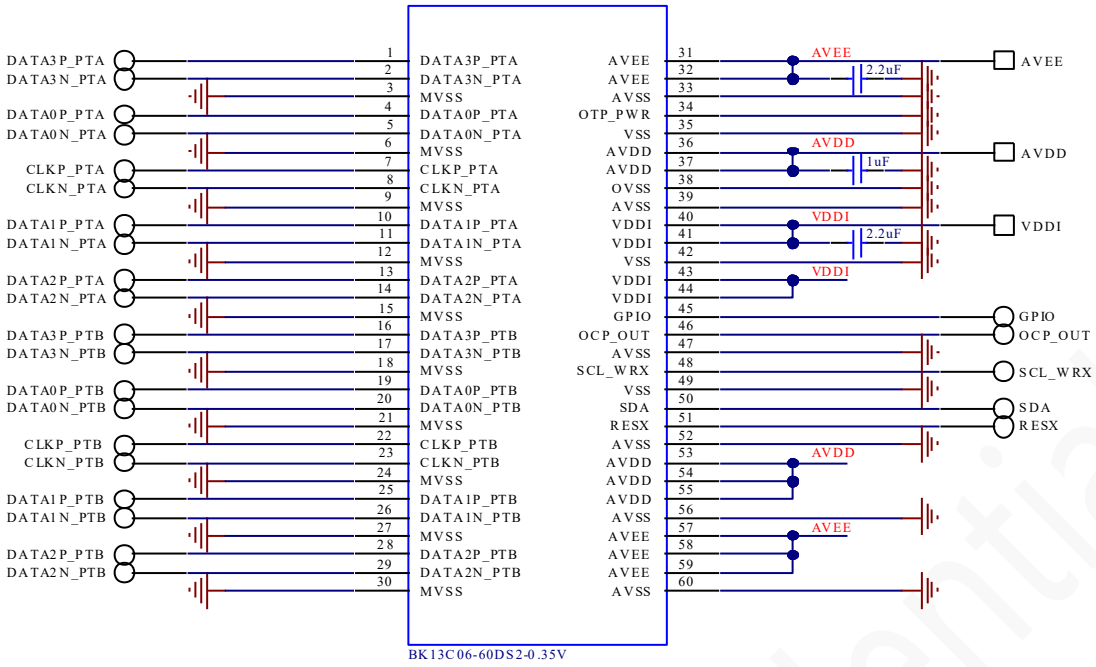
7 Pin Description

7.1 Pin Description

Pin No.	Symbol	Type	Description
1	DATA3P_PTA	Input/ Output	This pin is DSI D3+ signal if MIPI Port A interface is used. DATA3P/N_PTA is differential small amplitude signals. If not used, please keep it open.
2	DATA3N_PTA	Input/ Output	This pin is DSI D3- signal if MIPI Port A interface is used. DATA3P/N_PTA is differential small amplitude signals. If not used, please keep it open.
3	MVSS	Power	System GND for MIPI interface.
4	DATA0P_PTA	Input/ Output	This pin is DSI D0+ signal if MIPI Port A interface is used. DATA0P/N_PTA is differential small amplitude signals. If not used, please keep it open.
5	DATA0N_PTA	Input/ Output	This pin is DSI D0- signal if MIPI Port A interface is used. DATA0P/N_PTA is differential small amplitude signals. If not used, please keep it open.
6	MVSS	Power	System GND for MIPI interface.
7	CLKP_PTA	Input	This pin is DSI CLK+ signal if MIPI Port A interface is used. CLKP/N_PTA is differential small amplitude signals. If not used, please keep it open.
8	CLKN_PTA	Input	This pin is DSI CLK- signal if MIPI Port A interface is used. CLKP/N_PTA is differential small amplitude signals. If not used, please keep it open.
9	MVSS	Power	System GND for MIPI interface.
10	DATA1P_PTA	Input/ Output	This pin is DSI D1+ signal if MIPI Port A interface is used. DATA1P/N_PTA is differential small amplitude signals. If not used, please keep it open.
11	DATA1N_PTA	Input/ Output	This pin is DSI D1- signal if MIPI Port A interface is used. DATA1P/N_PTA is differential small amplitude signals. If not used, please keep it open.
12	MVSS	Power	System GND for MIPI interface.
13	DATA2P_PTA	Input/ Output	This pin is DSI D2+ signal if MIPI Port A interface is used. DATA2P/N_PTA is differential small amplitude signals. If not used, please keep it open.
14	DATA2N_PTA	Input/ Output	This pin is DSI D2- signal if MIPI Port A interface is used. DATA2P/N_PTA is differential small amplitude signals. If not used, please keep it open.
15	MVSS	Power	System GND for MIPI interface.
16	DATA3P_PTB	Input/ Output	This pin is DSI D3+ signal if MIPI Port B interface is used. DATA3P/N_PTB is differential small amplitude signals. If not used, pleased keep it open.
17	DATA3N_PTB	Input/ Output	This pin is DSI D3- signal if MIPI Port B interface is used. DATA3P/N_PTB is differential small amplitude signals. If not used, pleased keep it open.
18	MVSS	Power	System GND for MIPI interface.
19	DATA0P_PTB	Input/ Output	This pin is DSI D0+ signal if MIPI Port B interface is used. DATA0P/N_PTB is differential small amplitude signals. If not used, pleased keep it open.
20	DATA0N_PTB	Input/ Output	This pin is DSI D0- signal if MIPI Port B interface is used. DATA0P/N_PTB is differential small amplitude signals. If not used, pleased keep it open.
21	MVSS	Power	System GND for MIPI interface.
22	CLKP_PTB	Input	This pin is DSI CLK+ signal if MIPI Port B interface is used. CLKP/N_PTB is differential small amplitude signals. If not used, pleased keep it open.
23	CLKN_PTB	Input	This pin is DSI CLK- signal if MIPI Port B interface is used. CLKP/N_PTB is differential small amplitude signals. If not used, please keep it open.
24	MVSS	Power	System GND for MIPI interface.
25	DATA1P_PTB	Input/ Output	This pin is DSI D1+ signal if MIPI Port B interface is used. DATA1P/N_PTB is differential small amplitude signals. If not used, please keep it open.
26	DATA1N_PTB	Input/ Output	This pin is DSI D1- signal if MIPI Port B interface is used. DATA1P/N_PTB is differential small amplitude signals. If not used, please keep it open.
27	MVSS	Power	System GND for MIPI interface.
28	DATA2P_PTB	Input/ Output	This pin is DSI D2+ signal if MIPI Port B interface is used. DATA2P/N_PTB is differential small amplitude signals. If not used, please keep it open.

29	DATA2N_PTB	Input/ Output	This pin is DSI D2- signal if MIPI Port B interface is used. DATA2P/N_PTB is differential small amplitude signals. If not used, please keep it open.
30	MVSS	Power	System GND for MIPI interface.
31	AVEE	Power	-4.8V~-5.1V Power supply for OLED cell. Connect a capacitor for stabilization.
32	AVEE	Power	-4.8V~-5.1V Power supply for OLED cell. Connect a capacitor for stabilization.
33	AVSS	Power	System GND for analog system.
34	OTP_PWR	Input	Please connect to GND or OPEN.
35	VSS	Power	System GND for internal digital system.
36	AVDD	Power	5.8V~6VPower supply for analog system. connect a capacitor for stabilization.
37	AVDD	Power	5.8V~6VPower supply for analog system. connect a capacitor for stabilization.
38	OVSS	Power	System GND for oscillator.
39	AVSS	Power	System GND for analog system.
40	VDDI	Power	Power supply for interface system except for MIPI interface.
41	VDDI	Power	Power supply for interface system except for MIPI interface.
42	VSS	Power	System GND for internal digital system.
43	VDDI	Power	Power supply for interface system except for MIPI interface. Connect a capacitor for stabilization.
44	VDDI	Power	Power supply for interface system except for MIPI interface. Connect a capacitor for stabilization.
45	GPIO	Output	Digital global purpose in/out test pin
46	OCP_OUT	Output	Over current protect output flag.
47	AVSS	Power	System GND for analog system.
48	SCL_WRX	Input	Synchronous clock signal in I2C I/F. If this pin is not used, please connect to VDDI.
49	VSS	Power	System GND for internal digital system.
50	SDA	Input/ Output	Bi-direction data PIN in I2C I/F. If this pin is not used, please connect to VDDI.
51	RESX	Input	This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.
52	AVSS	Power	System GND for analog system.
53	AVDD	Power	5.8V~6VPower supply for analog system. connect a capacitor for stabilization.
54	AVDD	Power	5.8V~6VPower supply for analog system. connect a capacitor for stabilization.
55	AVDD	Power	5.8V~6VPower supply for analog system. connect a capacitor for stabilization.
56	AVSS	Power	System GND for analog system.
57	AVEE	Power	-4.8V~-5.1V Power supply for OLED cell. Connect a capacitor for stabilization.
58	AVEE	Power	-4.8V~-5.1V Power supply for OLED cell. Connect a capacitor for stabilization.
59	AVEE	Power	-4.8V~-5.1V Power supply for OLED cell. Connect a capacitor for stabilization.
60	AVSS	Power	System GND for analog system.

7.2 Application circuit



8 Electrical Characteristics

8.1 Absolute Maximum Ratings

The absolute maximum rating is listed on the below table. When this Micro-OLED product is used beyond the absolute maximum ratings, it may be permanently damaged. It is strongly recommended use this Micro-OLED product within the following specified limits for normal operation. If these electrical characteristic conditions are exceeded during normal operation, this Micro-OLED product will malfunction and cause poor reliability.

Item	Symbol	Value	Unit
Power Supply Voltage (1)	VDDI	5.5	V
Power Supply Voltage (2)	AVDD-AVSS	6.6	V
	AVEE-AVSS	6.6	V
Power Supply Voltage in AOI mode	VDDI	1.32	V
	AVDD-AVSS	6.6	V
	AVEE-AVSS	6.6	V
MIPI Differential Input	CLKP_PTA/B, CLKN_PTA/B DATAP0_PTA/B, DATAN0_PTA/B DATAP1_PTA/B, DATAN1_PTA/B DATAP2_PTA/B, DATAN2_PTA/B DATAP3_PTA/B, DATAN3_PTA/B	1.32	V
Input Voltage of Interface	Vin	-0.3 ~ VDDI+0.3	V
Output Voltage of Interface	Vo	-0.3 ~ VDDI+0.3	V
Operating temperature	Topr	-20 ~ 70	°C
Storage temperature	Tstg	-30 ~ 80	°C

8.2 Current Limit

Power Supply	Value	Unit
VDDI	≤200	mA
AVDD	≤160	mA
AVEE	≤100	mA
EL(ELVDD、VCOM)	≤100	mA

8.3 DC Characteristic

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
AVDD Input Level	AVDD	-	5. 8		6.0	V
Digital I/O Power Supply (non-MIPI I/O)	VDDI	-	1.65	1.8	1.95	V
Digital I/O Input Level @Logic High	VIH	VDDI=1.65V ~ 1.95V	0.7*VDDI	-	VDDI	V
Digital I/O Input Level @Logic Low	VIL	VDDI=1.65V ~ 1.95V	0	-	0.3*VDDI	V
Digital I/O Output Level @Logic High	VOH	Iout = -1mA	0.8*VDDI	-	VDDI	V
Digital I/O Output Level @Logic Low	VOL	Iout = +1mA	0	-	0.2*VDDI	V
Digital I/O Input leakage @Logic High	IIHD	Vin = VDDI			1	uA

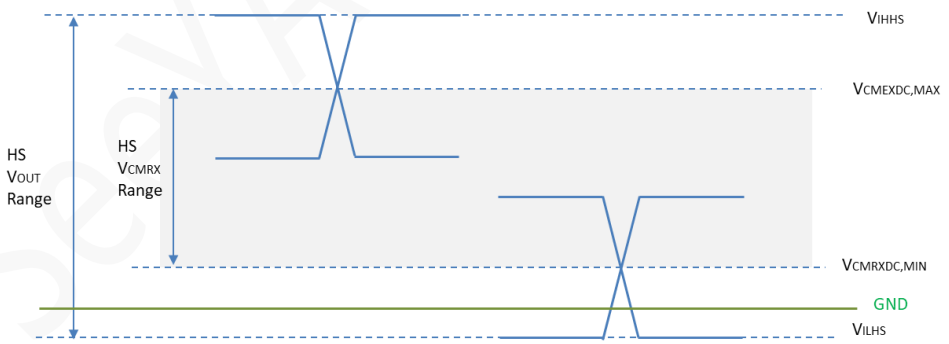
Digital I/O Input leakage @Logic Low	IILD	Vin = 0	-1			uA
MIPI I/O Power Supply	MVDD	-	-	1.2	-	V
MIPI Input leakage @Logic High	IIHMD	Vin = MVDD			1	uA
MIPI Input leakage @Logic Low	IILMD	Vin = 0	-1			uA
AVDD Current（AVDD-GND）	IAVDD				100	mA
AVEE Current（AVEE-GND）	IAVEE				80	mA
VDDI Current（VDDI-GND）	IVDDI				150	mA

8.4 DSI DC/AC Characteristic

8.4.1 Receiver characteristic

High speed receiver characteristic

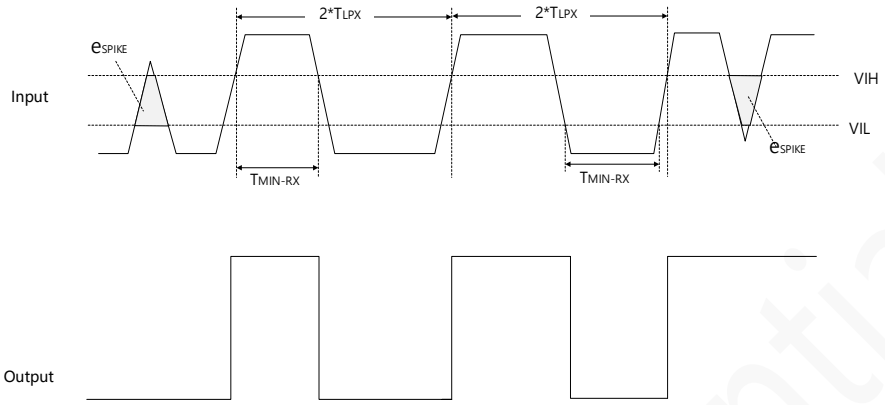
Parameter	Description	Min	Typ.	Max	Unit
VCMRX(DC)	Common-mode voltage HS receive mode	70	-	330	mV
ZID	Differential input impedance	80	100	125	Ω
VIDTH	Differential input high threshold	-	-	70	mV
VIDTL	Differential input low threshold	-70	-	-	mV
VIHHS	Single-ended input high voltage	-	-	460	mV
VILHS	Single-ended input low voltage	-40	-	-	mV
CCM	Common-mode termination	-	-	60	pF



Low power receiver characteristic

Parameter	Description	Min	Typ.	Max	Unit
VIH	Logic 1 input voltage	880	-	-	mV

VIL	Logic 0 input voltage, not in ULP state	-	-	550	mV
VIL_ULPS	Logic 0 input voltage, ULP state	-	-	300	mV
VHYST	Input hysteresis	25	-	-	mV
eSPIKE	Input pulse rejection	-	-	300	V·ps
TMIN-RX	Minimum pulse width response	20	-	-	



8.4.2 Transmitter Characteristics

High-Speed Transmitter Characteristics

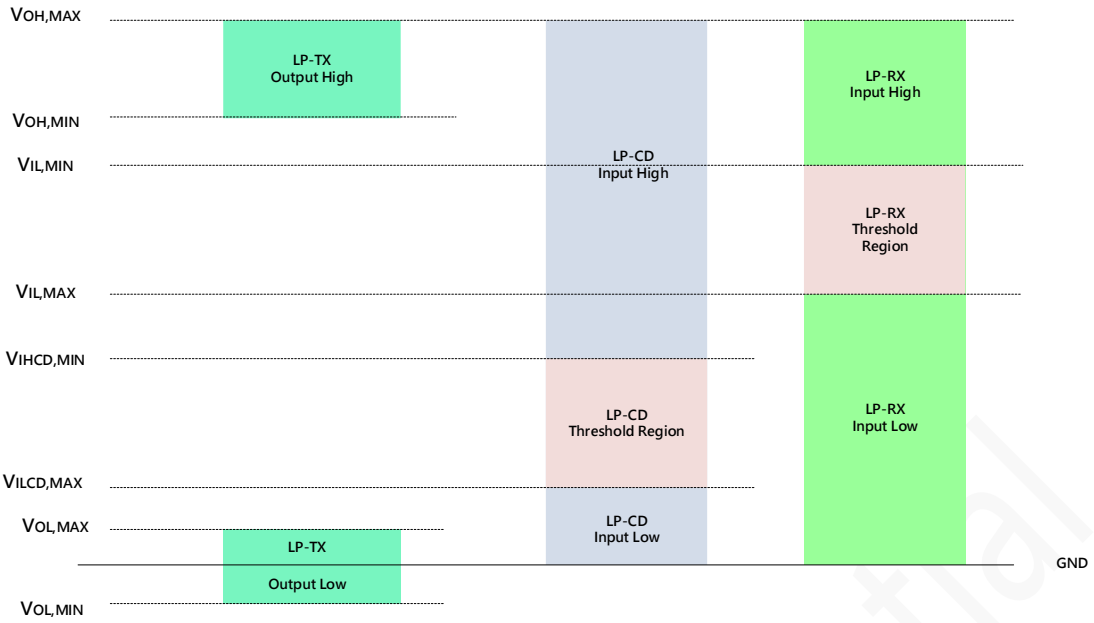
Parameter	Description	Min	Typ.	Max	Unit
V_{CMTX}	HS transmit static common-mode voltage	150	200	250	mV
$\|V_{OD}\|$	HS transmit differential voltage	140	200	270	mV
V_{OHHS}	HS output high voltage	-	-	360	mV
Z_{OS}	Single ended output impedance	40	50	62.5	Ω
t_R and t_F (note1,2)	20%-80%rise time and fall time	-	-	0.3	UI
		-	-	0.35	UI

Note:

1. Applicable when supporting maximum HS bitrates ≤ 1Gbps (UI≥1ns)

Low-Power Transmitter Characteristics

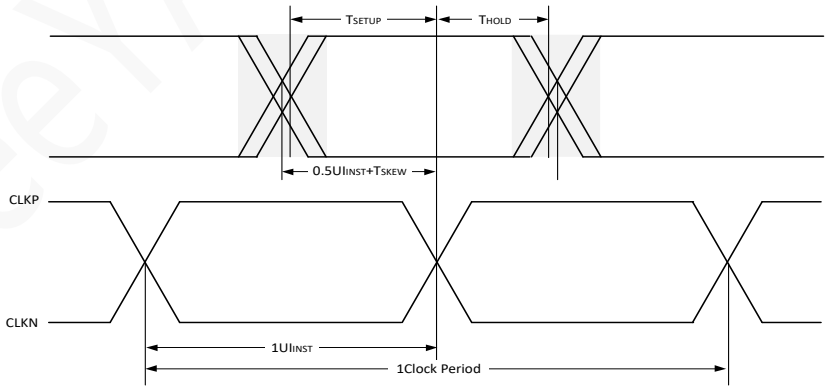
Parameter	Description	Min	Typ.	Max	Unit
V_{OH}	The output high level	1.1	1.2	1.3	V
V_{OL}	The output low level	-50	-	50	mV
Z_{OLP}	Output impedance of LP transmitter	110	-	-	Ω
V_{IHCD}	Logic1 contention threshold	450	-	-	mV
V_{ILCD}	Logic0 contention threshold	-	-	200	mV



8.5 Timing Characteristics

8.5.1 High Speed Mode Characteristics

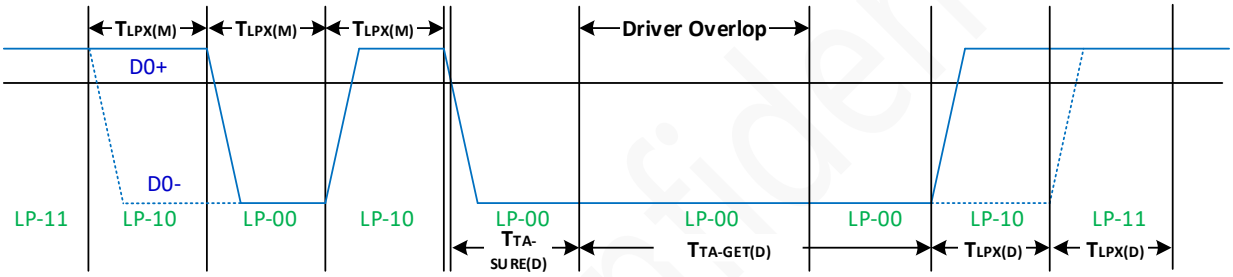
Parameter	Symbol	Min	Typ.	Max	Unit
UI instantaneous	UIINST	1	-	3	ns
T Data to Clock Skew	TSKEW	-0.15	-	0.15	UIHS
RX Data to Clock Setup Time Tolerance	TSETUP	0.15	-	-	UIHS
RX Data to Clock Hold Time Tolerance	THOLD	0.15	-	-	UIHS



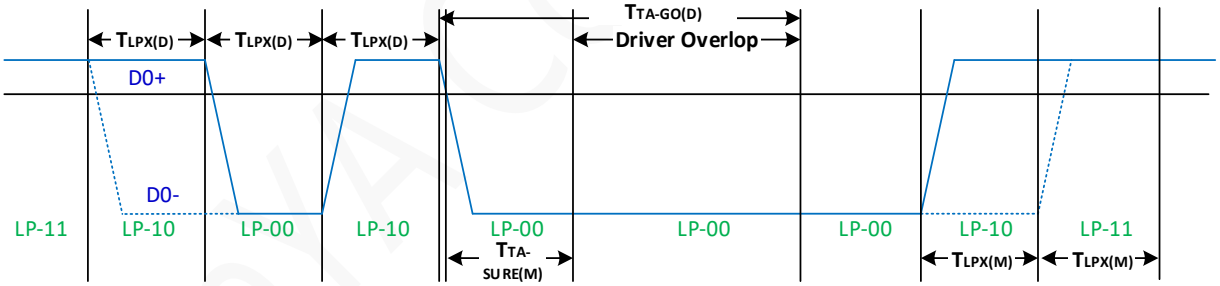
8.5.2 Low Power Mode Characteristics

Parameter	Description	Min	Typ.	Max	Unit
TLPX(M)	Transmitted length of any Low-Power state period (MCU to display module)	50	-	-	ns
TLPX(D)	Transmitted length of any Low-Power state period (display module to MCU)	50	-	-	ns
TTA-SURE	Time that the new transmitter waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround	TLPX	-	2*TLPX	
TTA-GET	Time that the new transmitter drives the Bridge state (LP-00) after accepting control during a Link Turnaround	5* TLPX			
TTA-GO	Time that the transmitter drives the Bridge state(LP-00) before releasing control during a Link Turnaround	4* TLPX			

- Bus Turnaround from MPU to display module



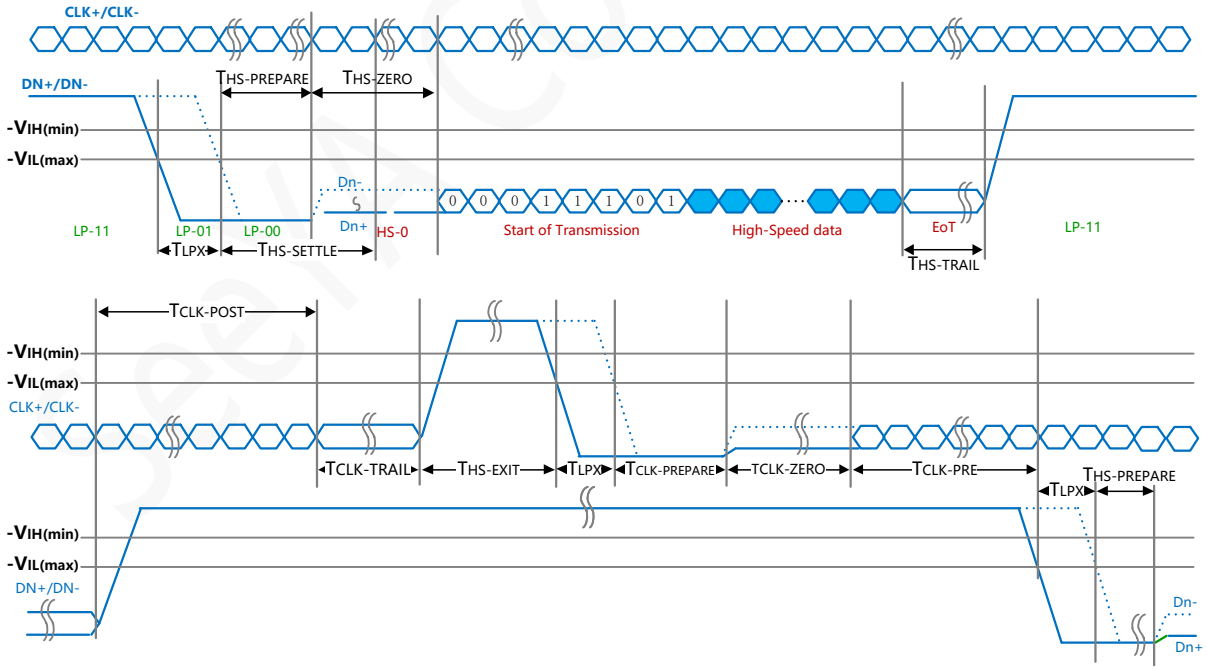
- Bus Turnaround from MPU to display module



8.5.3 High Speed Mode Operation Timing Characteristics

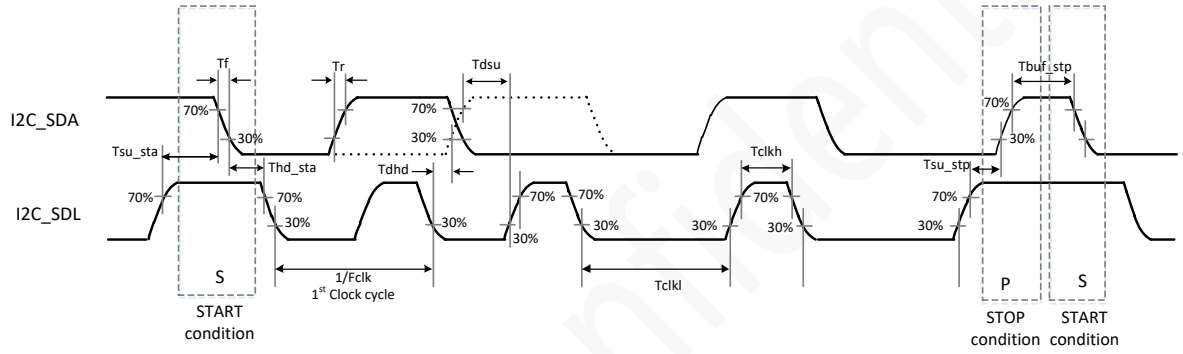
Parameter	Description	Min	Typ.	Max	Unit
TCLK-POST	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of TCLK-TRAIL	60ns+52* UI	-	-	ns
TCLK-PRE	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode	8	-	-	UI
TCLK-PREPARE	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	38	-	95	ns
TCLK-SETTLE	Time interval during which the HS receiver should ignore any Clock Lane HS transitions, starting from the beginning of TCLK-PREPARE	95	-	300	ns

TCLK-TERM_EN	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL, MAX	-	-	38	ns
TCLK-TRAIL	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst	60	-	-	ns
TCLK-PREPARE+TCLK-ZERO	TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock	300	-	-	ns
THS-EXIT	Time that the transmitter drives LP-11 following a HS burst	100	-	-	ns
TD-TERM_EN	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX	-	-	35ns+4*UI	ns
THS-PREPARE	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns+4*UI	-	85ns+6*UI	ns
THS-PREPARE+THS-ZERO	THS-PREPARE + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence	145ns+10*UI	-	-	ns
THS-SETTLE	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of THS-PREPARE. The HS receiver shall ignore any Data Lane transitions before the minimum value, and the HS receiver shall respond to any Data Lane transitions after the maximum value.	85ns+6*UI	-	145ns+10*UI	ns



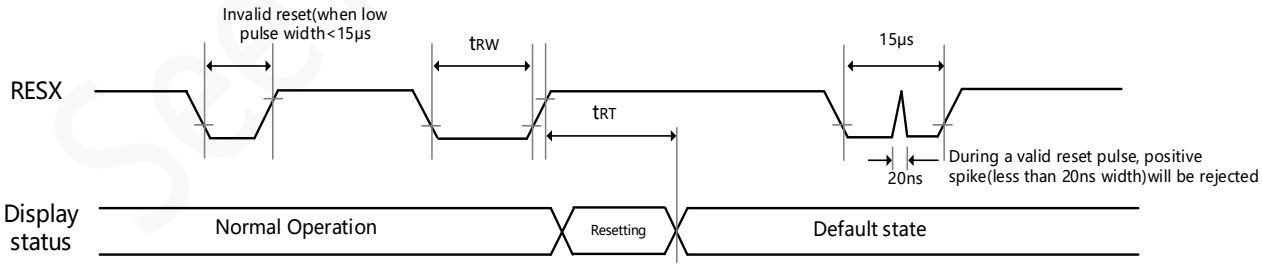
8.5.4 I2C-Bus Interface Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
I2C Clock Frequency	Fclk	-	-	400	kHz	
I2C Clock Low	Tclkl	1300	-	-	ns	
I2C Clock High	Tclkh	600	-	-	ns	
I2C Data Rising Time	Tdr	-	-	300	ns	
I2C Data Falling Time	Tdf	-	-	300	ns	
I2C Data Setup Time	Tdsu	100	-	-	ns	
I2C Data Hold Time	Tdhd	-	-	TBD	ns	
I2C Setup Time (Start Condition)	Tsu_sta	600	-	-	ns	
I2C Hold Time (Start Condition)	Thd_sta	600	-	-	ns	
I2C Setup Time (Stop Condition)	Tsu_stp	600	-	-	ns	
I2C Bus Free Time (Stop Condition)	Tbuf_stp	1300	-	-	ns	



8.6 Reset Timing Characteristics

When Reset happens in Sleep-out mode, this Micro-OLED product will enter blanking sequence with the maximum time 120 msec. Then this Micro-OLED product will remain in blanking state and return \ default state. During reset complete time (tRT), data in OTP will be re-loaded and latched to internal registers. This data re-load is done every time when there is an H/W reset and completes within 20 msec after the rising edge of RESX. Therefore, it is necessary to wait at least 20 msec after releasing the RESX before sending commands. Moreover, the Sleep-out command cannot be sent in 120 msec. Spike (less than 20ns width) Rejection can also be applied during a valid reset pulse.

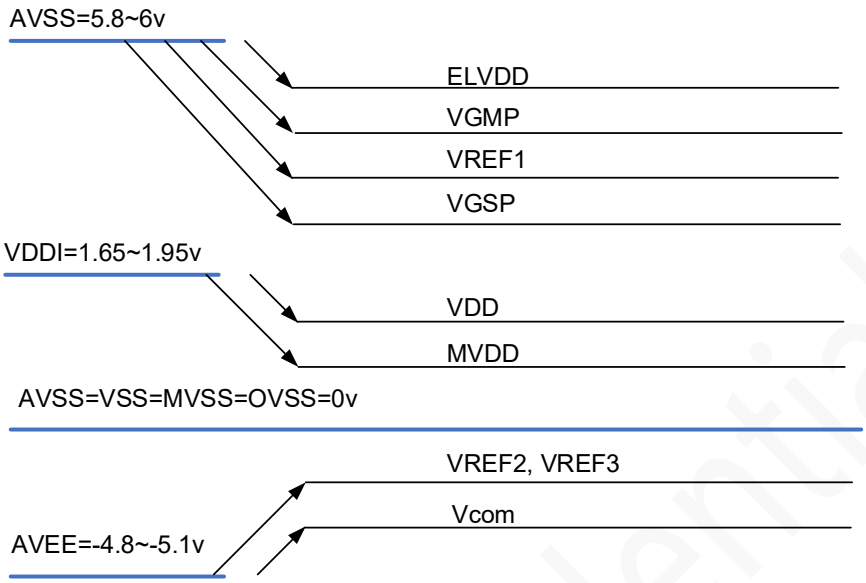


Reset time @VDDI=1.65V to 1.95V, AVSS = VSS = MVSS = 0V, Ta=-40°C to 85°C

Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit	Description
RESX	tRW	Reset low pulse width	15			us	
	tRT	Reset Complete time			20	ms	When reset applied at sleep-in mode
					120	ms	When reset applied at sleep-out mode

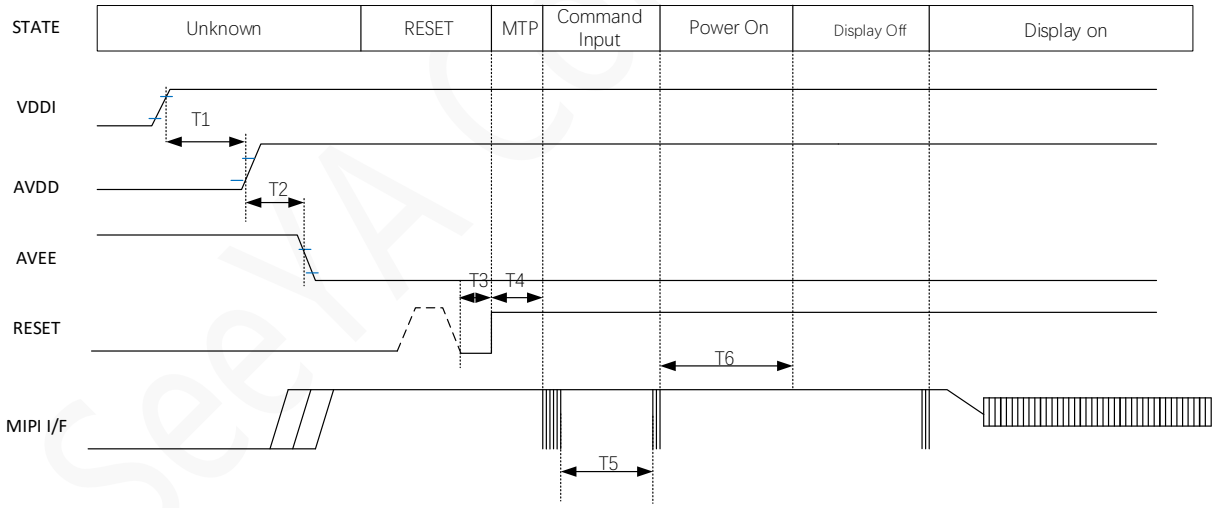
9 Power Sequence

9.1 Power Generation Scheme

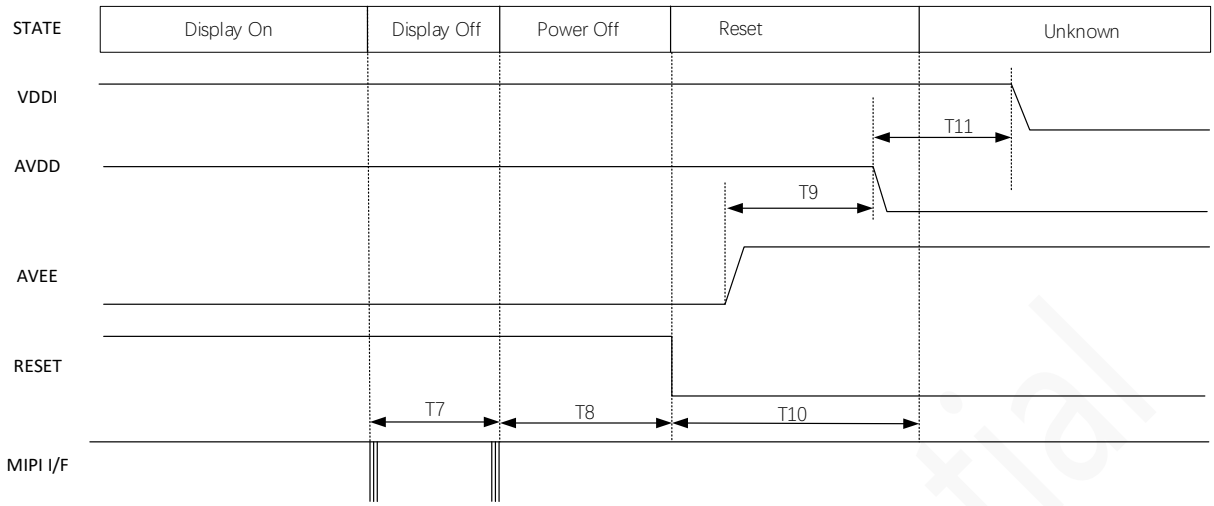


9.2 Power Sequence

Power on sequence



Power off sequence



Symbol	Min.	Typ.	Max.	Unit	Description
T1	1	-	-	ms	Power on time between VDDI and AVDD
T2	2	-	-	ms	Power on time between AVDD and AVEE
T3	1	-	-	ms	Effective hardware reset period
T4	20	-	-	ms	OTP reload time
T5	0	-	-	ms	The time is between initial code finished and sleep-out command
T6	2	-	8	Vsync Interval	Power on sequence, the period can be modified
T7	1	-	-	Vsync Interval	Blanking region
T8	-	1	-	Vsync Interval	Power off sequence, the period can be modified
T9	2	-	-	ms	Power off time between AVEE and AVDD
T10	1	-	-	ms	Effective hardware reset period
T11	1	-	-	ms	Power off time between AVDD and VDDI

10 Interface

This Micro-OLED product supports MIPI interface and inter-integrated circuit interface (I2C). 1 port MIPI or 2 port MIPI is selected by register, and I2C is selected by IM0, the detail interface selection by IM0 pin and register of PORT1_2_SEL shows in below table. IM0 has been fixed on high voltage (=1).

IM0	PORT1_2_SEL	Command Execute	Image Write
0	0	MIPI	MIPI 1port
0	1	MIPI	MIPI 2 port
1	0	I2C or MIPI	MIPI 1port
1	1	I2C or MIPI	MIPI 2 port

10.1 I2C Interface

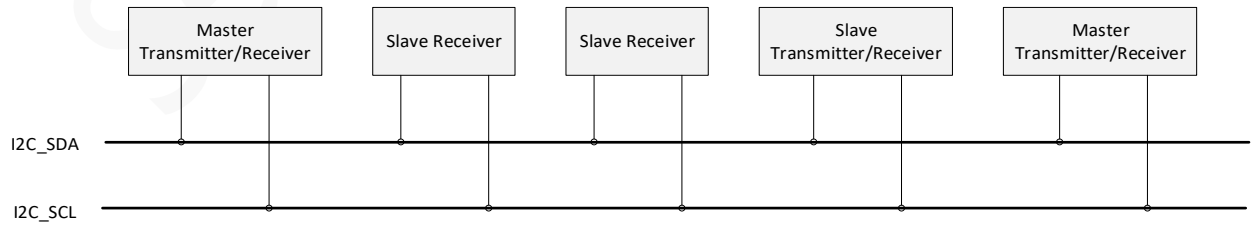
The I2C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines are the Serial Data Line (I2C_SDA) and Serial Clock Line (I2C_SCL). Both lines must be connected to a positive power supply via pull-up resistors. Data transfer can be initiated only when the bus is not busy. The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte maybe sent. The master generates all clock pulses, including the ninth acknowledge clock pulse.

10.1.1 I2C-Bus Protocol

Before any data is transmitted on the I2C-bus, the device which should response is addressed first. There are several slave addresses can be selected by MCU. The slave addressing is always carried out with the first byte transmitted after the START procedure.

Definition

- Transmitter: The device which sends the data to the bus.
- Receiver: The device which receives the data from the bus.
- Master: The device which initiates a transfer generates clock signals and terminates a transfer.
- Slave: The device addressed by a master.
- Multi-master: More than one master can attempt to control the bus at the same time without corrupting the message.
- Arbitration: Procedure to ensure that. If more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.
- Synchronization: Procedure to synchronize the clock signals of two or more devices.



10.1.2 Write Sequence

This Micro-OLED product supports register write sequence via I2C-bus transfer. The register writing supports single register write mode. The detailed transfer sequences are illustrated and described as below.

(1) Data transfer for register writing should follow the format shown as below.

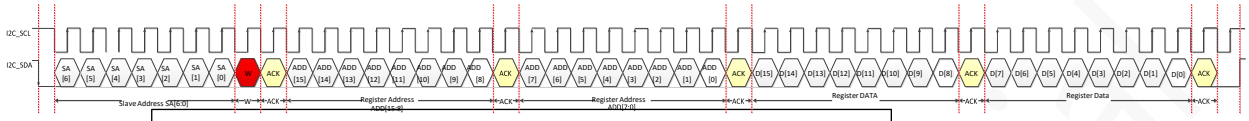
(2) After the START condition, a slave address is sent. R/$\overline{W}$ bit is setting to “0” for Write.

(3) The slave issues an ACK to the master.

(4) 8-bits register address transfer first then transfer the register data parameter.

(5) A data transfer is always terminated by a STOP condition.

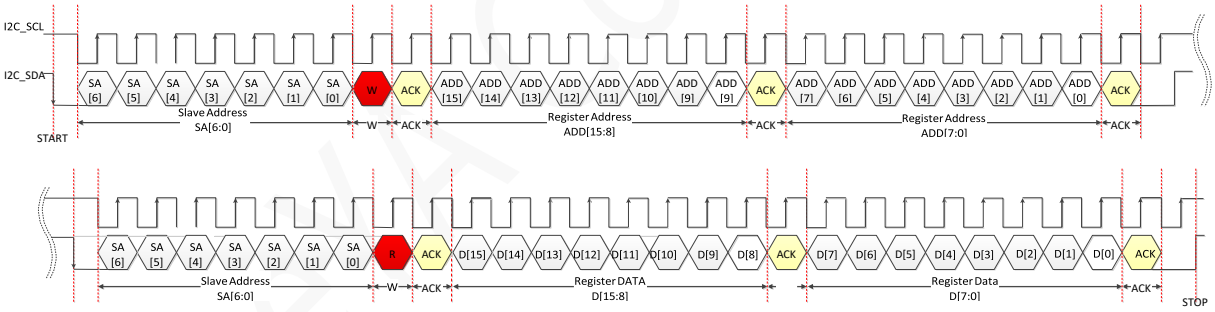
(6) The chip SA [6:0] =1001100.



W: Write Bit, W= “0” here
ACK: Acknowledge Bit, ACK= “0” here
SA[6:0]: Slave Address
ADD[15:0]: Register Address
D[15:0]: Register Data

10.1.3 Read Sequence

This Micro-OLED product supports register read sequence via I2C-bus transfer. The register reading supports single register read mode. The register data reading transfer are shown as below.



W: Write Bit, W= “0” here, R: Read Bit,R= “1” here
ACK: Acknowledge Bit, ACK= “0” here
SA[6:0]: Slave Address
ADD[15:0]: Register Address
D[15:0]: Register Data
NACK: Negative Acknowledge Bit, NACK= “1” here

10.2 MIPI Interface

Display serial interface (DSI) specifies the interface between a host processor and a peripheral such as a display module. It builds on existing MIPI Alliance specification by adoption pixel formats and command set.

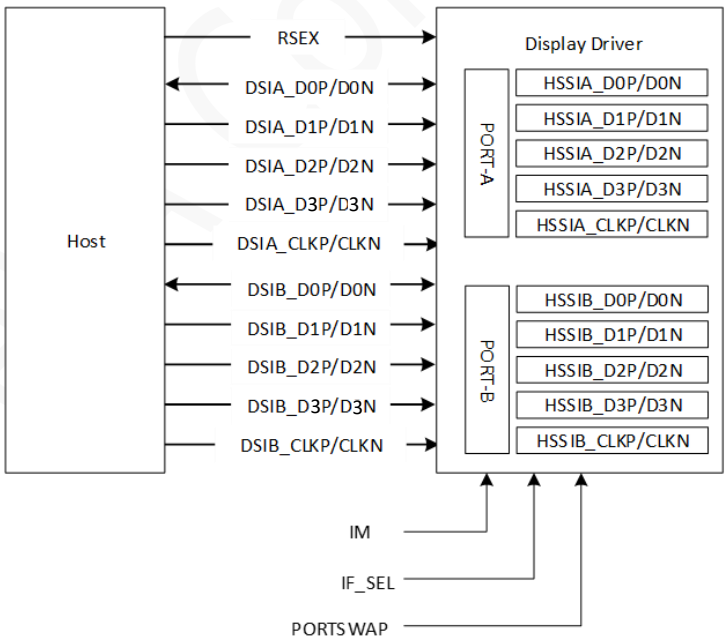
For DPHY, there are one Clock Lane and 1~4 Data Lane. The configuration for DPHY between host and this Micro-OLED product shows as the table below.

Lane Pair	Available Operation Mode	
Clock Lane	Unidirectional Lane	Forward High-Speed Clock Escape Mode (ULPS only)
Data Lane 0	Bi-directional Lane	Forward High-Speed Data Bi-directional Escape Mode Bi-directional LPDT
Data Lane 1	Unidirectional Lane	Forward High-Speed Data No LPDT Escape Mode (ULPM only)
Data Lane 2	Unidirectional Lane	Forward High-Speed Data No LPDT Escape Mode (ULPM only)
Data Lane 3	Unidirectional Lane	Forward High-Speed Data No LPDT Escape Mode (ULPM only)

10.1.1 DSI System Configuration

[DPHY]

This Micro-OLED product supports MIPI 2 port with 2, 3 or 4 lane configurations for DPHY. The system configuration is shown as the figure below. There are HW pin (IM, PORTSWAP) and registers (Lane_num_cfg, PSWAP, DSWAP) which can set the interface and lane related configuration.

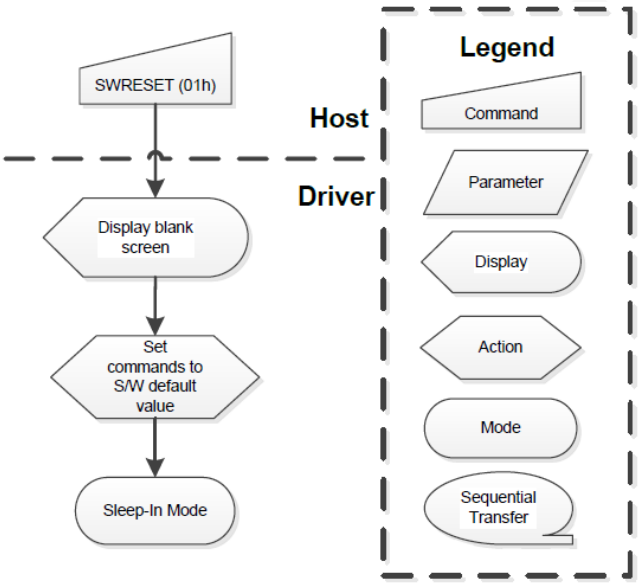


11 User Command

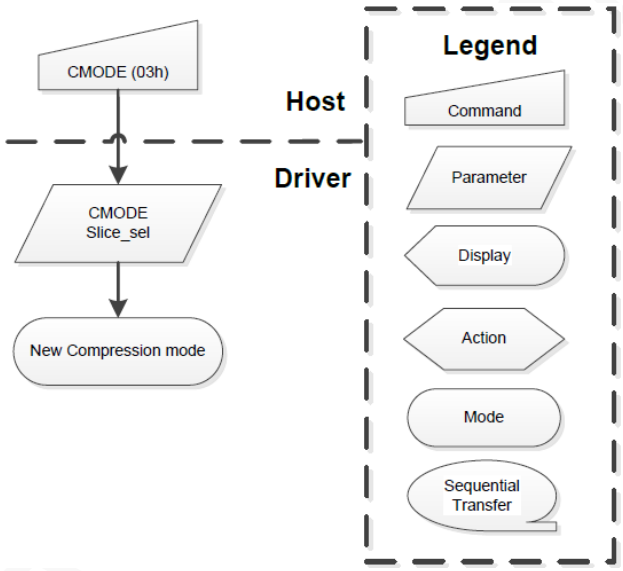
11.1 Command1 list

Instruction	R/W	Address		D7	D6	D5	D4	D3	D2	D1	D0	Default
		MIPI	Non-MIPI									
SWRESET	W	01h	0100h	No Parameter								N/A
CMODE	R/W	03h	0300h	slice2_sel	-	-	-	-	-	-	CMODE	80h
SLPIN	W	10h	1000h	No Parameter								N/A
SLPOUT	W	11h	1100h	No Parameter								N/A
ALLPOFF	W	22h	2200h	No Parameter								N/A
ALLPON	W	23h	2300h	No Parameter								N/A
DSPOFF	W	28h	2800h	No Parameter								N/A
DSPON	W	29h	2900h	No Parameter								N/A
CASET	R/W	2Ah	2A00h	XS[15:8]								00h
	R/W		2A01h	XS[7:0]								00h
RASET	R/W	2Bh	2B00h	YS[15:8]								00h
	R/W		2B01h	YS[7:0]								00h
TEON	R/W	35h	3500h	-	-	-	-	-	-	-	M	00h
MADCTL	R/W	36h	3600h	-	-	-	-	RGB	-	RSMX	RSMY	00h
IDMOFF	R/W	38h	3800h	No Parameter								N/A
IDMON	R/W	39h	3900h	No Parameter								N/A
SCACTRL	W	69h	6900h							SC_MOD_SEL[1:0]		00h
IFCONFG	R/W	6Bh	6B00h	-	-	-	PORT1_2_SEL_CMD1	-	-	-	-	10h
RESCTRL1	R/W	80h	8000h	-	-	-	-	-	-	-	OSC_FREQ_SEL	01h
			8001h	NC[7:0]								40h
			8002h	NL[7:0]								40h
			8003h	-	-	-	NC[8]	-	-	-	NL[8]	11h

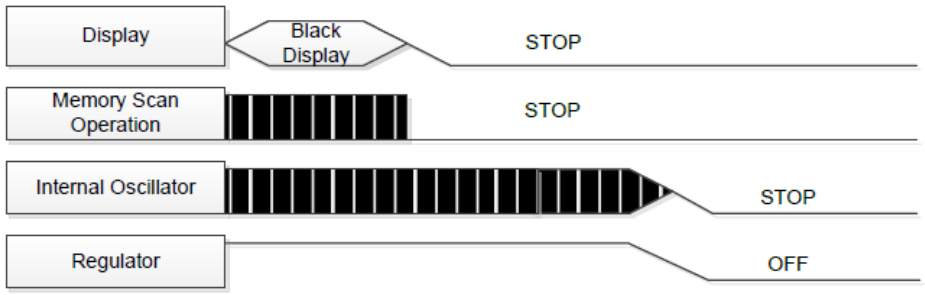
SWRESET(0100h): Software Reset

<table>
<tr><td>0100H</td><td colspan="11">SWRESET</td></tr>
<tr><td rowspan="2">Instruction</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td colspan="9">Parameter</td></tr>
<tr><td>MIPI</td><td>Other</td><td>D15- D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>SWRESET</td><td>W</td><td>01h</td><td>0100h</td><td>-</td><td colspan="7">No Parameter</td></tr>
<tr><td>Description</td><td colspan="11">When the Software Reset command is executed, all related register and parameters are reset to their S/W Reset default values.</td></tr>
<tr><td>Restriction</td><td colspan="11">It is necessary to wait 10m sec to send any command following the S/W Reset.
If S/W Reset is executed in Sleep-out mode, it is necessary to wait 120m sec to send Sleep-Out command. The Software Reset command cannot be sent during Sleep-Out sequence. Any new command cannot be sent within 8-frame until device enters Sleep-In mode.</td></tr>
<tr><td>Default</td><td colspan="11"><table>
<tr><td>Status</td><td colspan="2">Default Value</td></tr>
<tr><td>Power On Sequence</td><td>0100h</td><td>N/A</td></tr>
<tr><td>SW Reset</td><td colspan="2">The same as above</td></tr>
<tr><td>HW Reset</td><td colspan="2">The same as above</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="11"> 
</td></tr>
</table>

CMODE(0300h): Compression Mode

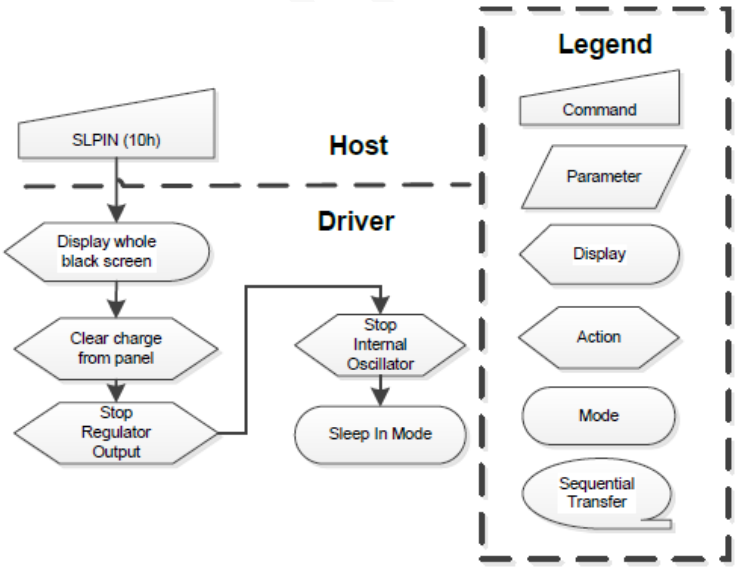
<table>
<tr><td>0400H</td><td colspan="12">RDID123</td></tr>
<tr><td rowspan="2">Instruction</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td colspan="10">Parameter</td></tr>
<tr><td>MIPI</td><td>Other</td><td>D15- D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>CMODE</td><td>R/W</td><td>03h</td><td>0300h</td><td>-</td><td>D7</td><td></td><td></td><td></td><td></td><td></td><td></td><td>D0</td></tr>
<tr><td>Description</td><td colspan="12">These commands are used for compression mode
<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Comment</th></tr>
<tr><td>D7</td><td>slice_sel</td><td>Compression slice selection</td><td>0=1 slice
1=2 slice</td></tr>
<tr><td>D0</td><td>CMODE</td><td>Enable/Disable compression mode</td><td>0=Disable
1=Enable</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="12">-</td></tr>
<tr><td>Default</td><td colspan="12"><table>
<tr><th>Status</th><th colspan="2">Default Value</th></tr>
<tr><td>Power On Sequence</td><td>0300h</td><td>80h</td></tr>
<tr><td>SW Reset</td><td colspan="2">The same as above</td></tr>
<tr><td>HW Reset</td><td colspan="2">The same as above</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="12"> 
</td></tr>
</table>

SLPIN (1000h): Sleep In

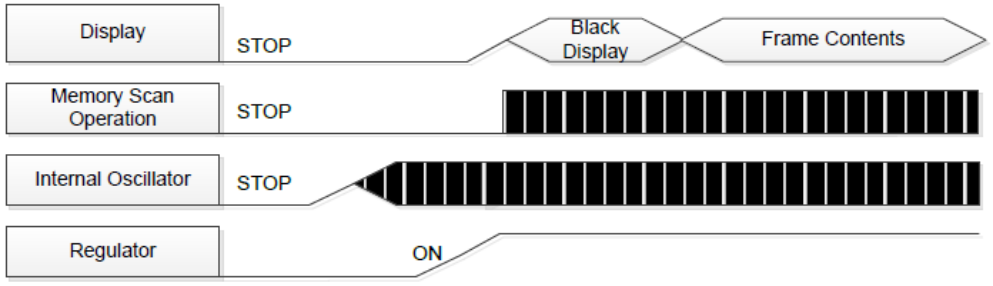
1000H	SLPIN											
Instruction	R/W	Address		Parameter								
		MIPI	Other	D15- D8	D7	D6	D5	D4	D3	D2	D1	D0
SLPIN	W	10h	1000h	-	No Parameter							
Description	This command force display module to enter *Sleep-In* mode. Under *Sleep-In* mode, internal display oscillator, and panel scanning are all stopped. The interface and related registers are still working and keeps its values. 											
Restriction	-											

Default	Status	Default Value	
	Power On Sequence	1000h	Sleep In Mode
	SW Reset	The same as above	
	HW Reset	The same as above	

Flow Chart

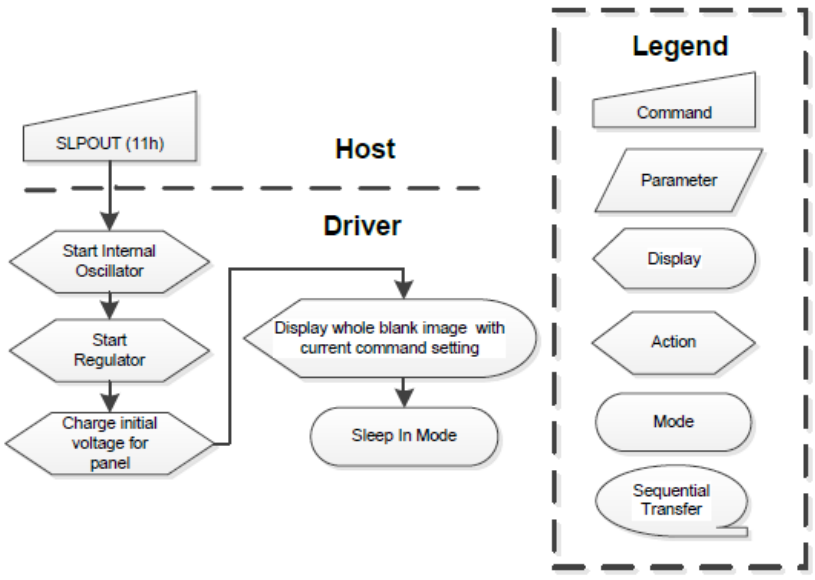


SLPOUT (1100h): Sleep Out

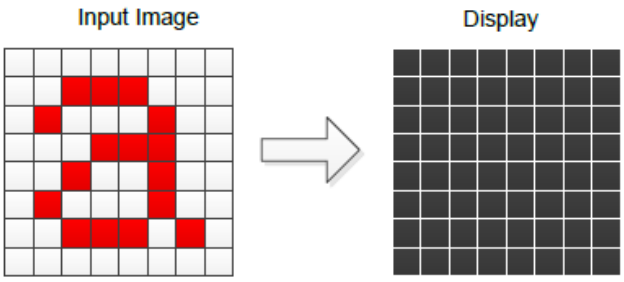
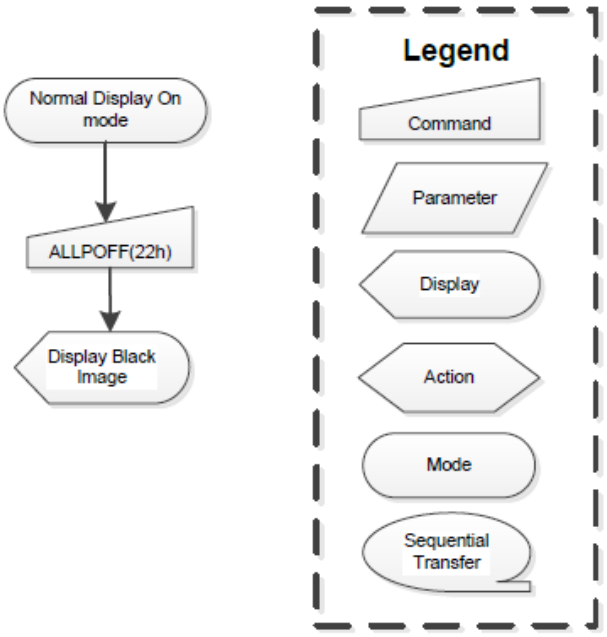
1100H	SLPOUT											
Instruction	R/W	Address		Parameter								
		MIPI	Other	D15- D8	D7	D6	D5	D4	D3	D2	D1	D0
SLPOUT	W	11h	1100h	-	No Parameter							
Description	This command force display module to exit *Sleep-In* mode. Under *Sleep-out* mode regulator, internal display oscillator, and panel scanning are all enabled. 											
Restriction	-											

Default	Status	Default Value	
	Power On Sequence	1100h	Sleep In Mode
	SW Reset	The same as above	
	HW Reset	The same as above	

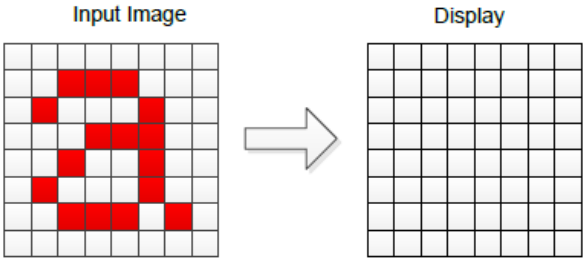
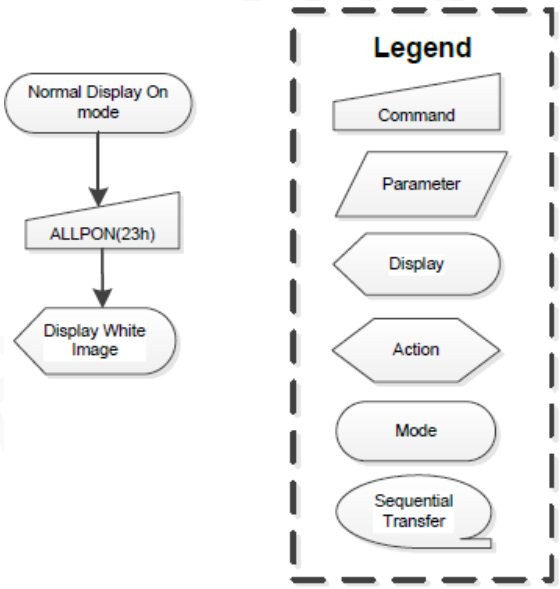
Flow chart



ALLPOFF (2200h): All Pixels OFF

<table>
<tr><td>2200H</td><td colspan="12">ALLPOFF</td></tr>
<tr><td rowspan="2">Instruction</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td colspan="10">Parameter</td></tr>
<tr><td>MIPI</td><td>Other</td><td>D15- D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>ALLPOFF</td><td>W</td><td>22h</td><td>2200h</td><td>-</td><td colspan="9">No Parameter</td></tr>
<tr><td>Description</td><td colspan="12">This command forces the display module to display black image in Display-On Mode.
 
</td></tr>
<tr><td>Restriction</td><td colspan="12">-</td></tr>
<tr><td>Default</td><td colspan="12"><table>
<tr><td>Status</td><td colspan="2">Default Value</td></tr>
<tr><td>Power On Sequence</td><td>2200h</td><td>All Pixel Off</td></tr>
<tr><td>SW Reset</td><td colspan="2">The same as above</td></tr>
<tr><td>HW Reset</td><td colspan="2">The same as above</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="12"> 
</td></tr>
</table>

ALLPON (2300h): All Pixel ON

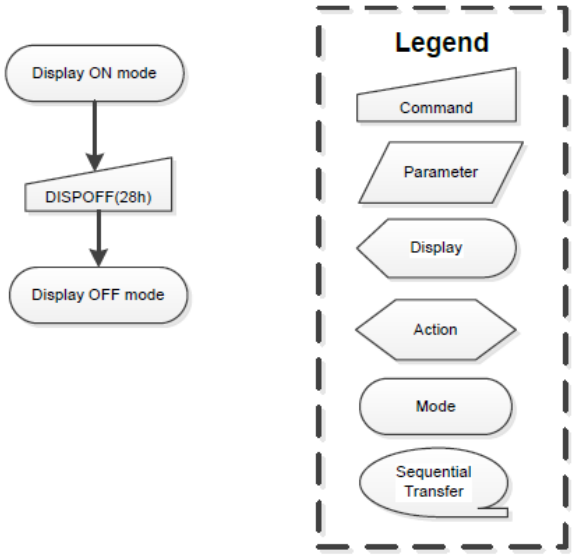
<table>
<tr><td>2300H</td><td colspan="12">ALLPON</td></tr>
<tr><td rowspan="2">Instruction</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td colspan="9">Parameter</td></tr>
<tr><td>MIPI</td><td>Other</td><td>D15- D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>ALLPON</td><td>W</td><td>23h</td><td>2300h</td><td>-</td><td colspan="8">No Parameter</td></tr>
<tr><td>Description</td><td colspan="12">This command forces the display module to display white image in Display-On Mode.
 
</td></tr>
<tr><td>Restriction</td><td colspan="12">-</td></tr>
<tr><td>Default</td><td colspan="12"><table>
<tr><td>Status</td><td colspan="2">Default Value</td></tr>
<tr><td>Power On Sequence</td><td>2300h</td><td>All Pixel Off</td></tr>
<tr><td>SW Reset</td><td colspan="2">The same as above</td></tr>
<tr><td>HW Reset</td><td colspan="2">The same as above</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="12"> 
</td></tr>
</table>

DISPOFF (2800h): Display OFF

2800H	DISPOFF											
Instruction	R/W	Address		Parameter								
		MIPI	Other	D15- D8	D7	D6	D5	D4	D3	D2	D1	D0
DISPOFF	W	28h	2800h	-	No Parameter							
Description	This command forces the display module to stop displaying image data.											
Restriction	This command has no effect when display driver is already in DISPLAY-OFF mode											

Default	Status	Default Value	
	Power On Sequence	2800h	Display Off
	SW Reset	The same as above	
	HW Reset	The same as above	

Flow Chart

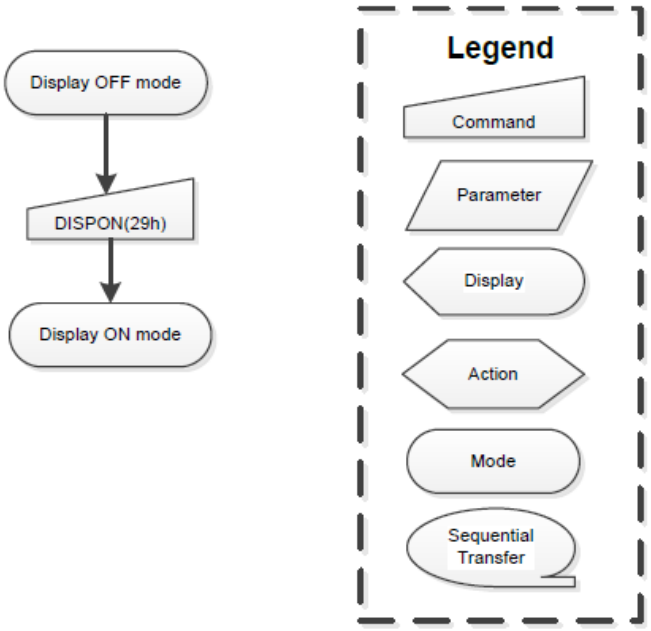


DISPON (2900h): Display ON

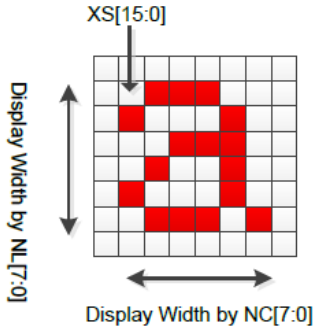
2900H	DISPON											
Instruction	R/W	Address		Parameter								
		MIPI	Other	D15- D8	D7	D6	D5	D4	D3	D2	D1	D0
DISPON	W	29h	2900h	-	No Parameter							
Description	This command forces the display module to start displaying image data.											
Restriction	This command has no effect when display driver is already in *DISPLAY-ON* mode.											

Default	Status	Default Value	
	Power On Sequence	2900h	Display Off
	SW Reset	The same as above	
	HW Reset	The same as above	

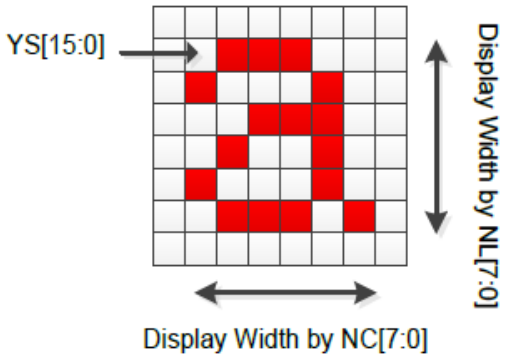
Flow Chart



CASET (2A00h): Column Address Set

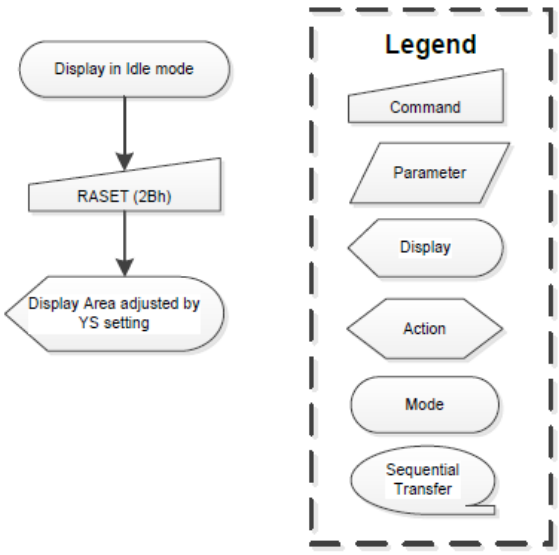
<table>
<tr><td>2A00H</td><td colspan="12">CASET</td></tr>
<tr><td rowspan="2">Instruction</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td colspan="10">Parameter</td></tr>
<tr><td>MIPI</td><td>Other</td><td>D15- D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td rowspan="2">CASET</td><td rowspan="2">R/W</td><td rowspan="2">2Ah</td><td>2A00h</td><td>-</td><td colspan="9">XS[15:8]</td></tr>
<tr><td>2A01h</td><td>-</td><td colspan="9">XS[7:0]</td></tr>
<tr><td>Description</td><td colspan="12">This command indicates display start position of display module in columns.
XS[15:0]: Display line start position.
 
</td></tr>
<tr><td>Restriction</td><td colspan="12">1. XS= 0 + 2N, N=integer
2. Display content can be adjusted by XS, YS, PIXEL_SHIFT_X_COUNT, and PIXEL_SHIFT_Y_COUNT. The constraint is that display content can’t exceed display area. XS should follow the rule as below:
PIXEL_SHIFT_X_DIR=0(Left)
Parameter range= 0 ≤ XS[15:0] + NC[7:0]*8 - PIXEL_SHIFT_X_COUNT*2 ≤ 2568 (A08h)
PIXEL_SHIFT_X_DIR=1(Right)
Parameter range= 0 ≤ XS[15:0] + NC[7:0]*8 + PIXEL_SHIFT_X_COUNT*2 ≤ 2568 (A08h)</td></tr>
<tr><td>Default</td><td colspan="12"><table>
<tr><td>Status</td><td colspan="2">Default Value</td></tr>
<tr><td rowspan="2">Power On Sequence</td><td>2A00h</td><td>00h</td></tr>
<tr><td>2A01h</td><td>00h</td></tr>
<tr><td>SW Reset</td><td colspan="2">The same as above</td></tr>
<tr><td>HW Reset</td><td colspan="2">The same as above</td></tr>
</table></td></tr>
</table>

RASET (2B00h): Row Address Set

2A00H	CASET										
Instruction	R/W	Address		Parameter							
		MIPI	Other	D15- D8	D7	D6	D5	D4	D3	D2	D1	D0
RASET	R/W	2Bh	2B00h	-	YS[15:8]							
			2B01h	-	YS[7:0]							
Description	This command indicates display start position of display module in rows. XS[15:0]: Display line start position.  										
Restriction	1. YS= 0 + 2N, N=integer 2. Display content cane be adjusted by XS, YS, PIXEL_SHIFT_X_COUNT, and PIXEL_SHIFT_Y_COUNT. The constraint is that display content can't exceed display area. YS should follow the rule as below: PIXEL_SHIFT_Y_DIR=0(Up) Parameter range= 0 ≤ YS[15:0] + NL[7:0]*8 - PIXEL_SHIFT_Y_COUNT*2 ≤ 2568 (A08h) PIXEL_SHIFT_Y_DIR=1(Down) Parameter range= 0 ≤ YS[15:0] + NL[7:0]*8 + PIXEL_SHIFT_Y_COUNT*2 ≤ 2568 (A08h)										

Default	Status	Default Value	
	Power On Sequence	2B00h	00h
		2B01h	00h
	SW Reset	The same as above	
	HW Reset	The same as above	

Flow Chart



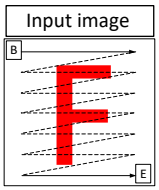
MADCTL (3600h): Set Address Mode

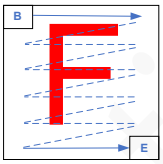
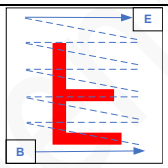
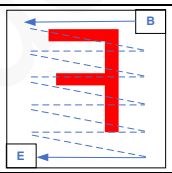
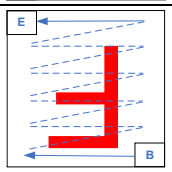
3600H	MADCTL										
Instruction	R/W	Address		Parameter							
		MIPI	Other	D15- D8	D7	D6	D5	D4	D3	D2	D1	D0
MADCTL	R/W	36h	3600h	-	-	-	-	-	-	-	D1	D0

Description

This command set scan direction of source and gate.

Bit	Symbol	Description	Comment
D1	RSMX	Horizontal Flip	1=Normal Display 0= Horizontal Flip
D0	RSMY	Vertical Flip	1= Normal Display 0= Vertical Flip

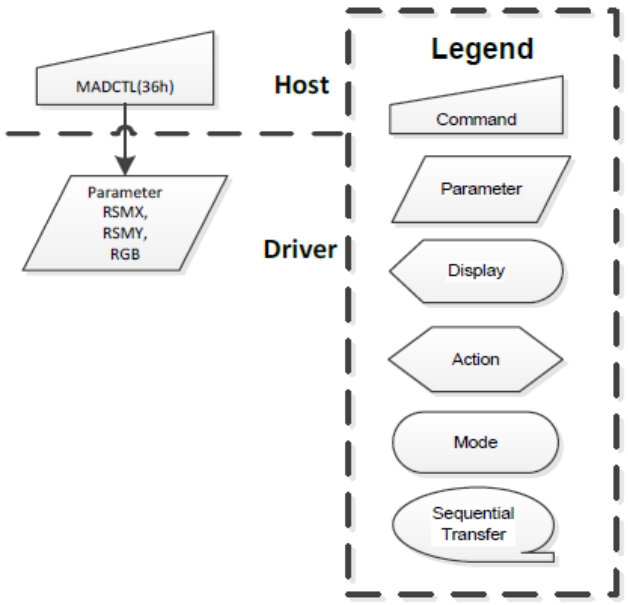


RSMX	RSMY	Display
0	0	
0	1	
1	0	
1	1	

Restriction: -

Default

Status	Default Value	
Power On Sequence	3600h	00h
SW Reset	The same as above	
HW Reset	The same as above	

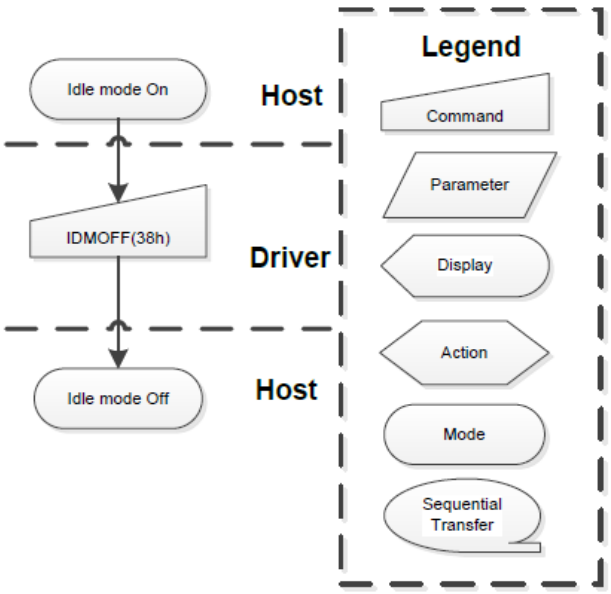
Flow Chart	

IDMOFF (3800h): Idle Mode Off

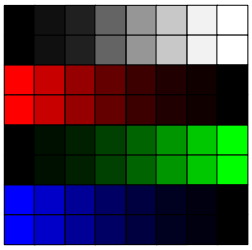
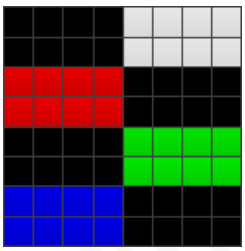
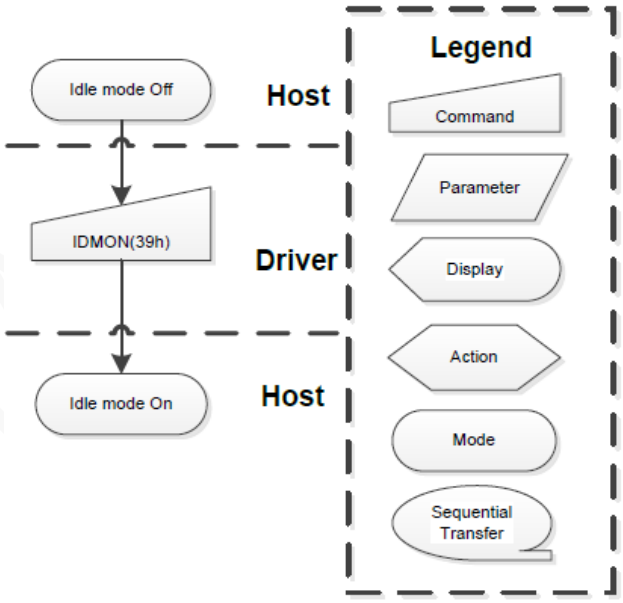
3800H	IDMOFF											
Instruction	R/W	Address		Parameter								
		MIPI	Other	D15- D8	D7	D6	D5	D4	D3	D2	D1	D0
IDMOFF	W	38h	3800h	-	No Parameter							
Description	This command cause display module to exit *Idle* mode.											
Restriction	This command has no effect when display module is not in *Idle* mode.											

Default	Status	Default Value	
	Power On Sequence	3800h	Idle mode off
	SW Reset	The same as above	
	HW Reset	The same as above	

Flow Chart



IDMON (3900h): Idle Mode On

<table>
<tr><td>3900H</td><td colspan="12">IDMON</td></tr>
<tr><td rowspan="2">Instruction</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td colspan="9">Parameter</td></tr>
<tr><td>MIPI</td><td>Other</td><td>D15- D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>IDMON</td><td>W</td><td>39h</td><td>3900h</td><td>-</td><td colspan="9">No Parameter</td></tr>
<tr><td>Description</td><td colspan="12">This command cause display module to enter Idle mode. In the idle mode, color expression is reduced.
Input Image
 
Display
  </td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when display module is already in Idle mode.</td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><td>Status</td><td colspan="2">Default Value</td></tr><tr><td>Power On Sequence</td><td>3900h</td><td>Idle mode off</td></tr><tr><td>SW Reset</td><td colspan="2">The same as above</td></tr><tr><td>HW Reset</td><td colspan="2">The same as above</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="12"> 
</td></tr>
</table>

SCACTRL (6900h): Scaling Up Control

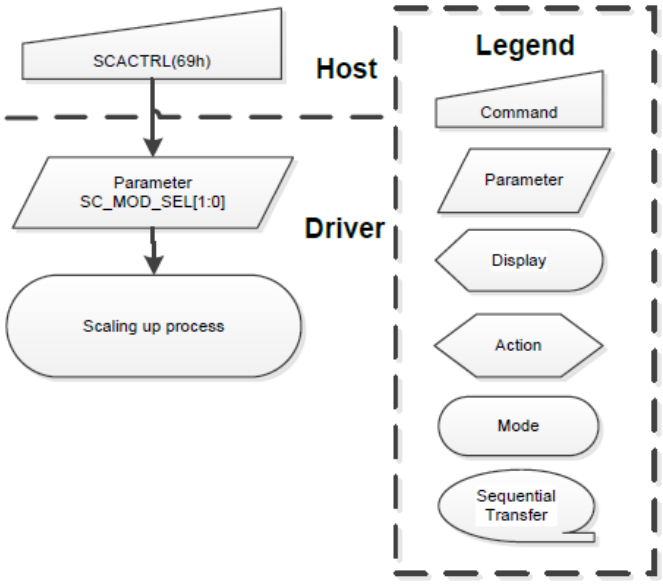
6900H	SCACTRL										
Instruction	R/W	Address		Parameter							
		MIPI	Other	D15- D8	D7	D6	D5	D4	D3	D2	D1	D0
SCACTRL	R/W	69h	6900h	-	-	-	-	-	-	-	D[1:0]	
Description	This command sets operation mode of MIPI clock lane during porch time.											

Bit	Symbol	Description	Comment
D[1:0]	SC_MOD_SEL	Scaling up ratio selection	0= off 1= 2x scaling up 2=1.33x scaling up 3= reserved

Restriction	-

Default	Status	Default Value	
	Power On Sequence	6900h	00h
	SW Reset	The same as above	
	HW Reset	The same as above	

Flow Chart



IFCONF (6B00h): Interface Configure

6900H	IFCONFG										
Instruction	R/W	Address		Parameter							
		MIPI	Other	D15- D8	D7	D6	D5	D4	D3	D2	D1	D0
IFCONFG	R/W	6Bh	6B00h	-	-	-	-	D4	-	-	-	-

Description

PORT_1_2_SEL_CMD1: Set MIPI Port1 or Port2 selection. XOR with PORT1_2_SEL (CMD2 page0 B102 D7).

Bit	Symbol	Description	Comment
D4	PORT1_2_SEL_CMD1	MIPI 1 port or 2 port selection	Refer to the table below

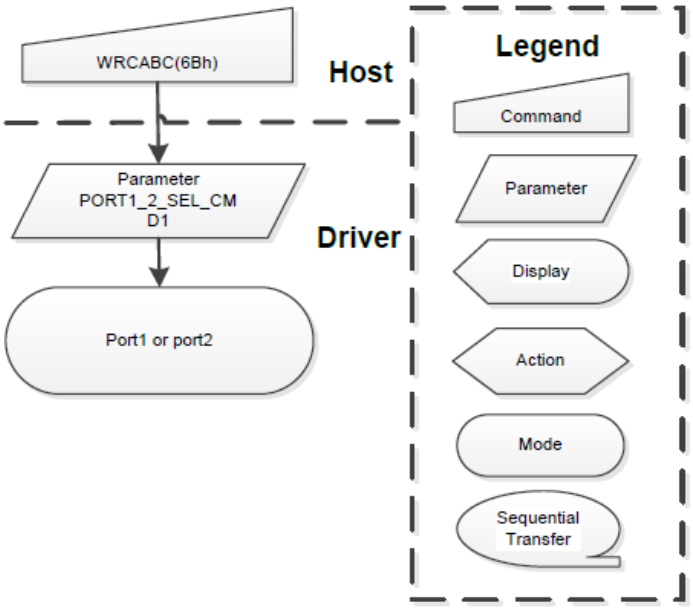
PORT_1_2_SEL_CMD1 (CMD1)	PORT1_2_SEL (CMD2 p0)	MIPI Port Selection
0h	0h	1-Port
0h	1h	2-Port
1h	0h	2-port
1h	1h	1-port

Restriction: -

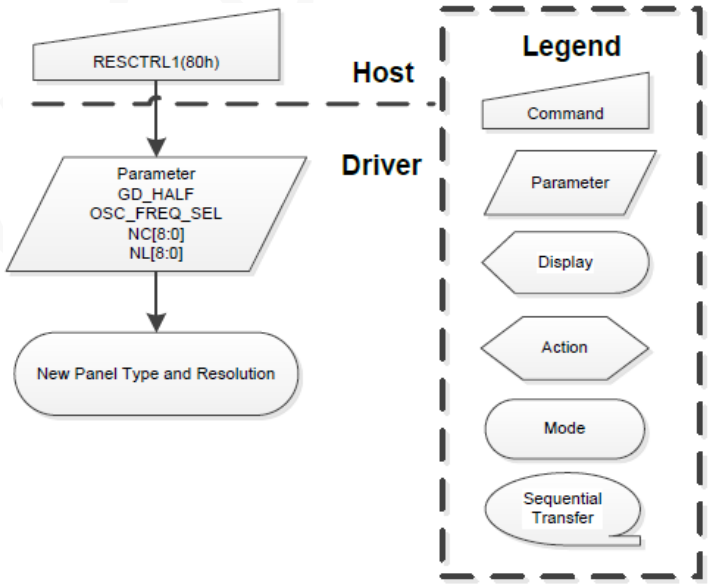
Default

Status	Default Value	
Power On Sequence	6B00h	10h
SW Reset	The same as above	
HW Reset	The same as above	

Flow Chart



RESCTRL1 (8000h): Resolution Control1

<table>
<tr><td>8000H</td><td colspan="12">RESCTRL1</td></tr>
<tr><td rowspan="2">Instruction</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td colspan="9">Parameter</td></tr>
<tr><td>MIPI</td><td>Other</td><td>D15- D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td rowspan="4">RESCTRL 1</td><td rowspan="4">R/W</td><td rowspan="4">80h</td><td>8000h</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>D0</td></tr>
<tr><td>8001h</td><td>-</td><td colspan="8">NC[7:0]</td></tr>
<tr><td>8002h</td><td>-</td><td colspan="8">NL[7:0]</td></tr>
<tr><td>8003h</td><td>-</td><td>-</td><td>-</td><td>-</td><td>NC[8]</td><td>-</td><td>-</td><td>-</td><td>NL[8]</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to set panel type and display resolution.
<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Comment</th></tr>
<tr><td>D0</td><td>OSC_FREQ_SEL</td><td>OSC frequency selection</td><td>0= 69.75MHz
1= 93MHz</td></tr>
<tr><td>D[8:0]</td><td>NC[8:0]</td><td>X-axis resolution</td><td>X-axis resolution= NC[8:0]*8</td></tr>
<tr><td>D[8:0]</td><td>NL[8:0]</td><td>Y-axis resolution</td><td>Y-axis resolution= NL[8:0]*8</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="12">Resolution switch is only valid in SLPIN mode.</td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th>Status</th><th colspan="2">Default Value</th></tr>
<tr><td rowspan="4">Power On Sequence</td><td>8000h</td><td>01h</td></tr>
<tr><td>8001h</td><td>40h</td></tr>
<tr><td>8002h</td><td>40h</td></tr>
<tr><td>8003h</td><td>11h</td></tr>
<tr><td>SW Reset</td><td colspan="2">The same as above</td></tr>
<tr><td>HW Reset</td><td colspan="2">The same as above</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="12"> 
</td></tr>
</table>

11.2 User Command list-Command2 Page1

BCCTR3 (C2h): Brightness Control

8000H	RESCTRL1										
Instruction	R/W	Address		Parameter							
		MIPI	Other	D15- D8	D7	D6	D5	D4	D3	D2	D1	D0
BCCTR3	R/W	C2h	C200h	-	-	-	-	-	-	-	EM_WD_0[9:8]	
			C201h	-	EM_WD_0[7:0]							
			C202h	-	-						EM_WD_1[9:8]	
			C203h	-	EM_WD_1[7:0]							
			C204h		-	-	-	-	-	-	EM_WD_2[9:8]	
			C205h		EM_WD_2[7:0]							
			C206h		-	-	-	-	-	-	EM_WD_3[9:8]	
			C207h		EM_WD_3[7:0]							
			C208h		EM_CYCLE_NUM [1:0]						EM_CYCLE_NUM _IDLE[1:0]	

Description

EM_WD_0~2[9:0]: The percentage of emission duty setting on normal mode. EM_WD_0~2 should keep the same setting.
EM_WD_IDLE[9:0]: The percentage of emission duty setting on IDLE mode. Suggest keep the same setting as EM_WD_0~2.

EM_WD_0[9:0], EM_WD_1[9:0] , EM_WD_2[9:0] , EM_WD_IDLE[9:0]	The percentage of emission duty
0h	1/1024
1h	2/1024
2h	3/1024
…	…
3FEh	1023/1024
3FFh	1024/1024

Restriction

Default

Status	Default Value	
Power On Sequence	C200h	03h
	C201h	FFh
	C202h	03h
	C203h	FFh
	C204h	03h
	C205h	FFh
	C206h	03h
	C207h	FFh
	C208h	82h
SW Reset	The same as above	
HW Reset	The same as above	

12 Reliability

No.	Item	Condition	Judgement
1	High Temperature Storage	80℃ 240hrs	After testing 1.No clearly visible defects or remarkable deterioration of display quality. 2.No function-related abnormalities *The results must be checked after 2hours later under room temperature
2	High Temperature Operating	70℃ 240hrs	
3	Low Temperature Storage	-30℃ 240hrs	
4	Low Temperature Operating	-20℃ 240hrs	
5	High Temperature / Humidity Storage	60℃/90%RH 240hrs	
6	High Temperature / Humidity Operating	60℃/90%RH 240hrs	
7	Thermal Shock	-30℃，0.5hr ⟷ 80℃, 0.5hr, Change time <1min, 100cycles	
8	ESD	Air discharge ±2kv Contact discharge ±1kv	Discharge module :150pf,330Ω Reference standard: IEC61000-4-2 . Class 1 After testing 1.Hard defect should not happen 2.If it would be recovered to normal state after reset, it would be judged as a good state.

13 Inspection Criteria

13.1 Declaration of Incoming Inspection

The customer shall inspect the modules within twenty calendar days since the delivery date（the “inspection period）. The inspection result inspection（accept or reject）shall be recorded in writing, and a copy of this writing document shall be promptly sent to the seller; If the inspection result from buyer does not deliver to the seller within twenty calendar days of the delivery date. The modules shall be considered accepted.

If the customer doesn’t notify the seller within the prescribed time (as above), the buyer's right to reject the module will be invalidated, and the modules will be deemed to have been accepted by the Buyer

13.2 Inspection Sampling Method

Lot size: Quantity per shipment lot per model

Sampling type: Normal inspection, Single sampling

Inspection level: level II

Sampling table: MIL-STD-105D

Acceptable quality level (AQL)

Major defect: AQL=0.4

Minor defect: AQL=1.00

13.3 Inspection Conditions

13.3.1 Ambient conditions:

a. Temperature: 23±3℃

b. Humidity: (55±5) %RH

c. Illumination: Appearance 1000±200 Lux, Display power on inspection＜50 Lux

13.3.2 Viewing distance（Optical device with magnifying lens）

The Module surface shall be close to the optical device, but shall not contact with it, and the inspector’s eyes should be close to the surface of optical device.

13.3.3 Viewing Angle

Front view（with optical device）

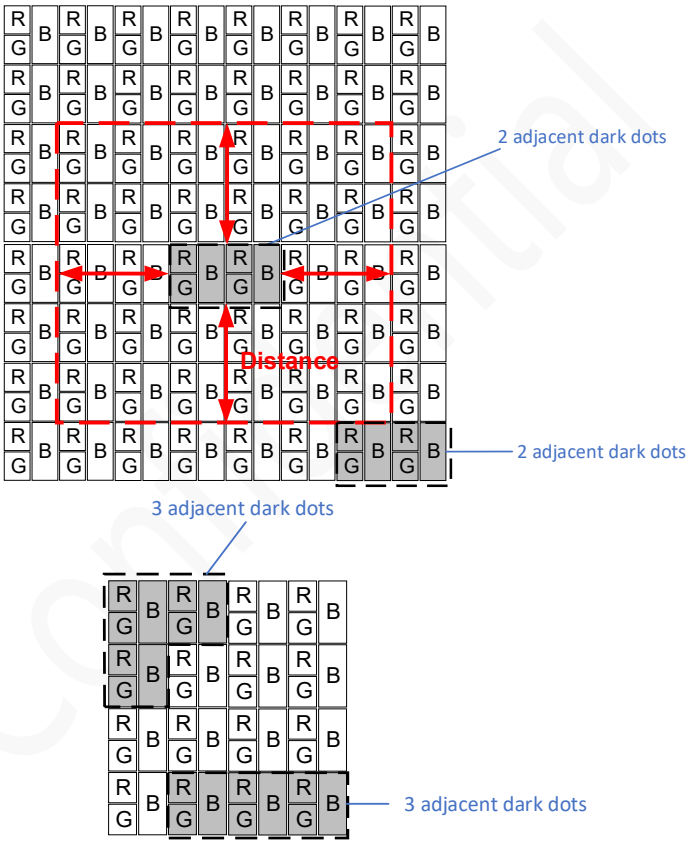
13.4 Criteria

The defects are included functional, display, appearance, etc. Meanwhile the major and minor defects are listed as below.

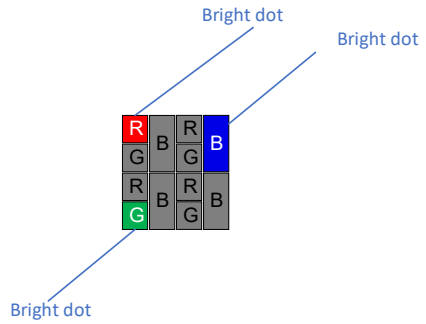
13.4.1 Functional

Item	Level	Criteria
No display	Major	Not allowed
Abnormal display (flickering, abnormal luminance, display image not intact, Block, etc)		

13.4.2 Display

<table>
<tr><th>Item</th><th>Level</th><th>Criteria</th></tr>
<tr><td>Dark dot</td><td>Minor</td><td>
<table>
<tr><th>Case</th><th>Criteria</th><th>Number</th><th>Distance</th></tr>
<tr><td>1 dark dot</td><td>L≤5%Gray255</td><td>≤10</td><td></td></tr>
<tr><td>2 adjacent dark dots</td><td>L≤5%Gray255</td><td>≤2</td><td>≥2pixel</td></tr>
<tr><td>≥3 adjacent dark dots</td><td>L≤5%Gray255</td><td>0</td><td></td></tr>
</table>
• Specify 1 main pixel as 1 dot.


</td></tr>
<tr><td>Bright dot
(Black pattern)</td><td>Minor</td><td>
<table>
<tr><th>Case</th><th>Criteria</th><th>Number</th><th>Distance</th></tr>
<tr><td>Bright dot</td><td>L≤5%Gray255</td><td>ignore</td><td>-</td></tr>
<tr><td>Bright dot</td><td>40%≥L>5%Gray255</td><td>≤2</td><td>≥2pixel</td></tr>
<tr><td>Bright dot</td><td>L>40%Gray255</td><td>0</td><td>-</td></tr>
</table>
• Specify 1 sub pixel as 1 dot.
</td></tr>
</table>

		
Bright line	Major	Not allowed
Dark line	Major	Not allowed
Spot/line caused by foreign body	Minor	Not allowed when visible by naked eyes
Mura/color shift	Minor	If necessary，discuss to define the limit sample

13.4.3 Appearance

Item	Level	Criteria
Stain/dirt	Minor	Not allowed if the defect cannot be cleaned and impact the display effect
Crack	Major	Not allowed
Wafer chipping	Minor	Chipping of the Seal Ring is not allowed. Not damage the pad. Not affect assembly
Wafer corner crack	Minor	Not touch the seal ring
CG chipping	Minor	Not allowed if damaged 1/3 width of sealant
CG corner crack	Minor	Not allowed if damaged 1/3 width of sealant
CG scratch	Minor	Not allowed if the defect impact the display effect
Protective film	Minor	Missing, not allowed Broken, not allowed
FPC dent	Minor	Not allowed metal expose
FPC ACF pin crack	Major	Not allowed
FPC scratch	Major	Not allowed metal expose

14 Warranty

Basically, warranty term is 12 months of reliability characteristics of quality level after the outgoing date in SeeYA, could compensate for defectives which happens within warranty term under condition that the products should be stored or be used as specified under normal condition within the contents of specification.

Otherwise, it is impossible to compensate for defectives when they happen by customer's mistake such as careless handing or circuit change, etc.

15 Packing

To be defined.

16 Environmental Requirements

The product of this model complies with ROHS 2.0 and halogen-free requirement.