

INDUSTRIAL STRENGTH... Start Your Application From YOURITECH

Integration support

Obsolescence Management

PCAP

Embedded Systems

Human Machine Interface

Touch Solutions

Software

Quality Management

Open Frame Monitors

LCD Controller

Research & Development

Firmware

EMC tests

on-site service

Optical Bonding

In-house Manufacturing

Cover glass

System solutions

OEM Solutions

Custom Display

Production
Custom designs
Installation

Mechanical design





FOR MESSRS : _____

DATE : Dec. 16th, 2024

CUSTOMER'S ACCEPTANCE SPECIFICATIONS

TX18D204VM0BVA

Contents

No.	ITEM	SHEET No.	PAGE
1	COVER	7B64PS 2701-TX18D204VM0BVA-4	1-1/1
2	RECORD OF REVISION	7B64PS 2702-TX18D204VM0BVA-4	2-1/2~2/2
3	GENERAL DATA	7B64PS 2703-TX18D204VM0BVA-4	3-1/1
4	ABSOLUTE MAXIMUM RATINGS	7B64PS 2704-TX18D204VM0BVA-4	4-1/1
5	ELECTRICAL CHARACTERISTICS	7B64PS 2705-TX18D204VM0BVA-4	5-1/2~2/2
6	OPTICAL CHARACTERISTICS	7B64PS 2706-TX18D204VM0BVA-4	6-1/2~2/2
7	BLOCK DIAGRAM	7B64PS 2707-TX18D204VM0BVA-4	7-1/1
8	RELIABILITY TESTS	7B64PS 2708-TX18D204VM0BVA-4	8-1/1
9	LCD INTERFACE	7B64PS 2709-TX18D204VM0BVA-4	9-1/7~7/7
10	OUTLINE DIMENSIONS	7B64PS 2710-TX18D204VM0BVA-4	10-1/2~2/2
11	TOUCH PANEL	7B64PS 2711-TX18D204VM0BVA-4	11-1/2~2/2
12	APPEARANCE STANDARD	7B64PS 2712-TX18D204VM0BVA-4	12-1/4~4/4
13	PRECAUTIONS	7B64PS 2713-TX18D204VM0BVA-4	13-1/2~2/2
14	DESIGNATION OF LOT MARK	7B64PS 2714-TX18D204VM0BVA-4	14-1/1

ACCEPTED BY: _____

PROPOSED BY: Oblack Tsai

JDI Taiwan Inc. Kaohsiung Branch	SHEET NO.	7B64PS 2701-TX18D204VM0BVA-4	PAGE	1-1/1
----------------------------------	-----------	------------------------------	------	-------

2. RECORD OF REVISION

DATE	SHEET No.	SUMMARY																																																																																																							
Jan.03,'23	7B64PS 2701 – TX18D204VM0BVA-2 Page 1-1/1	Company logo changed : KOE JDI Group Kaohsiung Opto-Electronics Inc. → JDI Japan Display Inc.																																																																																																							
	7B64PS 2714 – TX18D204VM0BVA-2 Page 14-1/1																																																																																																								
	All page																																																																																																								
		Company name changed: From “KAOHSIUNG OPTO-ELECTRONICS INC.” to “JDI Taiwan Inc. Kaohsiung Branch”																																																																																																							
Sep.02,'24	7B64PS 2703 - TX18D204VM0BVA-3 Page 3-1/1	3.1 DISPLAY FEATURES Revised amorphous silicon TFT → LTPS TFT Module Dimensions 5.5 (D) → 5.75 (D) 0.53W for LCD → 0.84W for LCD																																																																																																							
	7B64PS 2705 – TX18D204VM0BVA-3 Page 5-1/2	5.1 LCD CHARACTERISTICS Revised Power Supply Current Typ. 160 → 255 、Max. 210 → 310 Frame Frequency Max. 67 → - CLK Frequency Max. 160 → 150 Note 4 Delete																																																																																																							
	7B64PS 2706 – TX18D204VM0BVA-3 Page 6-1/2	6. OPTICAL CHARACTERISTICS Add Color Chromaticity Min. & Max.																																																																																																							
	7B64PS 2707 – TX18D204VM0BVA-3 Page 7-1/1	7. BLOCK DIAGRAM Revised																																																																																																							
	7B64PS 2708 – TX18D204VM0BVA-3 Page 8-1/1	8. RELIABILITY TESTS Revised Tip: 200 pF, 250 Ω → Tip: 150 pF, 330 Ω																																																																																																							
	7B64PS 2709 – TX18D204VM0BVA-3 Page 9-3/7	9.4 TIMING CHART Fig. 9.3 Setup & Hold Time Delete																																																																																																							
	7B64PS 2709 – TX18D204VM0BVA-3 Page 9-4/7	9.5 TIMING TABLE Revised A. DE MODE Horizontal CLK Frequency Max. 160 → 150 A. DE MODE Horizontal Cycle Time Max. 2320 → 2248																																																																																																							
7B64PS 2709 – TX18D204VM0BVA-3 Page 9-5/7	9.6 LVDS RECEIVER TIMING Revised <table><tr><th></th><th>Item</th><th>Symbol</th><th>Min.</th><th>Typ.</th><th>Max.</th><th>Unit</th></tr><tr><td rowspan="8">RinX (X=0,1,2,3)</td><td>CLK</td><td>Cycle frequency</td><td>1/t_{CLK}</td><td>135.3</td><td>148.5</td><td>160</td><td>MHz</td></tr><tr><td>0 data position</td><td>IRP0</td><td>1/7* t_{CLK}-0.49</td><td>1/7* t_{CLK}</td><td>1/7* t_{CLK}+0.49</td><td rowspan="6">ns</td></tr><tr><td>1st data position</td><td>IRP1</td><td>-0.49</td><td>0</td><td>+0.49</td></tr><tr><td>2nd data position</td><td>IRP2</td><td>6/7* t_{CLK}-0.49</td><td>6/7* t_{CLK}</td><td>6/7* t_{CLK}+0.49</td></tr><tr><td>3rd data position</td><td>IRP3</td><td>5/7* t_{CLK}-0.49</td><td>5/7* t_{CLK}</td><td>5/7* t_{CLK}+0.49</td></tr><tr><td>4th data position</td><td>IRP4</td><td>4/7* t_{CLK}-0.49</td><td>4/7* t_{CLK}</td><td>4/7* t_{CLK}+0.49</td></tr><tr><td>5th data position</td><td>IRP5</td><td>3/7* t_{CLK}-0.49</td><td>3/7* t_{CLK}</td><td>3/7* t_{CLK}+0.49</td></tr><tr><td>6th data position</td><td>IRP6</td><td>2/7* t_{CLK}-0.49</td><td>2/7* t_{CLK}</td><td>2/7* t_{CLK}+0.49</td><td></td></tr></table> ↓ <table><tr><th></th><th>Item</th><th>Symbol</th><th>Min.</th><th>Typ.</th><th>Max.</th><th>Unit</th></tr><tr><td rowspan="8">RinX (X=0,1,2,3)</td><td>CLK</td><td>Cycle frequency</td><td>1/t_{CLK}</td><td>135.3</td><td>148.5</td><td>160</td><td>MHz</td></tr><tr><td>0 data position</td><td>IRP0</td><td>1/7* t_{CLK}-0.17</td><td>1/7* t_{CLK}</td><td>1/7* t_{CLK}+0.17</td><td rowspan="6">ns</td></tr><tr><td>1st data position</td><td>IRP1</td><td>-0.17</td><td>0</td><td>+0.17</td></tr><tr><td>2nd data position</td><td>IRP2</td><td>6/7* t_{CLK}-0.17</td><td>6/7* t_{CLK}</td><td>6/7* t_{CLK}+0.17</td></tr><tr><td>3rd data position</td><td>IRP3</td><td>5/7* t_{CLK}-0.17</td><td>5/7* t_{CLK}</td><td>5/7* t_{CLK}+0.17</td></tr><tr><td>4th data position</td><td>IRP4</td><td>4/7* t_{CLK}-0.17</td><td>4/7* t_{CLK}</td><td>4/7* t_{CLK}+0.17</td></tr><tr><td>5th data position</td><td>IRP5</td><td>3/7* t_{CLK}-0.17</td><td>3/7* t_{CLK}</td><td>3/7* t_{CLK}+0.17</td></tr><tr><td>6th data position</td><td>IRP6</td><td>2/7* t_{CLK}-0.17</td><td>2/7* t_{CLK}</td><td>2/7* t_{CLK}+0.17</td><td></td></tr></table>		Item	Symbol	Min.	Typ.	Max.	Unit	RinX (X=0,1,2,3)	CLK	Cycle frequency	1/t _{CLK}	135.3	148.5	160	MHz	0 data position	IRP0	1/7* t _{CLK} -0.49	1/7* t _{CLK}	1/7* t _{CLK} +0.49	ns	1st data position	IRP1	-0.49	0	+0.49	2nd data position	IRP2	6/7* t _{CLK} -0.49	6/7* t _{CLK}	6/7* t _{CLK} +0.49	3rd data position	IRP3	5/7* t _{CLK} -0.49	5/7* t _{CLK}	5/7* t _{CLK} +0.49	4th data position	IRP4	4/7* t _{CLK} -0.49	4/7* t _{CLK}	4/7* t _{CLK} +0.49	5th data position	IRP5	3/7* t _{CLK} -0.49	3/7* t _{CLK}	3/7* t _{CLK} +0.49	6th data position	IRP6	2/7* t _{CLK} -0.49	2/7* t _{CLK}	2/7* t _{CLK} +0.49			Item	Symbol	Min.	Typ.	Max.	Unit	RinX (X=0,1,2,3)	CLK	Cycle frequency	1/t _{CLK}	135.3	148.5	160	MHz	0 data position	IRP0	1/7* t _{CLK} -0.17	1/7* t _{CLK}	1/7* t _{CLK} +0.17	ns	1st data position	IRP1	-0.17	0	+0.17	2nd data position	IRP2	6/7* t _{CLK} -0.17	6/7* t _{CLK}	6/7* t _{CLK} +0.17	3rd data position	IRP3	5/7* t _{CLK} -0.17	5/7* t _{CLK}	5/7* t _{CLK} +0.17	4th data position	IRP4	4/7* t _{CLK} -0.17	4/7* t _{CLK}	4/7* t _{CLK} +0.17	5th data position	IRP5	3/7* t _{CLK} -0.17	3/7* t _{CLK}	3/7* t _{CLK} +0.17	6th data position	IRP6	2/7* t _{CLK} -0.17	2/7* t _{CLK}	2/7* t _{CLK} +0.17	
	Item	Symbol	Min.	Typ.	Max.	Unit																																																																																																			
RinX (X=0,1,2,3)	CLK	Cycle frequency	1/t _{CLK}	135.3	148.5	160	MHz																																																																																																		
	0 data position	IRP0	1/7* t _{CLK} -0.49	1/7* t _{CLK}	1/7* t _{CLK} +0.49	ns																																																																																																			
	1st data position	IRP1	-0.49	0	+0.49																																																																																																				
	2nd data position	IRP2	6/7* t _{CLK} -0.49	6/7* t _{CLK}	6/7* t _{CLK} +0.49																																																																																																				
	3rd data position	IRP3	5/7* t _{CLK} -0.49	5/7* t _{CLK}	5/7* t _{CLK} +0.49																																																																																																				
	4th data position	IRP4	4/7* t _{CLK} -0.49	4/7* t _{CLK}	4/7* t _{CLK} +0.49																																																																																																				
	5th data position	IRP5	3/7* t _{CLK} -0.49	3/7* t _{CLK}	3/7* t _{CLK} +0.49																																																																																																				
	6th data position	IRP6	2/7* t _{CLK} -0.49	2/7* t _{CLK}	2/7* t _{CLK} +0.49																																																																																																				
	Item	Symbol	Min.	Typ.	Max.	Unit																																																																																																			
RinX (X=0,1,2,3)	CLK	Cycle frequency	1/t _{CLK}	135.3	148.5	160	MHz																																																																																																		
	0 data position	IRP0	1/7* t _{CLK} -0.17	1/7* t _{CLK}	1/7* t _{CLK} +0.17	ns																																																																																																			
	1st data position	IRP1	-0.17	0	+0.17																																																																																																				
	2nd data position	IRP2	6/7* t _{CLK} -0.17	6/7* t _{CLK}	6/7* t _{CLK} +0.17																																																																																																				
	3rd data position	IRP3	5/7* t _{CLK} -0.17	5/7* t _{CLK}	5/7* t _{CLK} +0.17																																																																																																				
	4th data position	IRP4	4/7* t _{CLK} -0.17	4/7* t _{CLK}	4/7* t _{CLK} +0.17																																																																																																				
	5th data position	IRP5	3/7* t _{CLK} -0.17	3/7* t _{CLK}	3/7* t _{CLK} +0.17																																																																																																				
	6th data position	IRP6	2/7* t _{CLK} -0.17	2/7* t _{CLK}	2/7* t _{CLK} +0.17																																																																																																				

DATE	SHEET No.	SUMMARY																																											
Sep.02,'24	7B64PS 2710 – TX18D204VM0BVA-3 Page 10-1/2	10.1 FRONT VIEW Revised 5.5→5.75																																											
	7B64PS 2711 – TX18D204VM0BVA-3 Page 12-2/4	11.2 LCD APPEARANCE SPECIFICATION Revised <table><tr><td rowspan="10">Dot-Defect (Note 1)</td><td rowspan="5">Bright dot-defect</td><td>Type</td><td>Maximum number</td></tr><tr><td>1 dot</td><td>4</td></tr><tr><td>2 adjacent dot</td><td>1</td></tr><tr><td>3 adjacent dot or above</td><td>Not allowed</td></tr><tr><td>Density</td><td>2(φ 20mm)</td></tr><tr><td rowspan="5">Dark dot-defect</td><td>1 dot</td><td>5</td></tr><tr><td>2 adjacent dot</td><td>2</td></tr><tr><td>3 adjacent dot or above</td><td>Not allowed</td></tr><tr><td>Density</td><td>3(φ 20mm)</td></tr><tr><td>In total</td><td>5</td></tr><tr><td colspan="2">In total</td><td>10</td></tr></table> ↓ <table><tr><td rowspan="7">Dot-Defect (Note 1)</td><td rowspan="2">Bright dot-defect</td><td>Type</td><td>Maximum number</td></tr><tr><td>1 dot</td><td>0</td></tr><tr><td rowspan="5">Dark dot-defect</td><td>1 dot</td><td>5</td></tr><tr><td>2 adjacent dot</td><td>2</td></tr><tr><td>3 adjacent dot or above</td><td>Not allowed</td></tr><tr><td>Density</td><td>3(φ 20mm)</td></tr><tr><td>In total</td><td>5</td></tr></table>	Dot-Defect (Note 1)	Bright dot-defect	Type	Maximum number	1 dot	4	2 adjacent dot	1	3 adjacent dot or above	Not allowed	Density	2(φ 20mm)	Dark dot-defect	1 dot	5	2 adjacent dot	2	3 adjacent dot or above	Not allowed	Density	3(φ 20mm)	In total	5	In total		10	Dot-Defect (Note 1)	Bright dot-defect	Type	Maximum number	1 dot	0	Dark dot-defect	1 dot	5	2 adjacent dot	2	3 adjacent dot or above	Not allowed	Density	3(φ 20mm)	In total	5
	Dot-Defect (Note 1)	Bright dot-defect			Type	Maximum number																																							
1 dot					4																																								
2 adjacent dot					1																																								
3 adjacent dot or above					Not allowed																																								
Density				2(φ 20mm)																																									
Dark dot-defect		1 dot		5																																									
		2 adjacent dot		2																																									
		3 adjacent dot or above		Not allowed																																									
		Density		3(φ 20mm)																																									
		In total	5																																										
In total		10																																											
Dot-Defect (Note 1)	Bright dot-defect	Type	Maximum number																																										
		1 dot	0																																										
	Dark dot-defect	1 dot	5																																										
		2 adjacent dot	2																																										
		3 adjacent dot or above	Not allowed																																										
		Density	3(φ 20mm)																																										
		In total	5																																										
7B64PS 2714 – TX18D204VM0BVA-3 Page 14-1/1	14. DESIGNATION OF LOT MARK Added : <table><tr><th>REV. No</th><th>ITEM</th><th>REMARKS</th></tr><tr><td>B</td><td>Driver ICs and LCD changed</td><td>PCN 1077</td></tr></table>	REV. No	ITEM	REMARKS	B	Driver ICs and LCD changed	PCN 1077																																						
REV. No	ITEM	REMARKS																																											
B	Driver ICs and LCD changed	PCN 1077																																											
Dec.16,'24	7B64PS 2709 – TX18D204VM0BVA-4 Page 9-5/7	9.6 LVDS RECEIVER TIMING Revised Cycle frequency Max. 160 → 150																																											
	7B64PS 2710 – TX18D204VM0BVA-4 Page 10-1/2	10.1 FRONT VIEW Revised 1.4±0.3→1.45±0.3																																											
	7B64PS 2710 – TX18D204VM0BVA-4 Page 10-2/2	10.2 REAR VIEW Revised →																																											
	7B64PS 2712 – TX18D204VM0BVA-4 Page 12-3/4	12.2 LCD APPEARANCE SPECIFICATION Revised Note 1																																											
	7B64PS 2713 – TX18D204VM0BVA-4 Page 13-1/2	13.2 PRECAUTIONS of HANDLING Revised 4) 、 5)																																											

3. GENERAL DATA

3.1 DISPLAY FEATURES

This module is a 7" FHD of 16:9 format LTPS TFT. The pixel format is vertical stripe and sub pixels are arranged as R (red), G (green), B (blue) sequentially. This display is RoHS compliant, COG (chip on glass) technology and LED backlight are applied on this display.

Part Name	TX18D204VM0BVA
Module Dimensions	178.8(W) mm x 115.0(H) mm x 5.75 (D) mm (Except PCB area)
LCD Active Area	155.52(W) mm x 87.48(H) mm
Pixel Pitch	0.081(W) mm x 0.081 (H) mm
Resolution	1920 x 3(RGB)(W) x 1080(H) Dots
Color Pixel Arrangement	R, G, B Vertical Stripe
LCD Type	Transmissive Color TFT; Normally Black
Display Type	Active Matrix
Number of Colors	16.7M Colors
Backlight	Light Emitting Diode (LED)
Weight	174g
Interface	LVDS; 20 pins
Power Supply Voltage	3.3V for LCD; 12V for Backlight
Power Consumption	0.84W for LCD; 2.9W for Backlight
Viewing Direction	Super Wide Version (In-Plane Switching)
Touch Panel	Projected Capacitive type; Cover Glass on ITO Film

4. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit	Remarks
Supply Voltage	V _{DD}	-0.3	4.0	V	-
Input Voltage of Logic	V _I	-0.3	V _{DD} +0.3	V	Note 1
Operating Temperature	T _{op}	-20	70	°C	Note 2
Storage Temperature	T _{st}	-30	80	°C	Note 2
Backlight Input Voltage	V _{LED}	-	15	V	-

Note 1: The rating is defined for the signal voltages of the interface such as CLK and pixel data pairs.

Note 2: The maximum rating is defined as above based on the chamber temperature, which might be different from ambient temperature after assembling the panel into the application. Moreover, some temperature-related phenomenon as below needed to be noticed:

- Background color, contrast and response time would be different in temperatures other than 25°C.
- Operating under high temperature will shorten LED lifetime.

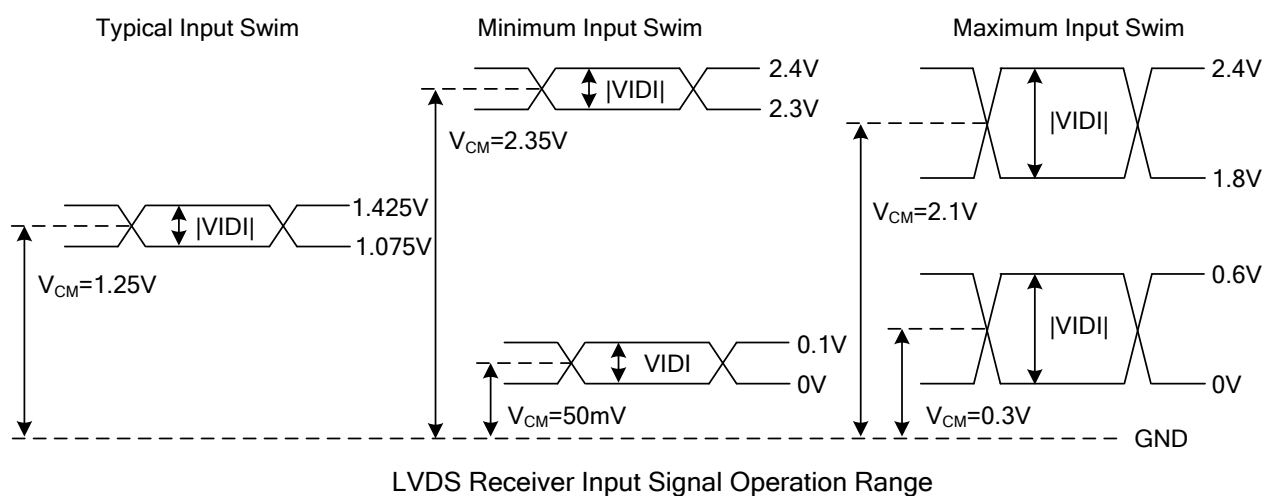
5. ELECTRICAL CHARACTERISTICS

5.1 LCD CHARACTERISTICS

$T_a = 25\text{ }^{\circ}\text{C}$, $V_{SS} = 0\text{V}$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Power Supply Voltage	V_{DD}	-	3.0	3.3	3.6	V	-
Differential Input Voltage for LVDS Receiver Threshold	V_I	"H" level	-	-	+100	mV	Note 1
		"L" level	-100	-	-		
Power Supply Current	I_{DD}	$V_{DD}=3.3\text{V}$	-	255	310	mA	Note 2
Frame Frequency	f_{Frame}	-	-	60	-	Hz	Note 3
CLK Frequency	f_{CLK}	-	135.3	148.5	150	MHz	

Note 1: VCM 1.2V is common mode voltage of LVDS transmitter and receiver.



Note 2: An all white check pattern is used when measuring I_{DD} . f_{Frame} is set to 60 Hz.

Note 3: For LVDS transmitter input.

5.2 BACKLIGHT CHARACTERISTICS

$T_a = 25^\circ\text{C}$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
LED Input Voltage	V_{LED}	-	10.8	12	13.2	V	Note1
LED Forward Current (Dim Control)	I_{LED}	0V; 0% duty	-	242	-	mA	Note 2
		3.3VDC; 100% duty	-	10	-		
LED lifetime	-	$I_{LED} = 242\text{ mA}$	-	40K	-	hrs	Note 3

Note 1: As Fig. 5.1 shown, LED current is constant, 242 mA, controlled by the LED driver when applying 12V.

Note 2: Dimming function can be obtained by applying DC voltage or PWM signal from the display interface CN1. The recommended PWM signal is 1K ~ 10K Hz with 3.3V amplitude.

Note 3: The estimated lifetime is specified as the time to reduce 50% brightness by applying 242 mA at 25°C .

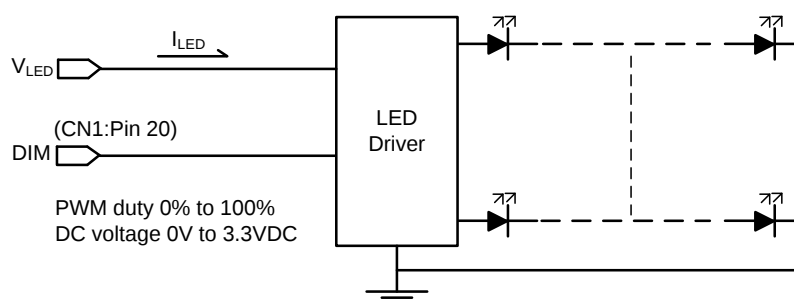


Fig 5.1

6. OPTICAL CHARACTERISTICS

The optical characteristics are measured based on the conditions as below:

- Supplying the signals and voltages defined in the section of electrical characteristics.
- The backlight unit needs to be turned on for 30 minutes.
- The ambient temperature is 25 °C .
- In the dark room less than 100 lx, the equipment has been set for the measurements as shown in Fig 6.1.

$$T_a = 25\text{ }^{\circ}\text{C}, f_{\text{Frame}} = 60\text{ Hz}, V_{\text{DD}} = 3.3\text{V}$$

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Brightness of White		-	$\phi = 0^{\circ}, \theta = 0^{\circ}$, $I_{\text{LED}} = 242\text{ mA}$	400	500	-	cd/m ²	Note 1
Brightness Uniformity		-		70	-	-	%	Note 2,3
Contrast Ratio		CR		500	800	-	-	Note 4
Response Time		$T_r + T_f$	$\phi = 0^{\circ}, \theta = 0^{\circ}$	-	23	-	ms	Note 5
Viewing Angle		θ_x	$\phi = 0^{\circ}, \text{CR} \geq 10$	-	85	-	Degree	Note 6
		$\theta_{x'}$	$\phi = 180^{\circ}, \text{CR} \geq 10$	-	85	-		
		θ_y	$\phi = 90^{\circ}, \text{CR} \geq 10$	-	85	-		
		$\theta_{y'}$	$\phi = 270^{\circ}, \text{CR} \geq 10$	-	85	-		
Color Chromaticity	Red	X	$\phi = 0^{\circ}, \theta = 0^{\circ}$	0.59	0.64	0.69	-	Note 7
		Y		0.27	0.32	0.37		
	Green	X		0.29	0.34	0.39		
		Y		0.55	0.60	0.65		
	Blue	X		0.09	0.14	0.19		
		Y		0.00	0.05	0.10		
	White	X		0.25	0.30	0.35		
		Y		0.26	0.31	0.36		

Note 1: The brightness is measured from the center point of the panel, P5 in Fig. 6.2, for the typical value.

Note 2: The brightness uniformity is calculated by the equation as below:

$$\text{Brightness uniformity} = \frac{\text{Min. Brightness}}{\text{Max. Brightness}} \times 100\%$$

which is based on the brightness values of the 9 points in active area measured by BM-5 as shown in Fig. 6.2.

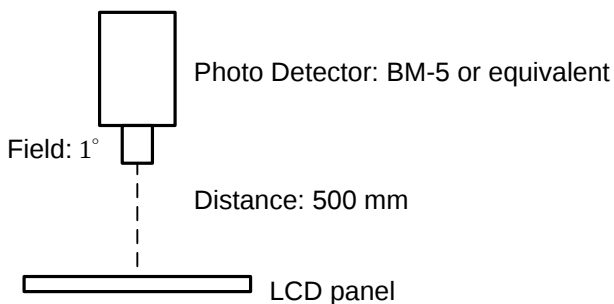


Fig 6.1

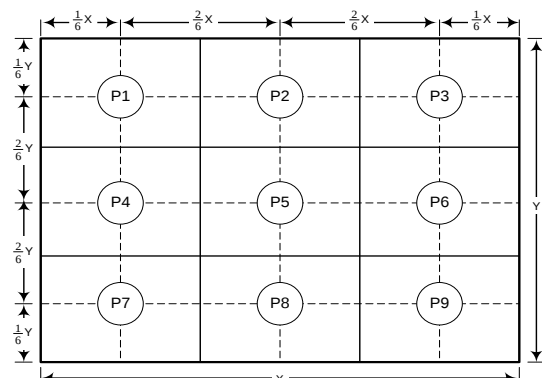


Fig 6.2

Note 3: Continuously operating the test pattern (see below chess pattern Fig.6.3) on display for 2 hours at 25°C then switch to completely white pattern, the previous test pattern shall disappear within 2 seconds.

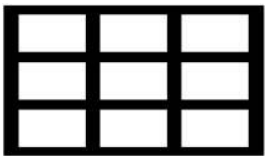


Fig.6.3

Note 4: The Contrast Ratio is measured from the center point of the panel, P5, and defined as the following equation:

$$CR = \frac{\text{Brightness of White}}{\text{Brightness of Black}}$$

Note 5: The definition of response time is shown in Fig. 6.4. The rising time is the period from 10% brightness to 90% brightness when the data is from black to white. Oppositely, Falling time is the period from 90% brightness falling to 10% brightness.

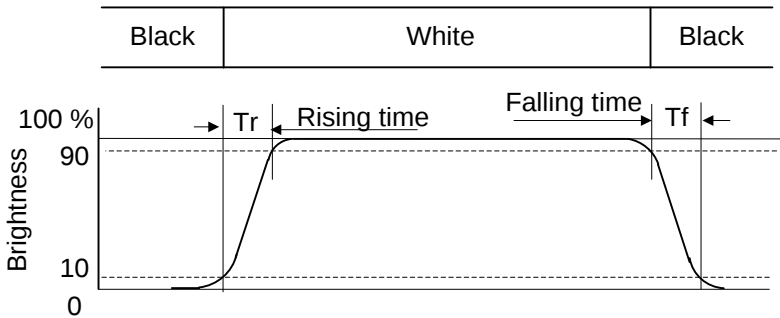


Fig.6.4

Note 6: The definition of viewing angle is shown in Fig. 6.5. Angle ϕ is used to represent viewing directions, for instance, $\phi=270^\circ$ means 6 o'clock, and $\phi=0^\circ$ means 3 o'clock. Moreover, angle θ is used to represent viewing angles from axis Z toward plane XY.

The display is super wide viewing angle version, so that the best optical performance can be obtained from every viewing direction.

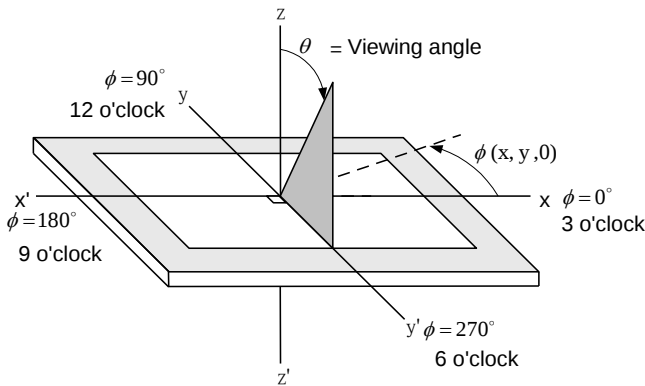
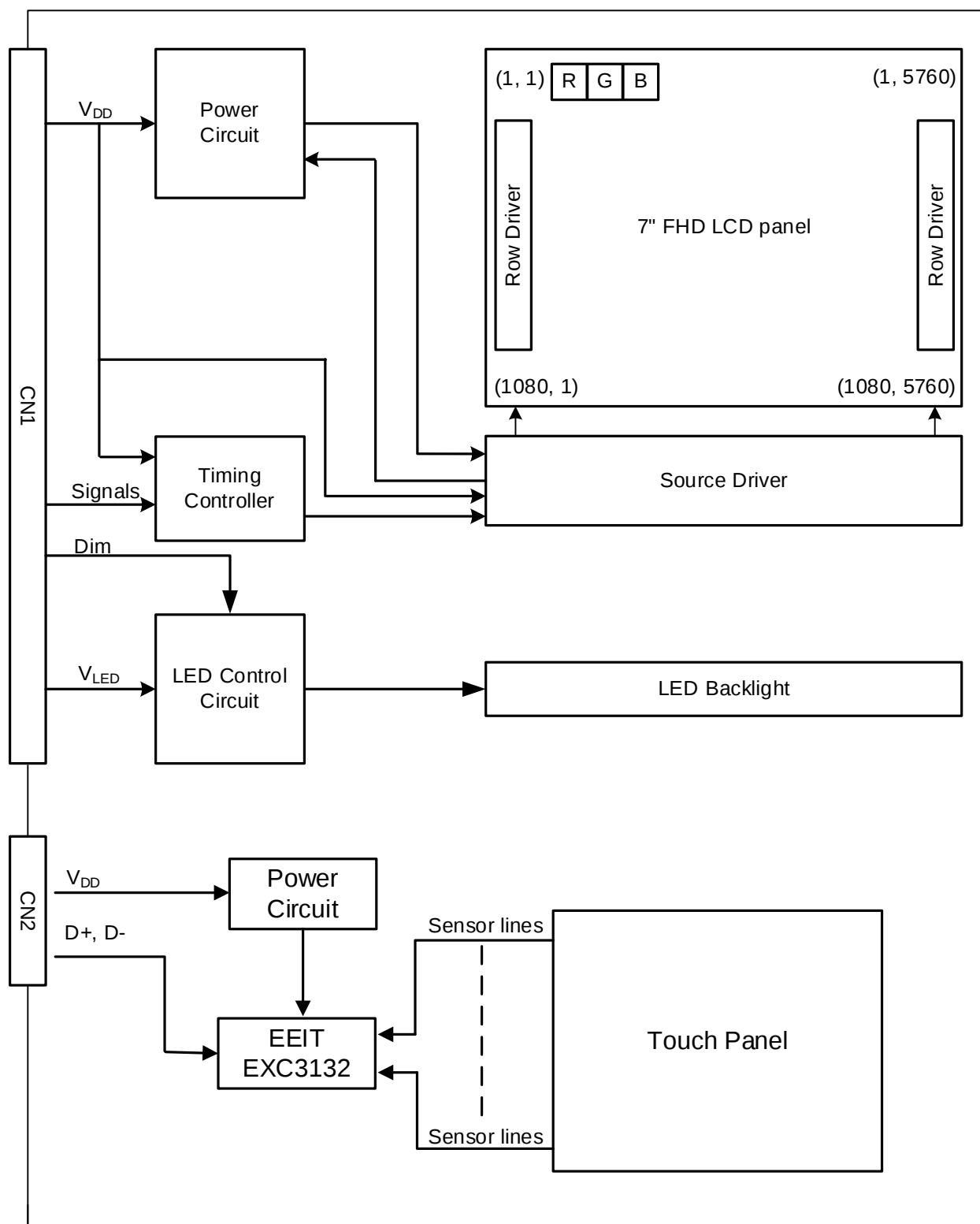


Fig 6.5

Note 7: The color chromaticity is measured from the center point of the panel, P5, as shown in Fig. 6.2.

7. BLOCK DIAGRAM



Note 1: Signals are CLK and pixel data pairs.

8. RELIABILITY TESTS

Test Item	Condition	
High Temperature	1) Operating 2) 70 °C	240 hrs
Low Temperature	1) Operating 2) -20 °C	240 hrs
High Temperature	1) Storage 2) 80 °C	240 hrs
Low Temperature	1) Storage 2) -30 °C	240 hrs
Heat Cycle	1) Operating 2) -20 °C ~70 °C 3) 3hrs~1hr~3hrs	240 hrs
Thermal Shock	1) Non-Operating 2) -35 °C ↔ 85 °C 3) 0.5 hr ↔ 0.5 hr	240 hrs
High Temperature & Humidity	1) Operating 2) 40 °C & 85%RH 3) Without condensation	240 hrs (Note 3)
Vibration	1) Non-Operating 2) 20~200 Hz 3) 2G 4) X, Y, and Z directions	1 hr for each direction
Mechanical Shock	1) Non-Operating 2) 10 ms 3) 50G 4) ±X, ±Y and ±Z directions	Once for each direction
ESD	1) Operating 2) Tip: 150 pF, 330 Ω 3) Air discharge for glass: ± 8KV 4) Contact discharge for metal frame: ± 8KV	1) Glass: 9 points 2) Metal frame: 8 points (Note4)

Note 1: Display functionalities are inspected under the conditions defined in the specification after the reliability tests.

Note 2: The display is not guaranteed for use in corrosive gas environments.

Note 3: Under the condition of high temperature & humidity, if the temperature is higher than 40°C , the humidity needs to be reduced as Fig. 8.1 shown.

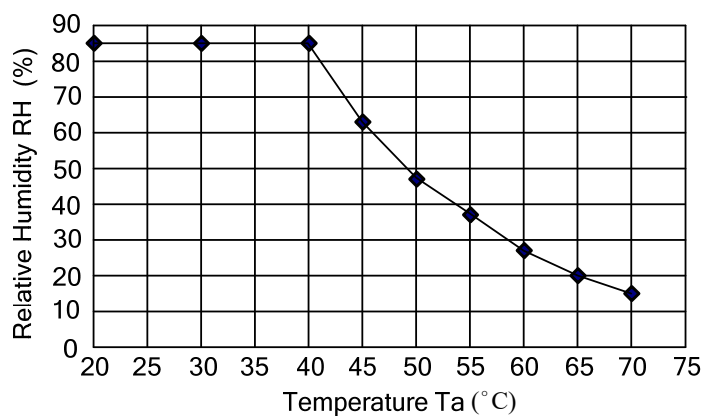


Fig. 8.1

Note 4: All pins of LCD interface (CN1) have been tested by ± 100V contact discharge of ESD under non-operating condition.

9. LCD INTERFACE

9.1 INTERFACE PIN CONNECTIONS

The display interface connector (CN1) is FI-SEB20P-HF13E-E1500 made by JAE and pin assignment is as below:

Pin No.	Symbol	Signal	Pin No.	Symbol	Signal
1	V _{DD}	Power Supply for Logic	11	IN2-	B2~B5, DE
2	V _{DD}		12	IN2+	
3	V _{SS}	GND	13	V _{SS}	GND
4	V _{SS}		14	CLK IN-	Pixel Clock
5	IN0-	R0~R5, G0	15	CLK IN+	
6	IN0+		16	V _{SS}	GND
7	V _{SS}	GND	17	IN3-	R6~R7, G6~G7, B6~B7
8	IN1-	G1~G5, B0~B1	18	IN3+	
9	IN1+		19	V _{LED}	12 VDC
10	V _{SS}	GND	20	DIM	Note 2

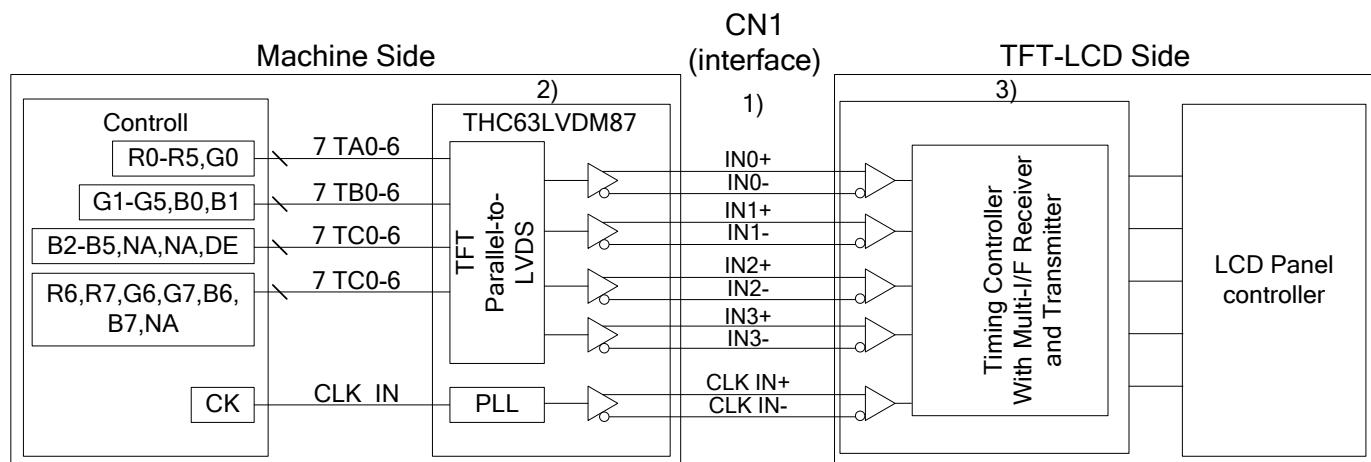
Note 1: IN n- and IN n+ (n=0, 1, 2, 3), CLK IN- and CLK IN+ should be wired by twist-pairs or side-by-side FPC patterns, respectively.

Note 2: Normal brightness: 0V or 0% PWM duty; Brightness control: 0V to 3.3V DC or 0% to 100% PWM duty.

The capacitive touch panel interface FPC: pitch 0.5mm 10pins, and pin assignment is as below:

Pin No.	Symbol	Signal
1	NC	No Connection
2	NC	
3	NC	
4	NC	
5	NC	
6	RST	Reset
7	V _{CC} (5V)	Power Supply
8	D+	USB Signal
9	D-	
10	GND	Ground

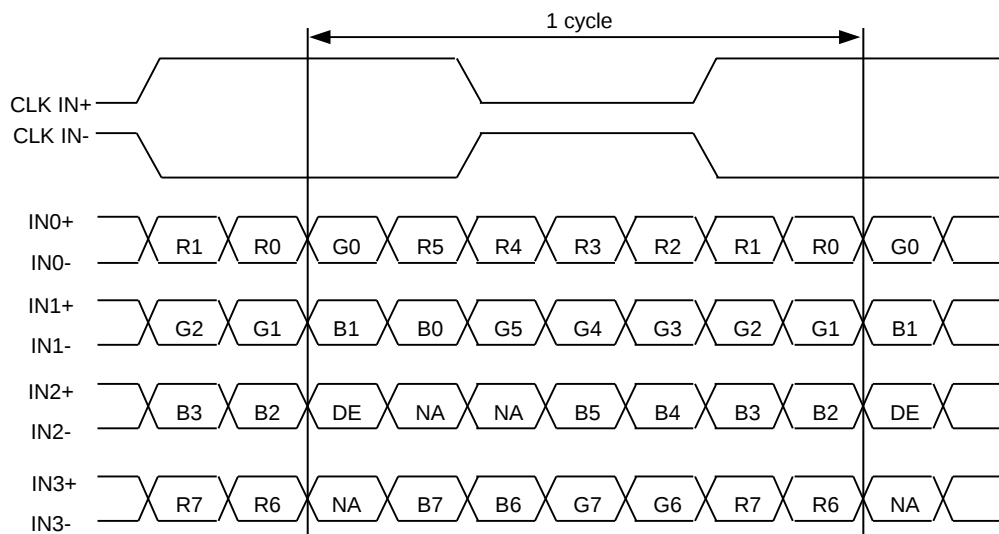
9.2 LVDS INTERFACE



Note 1: LVDS cable impedance should be 100 ohms per signal line when each 2-lines (+, -) is used in differential mode.

Note 2: The recommended transmitter, THC63LVDM87, is made by Thine or equivalent, which is not contained in the module.

9.3 LVDS DATA FORMAT (VESA)



DE: Display Enable

NA: Not Available

9.4 TIMING CHART

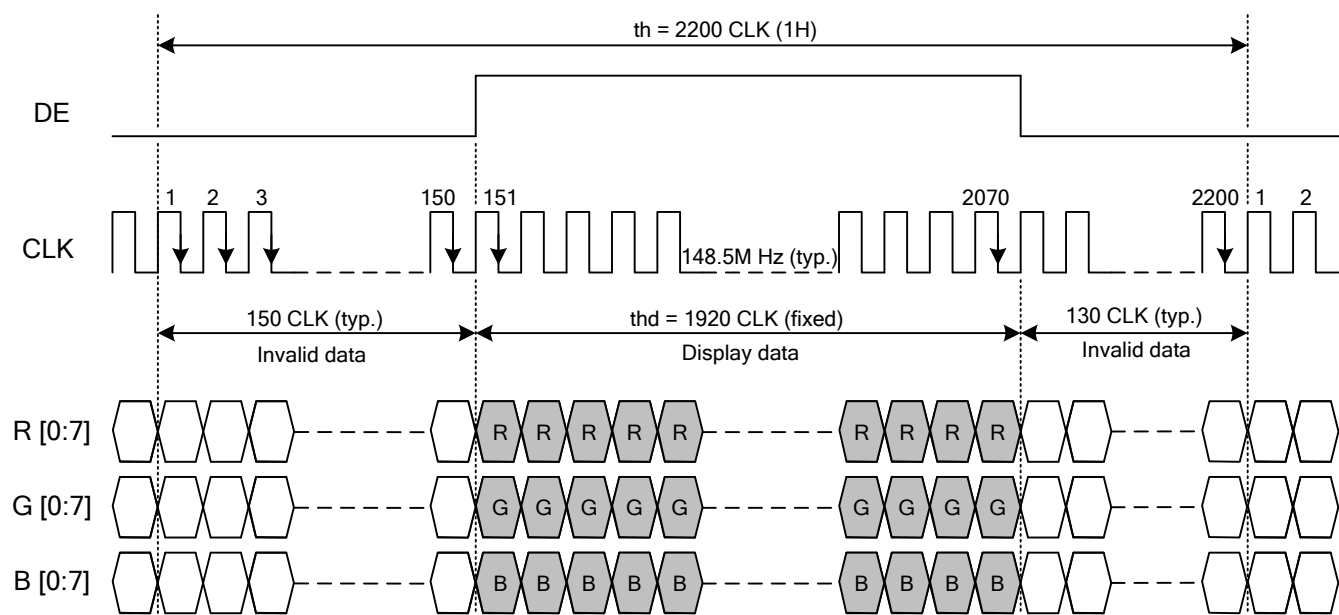


Fig. 9.1 Horizontal Timing

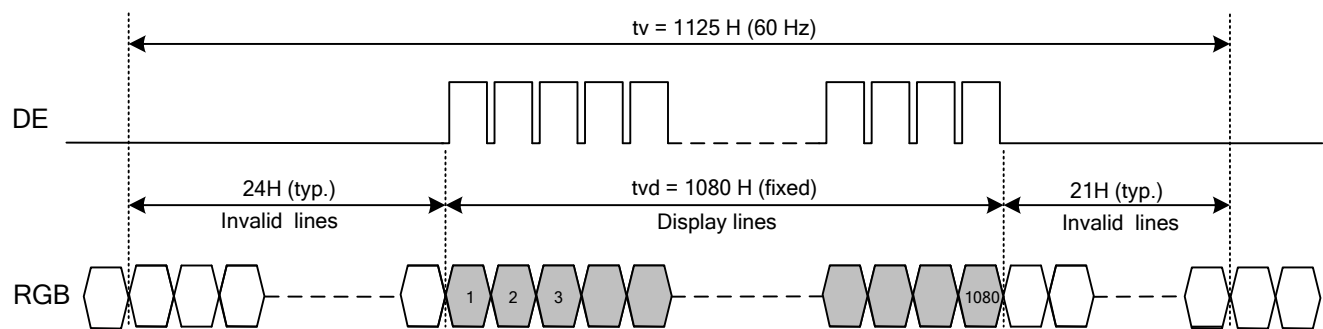


Fig. 9.2 Vertical Timing

9.5 TIMING TABLE

The column of timing sets including minimum, typical, and maximum as below are based on the best optical performance, frame frequency (f_{Frame}) = 60Hz to define.

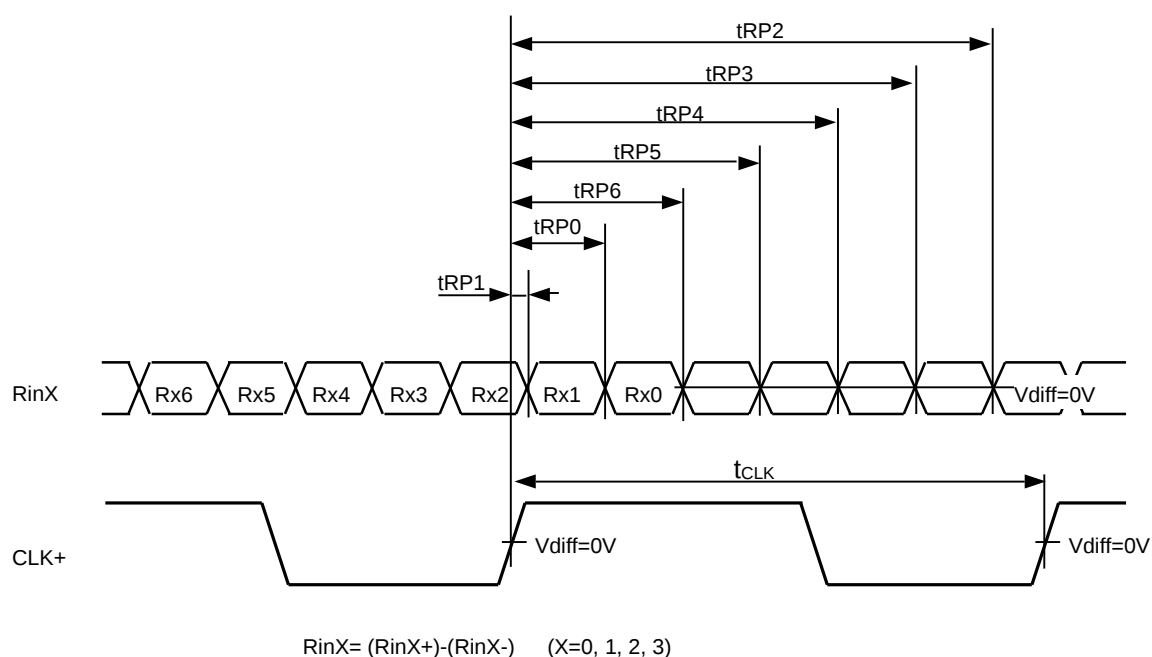
A. DE MODE

Item		Symbol	Min.	Typ.	Max.	Unit
Horizontal	CLK Frequency	fclk	135.3	148.5	150	MHz
	Display Data	thd	1920			CLK
	Cycle Time	th	2050	2200	2248	
Vertical	Display Line	tvd	1080			H
	Cycle Time	tv	1100	1125	1150	

B. CLOCK AND DATA INPUT TIMING

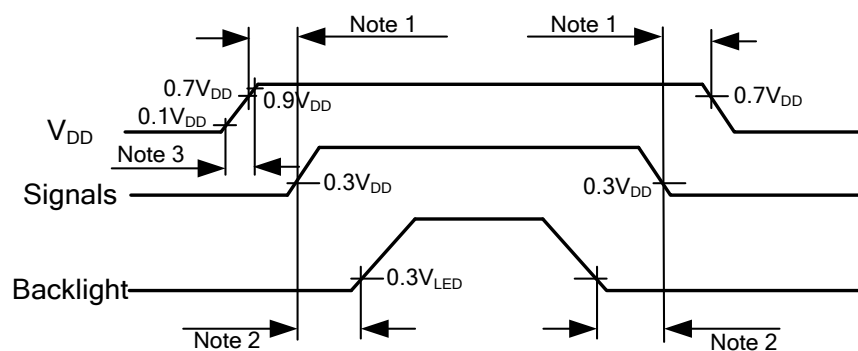
Item		Symbol	Min.	Typ.	Max.	Unit
CLK	Duty	Tcwh	47.5	50	52.5	%
	Cycle Time	Tcph	-	6.74	-	ns
Data	Setup Time	Tdsu	1	-	-	
	Hold Time	Tdhd	1	-	-	
DE	Setup Time	Tesu	1	-	-	
	Hold Time	Tehd	1	-	-	

9.6 LVDS RECEIVER TIMING



	Item	Symbol	Min.	Typ.	Max.	Unit
CLK	Cycle frequency	$1/t_{CLK}$	135.3	148.5	150	MHz
RinX (X=0,1,2,3)	0 data position	$tRP0$	$1/7 * t_{CLK} - 0.17$	$1/7 * t_{CLK}$	$1/7 * t_{CLK} + 0.17$	ns
	1st data position	$tRP1$	-0.17	0	+0.17	
	2nd data position	$tRP2$	$6/7 * t_{CLK} - 0.17$	$6/7 * t_{CLK}$	$6/7 * t_{CLK} + 0.17$	
	3rd data position	$tRP3$	$5/7 * t_{CLK} - 0.17$	$5/7 * t_{CLK}$	$5/7 * t_{CLK} + 0.17$	
	4th data position	$tRP4$	$4/7 * t_{CLK} - 0.17$	$4/7 * t_{CLK}$	$4/7 * t_{CLK} + 0.17$	
	5th data position	$tRP5$	$3/7 * t_{CLK} - 0.17$	$3/7 * t_{CLK}$	$3/7 * t_{CLK} + 0.17$	
	6th data position	$tRP6$	$2/7 * t_{CLK} - 0.17$	$2/7 * t_{CLK}$	$2/7 * t_{CLK} + 0.17$	

9.7 POWER SEQUENCE



Note 1: In order to avoid any damages, V_{DD} has to be applied before all other signals. The opposite is true for power off where V_{DD} has to be remained on until all other signals have been switch off. The recommended time period is 1 second.

Note 2: In order to avoid showing uncompleted patterns in transient state. It is recommended that switching the backlight on is delayed for 1 second after the signals have been applied. The opposite is true for power off where the backlight has to be switched off 1 second before the signals are removed.

Note 3: In order to avoid high Inrush current, V_{DD} rising time need to set more than 0.5ms.

9.8 DATA INPUT for DISPLAY COLOR

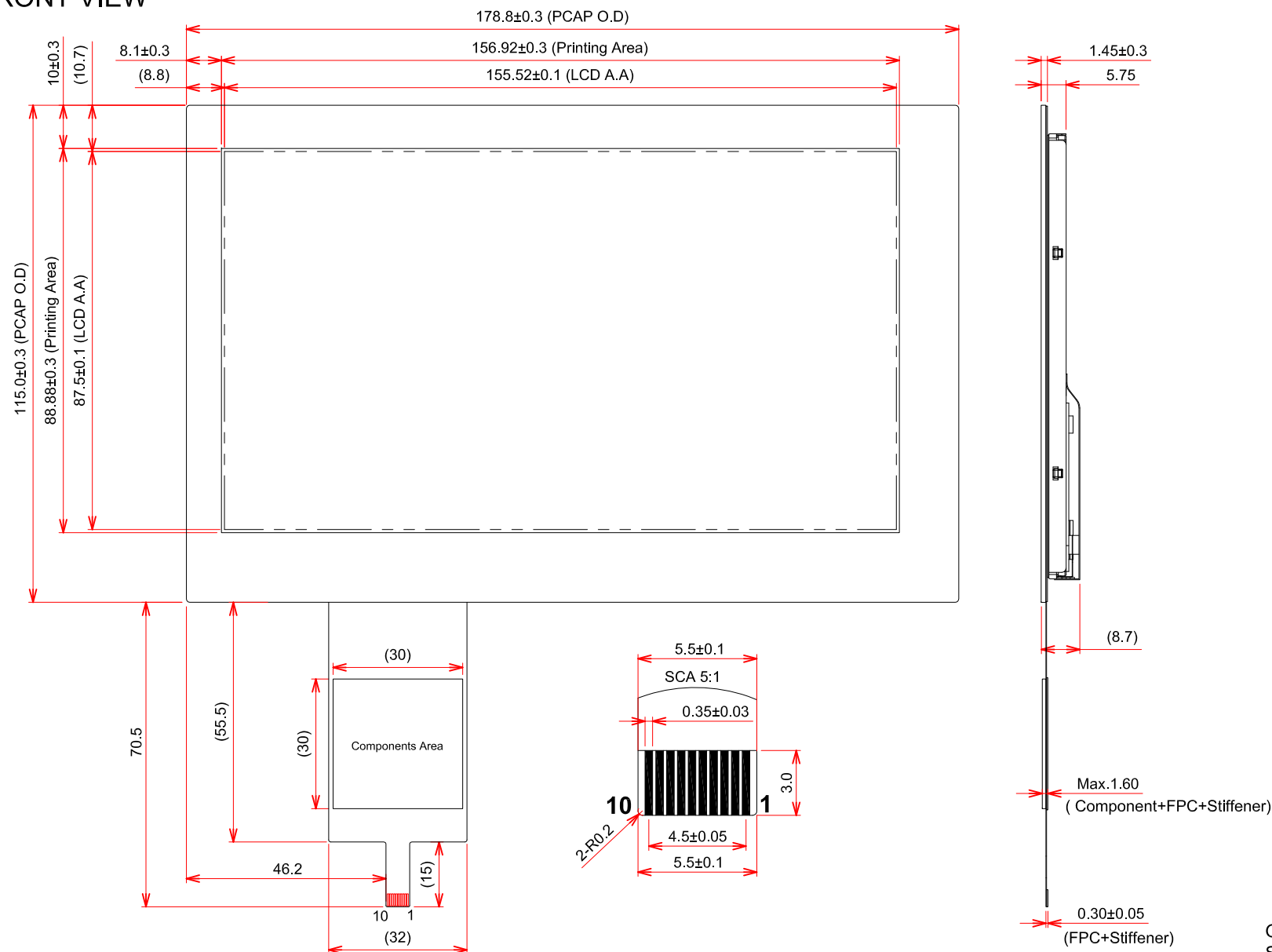
Input color		Red Data								Green Data								Blue Data							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
		MSB								LSB								MSB							
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note 1: Definition of gray scale : Color(n) Number in parenthesis indicates gray scale level. Larger number corresponds to brighter level.

Note 2: Data Signal : 1 : High, 0 : Low

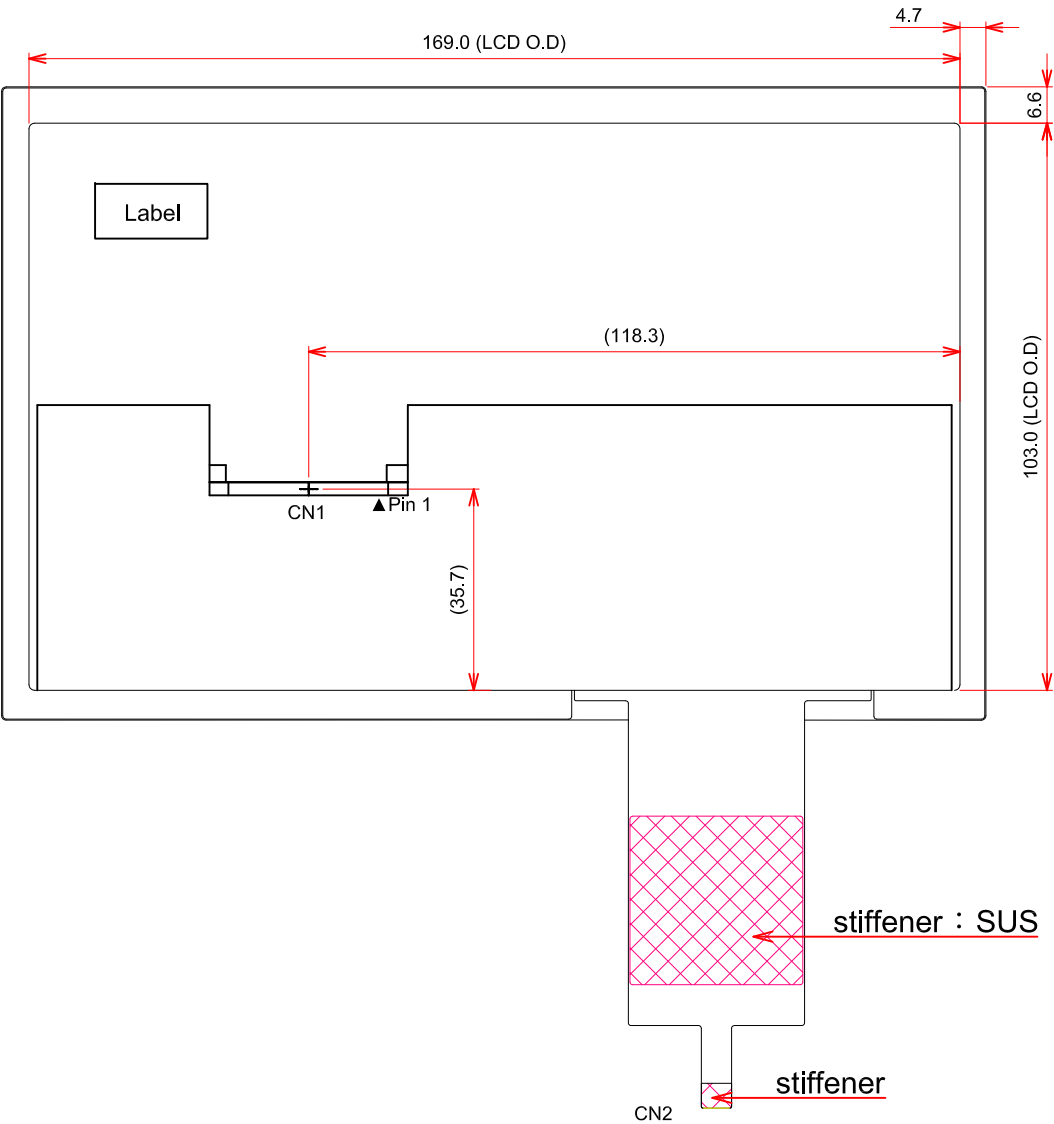
10. OUTLINE DIMENSIONS

10.1 FRONT VIEW



General Tolerance: $\pm 0.5\text{mm}$
Scale : NTS
Unit : mm

10.2 REAR VIEW

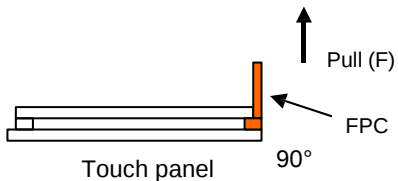
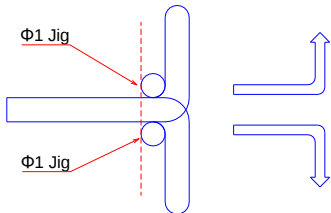


General Tolerance:±0.5mm
Scale : NTS
Unit : mm

11. TOUCH PANEL

The type of touch panel used on this display is capacitive touch panel film, and more characteristics are shown as below:

11.1 MECHANICAL CHARACTERISTICS

Item	Specification	Remarks
Thickness	1.45 ± 0.3 mm	Chemically Strengthened Glass
CG Material	Soda lime	-
Surface Hardness	≥ 7H	-
Input Method	Through a special stylus or finger	-
FPC Peeling Force	5N min.	Peeling upward by 90° 
FPC Bending Resistance	Meet electrical spec. after testing	Bending area Bending degree: 90 Bending radius: R1.0 mm Bending times: 3 times 
Touch Function	10 points	-
Connection insert/remove test	Meet electrical spec. after testing	Insert/remove touch panel FPC for 5 cycles

11.2 ELECTRICAL CHARACTERISTICS

Item	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Power supply voltage	V _{in}	-	3.5	5.0	5.5	V
Crystal Clock	Crystal clock	-	-	12	-	MHZ
V _{IH}	Input high level voltage	V _{DD} =3.3V	V _{DD} -0.8	-	-	V
V _{IL}	Input low level voltage	-	-	-	0.8	V
V _{OH}	Output high voltage	I=2mA	V _{DD} -0.4	-	-	V
V _{OL}	Output low voltage	I=2mA	-	-	0.4	V

11.3 CONTROLLER CHARACTERISTICS

The Capacitive Touch Panel features as below:

- Controller IC is EETI EXC3132
- Interface : USB
- OS : Window7, Android, Linux
- Firmware information :

Mode Name : SIRIUS_3723

Type Name : PCAP3132UR SERIES

Version : 00_TEST1

11.4 ELECTRICAL CHARACTERISTICS

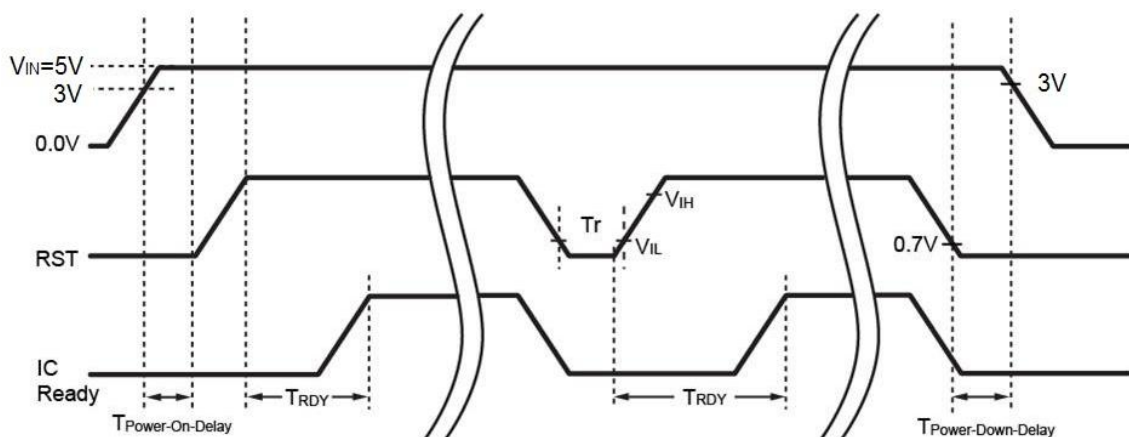


Fig. 11.1 Power On Sequence Diagram

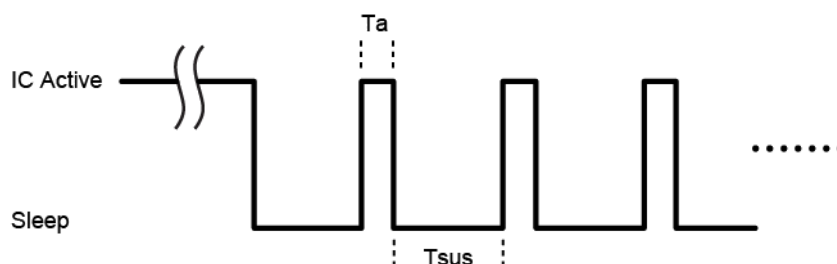


Fig. 11.2 Idle Sequence Diagram

11.5 TIMING TABLE

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Tr	Host pull low period	-	1	-	-	ms
TRDY	IC ready to communication	-	-	65	-	ms
Ta	IC active period	-	-	5	-	ms
Tsus	IC suspend period	-	-	10	-	ms
T _{Power-On-Delay}	Power-on delay	-	100	-	-	us
T _{Power-Down-Delay}	Power-down delay	-	0	-	-	ms
VIL	RST input low Voltage	-	-	-	0.8	V
VIH	RST input high Voltage	-	V _{DD} -0.8	-	-	V

12. APPEARANCE STANDARD

The appearance inspection is performed in a dark room around 100 lx based on the conditions as below:

- The distance between inspector's eyes and display is 30 cm.
- The viewing zone is defined with angle θ shown in Fig. 12.1 The inspection should be performed within 45° when display is shut down. The inspection should be performed within 5° when display is power on.

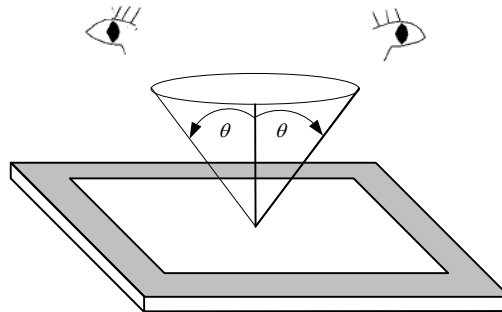


Fig. 12.1

12.1 THE DEFINITION OF LCD ZONE

LCD panel is divided into 2 areas as shown in Fig.12.2 for appearance specification in next section. A zone is the LCD active area (dot area); B zone is the area between A zone and metal frame.

In terms of housing design, B zone is the recommended window area customers' housing should be located in.

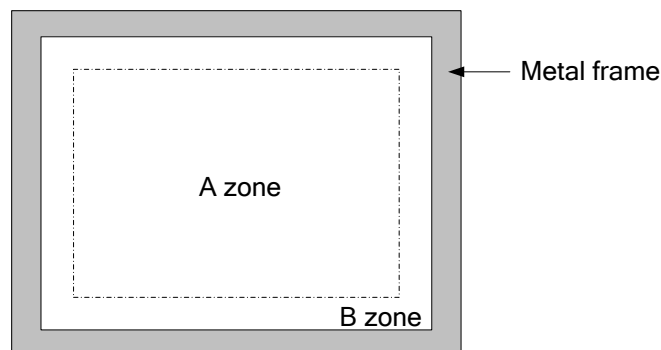


Fig. 12.2

12.2 LCD APPEARANCE SPECIFICATION

The specification as below is defined as the amount of unexpected phenomenon or material in different zones of LCD panel. The definitions of length, width and average diameter using in the table are shown in Fig. 12.3 and Fig. 12.4.

Item	Criteria				Applied zone
Scratches	Length (mm)	Width (mm)	Maximum number	Minimum space	A 、 B
	Ignored	$W\leq 0.01$	Ignored	-	
	$L\leq 40$	$W\leq 0.02$	10	-	
	$L\leq 20$	$W\leq 0.04$	10	-	
	Round (Dot Shape)				
	Average diameter (mm)		Maximum number	Minimum space	
	$D\leq 0.2$		Ignore	-	
	$D\leq 0.4$		10	-	
Dent	Serious one is not allowed				A
Wrinkles in polarizer	Serious one is not allowed				A
Bubbles on polarizer	Average diameter (mm)		Maximum number		A
	$D\leq 0.3$		Ignored		
	$0.3<D\leq 0.5$		10		
	$0.5<D\leq 1.0$		5		
1) Stains 2) Foreign Materials 3) Dark Spot	Filamentous (Line shape)				A 、 B
	Length (mm)	Width (mm)		Maximum number	
	Ignored	$W\leq 0.02$		Ignored	
	$L\leq 2.0$	$W\leq 0.03$		10	
	$L\leq 1.0$	$W\leq 0.06$		10	
	Round (Dot shape)				A 、 B
	Average diameter (mm)		Maximum number	Minimum Space	
	$D\leq 0.3$		Ignored	-	
	$0.3<D\leq 0.5$		5	-	
	$D>0.5$		0	-	
	In total		Filamentous + Round=10		
	Those wiped out easily are acceptable				
Dot-Defect (Note 1)		Type	Maximum number		A
	Bright dot-defect	1 dot	0		
	Dark dot-defect	1 dot	5		
		2 adjacent dot	2		
		3 adjacent dot or above	Not allowed		
		Density	3(φ 20mm)		
		In total	5		

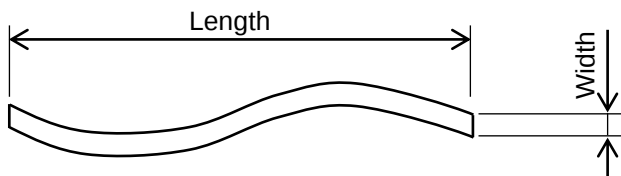


Fig 12.3



Fig 12.4

Note 1: The definitions of dot defect are as below:

- For bright dot-defect, showing black pattern, defect size over 1/2 dot area is defined.
- For dark dot-defect, showing white pattern, defect size over 1/2 dot area is defined.
- The definition of 1-dot-defect is the defect-dot, which is isolated and no adjacent defect-dot.
- The definition of adjacent dot is shown as Fig. 12.5.
- The Density of dot defect is defined in the area within diameter $\phi = 20\text{mm}$.

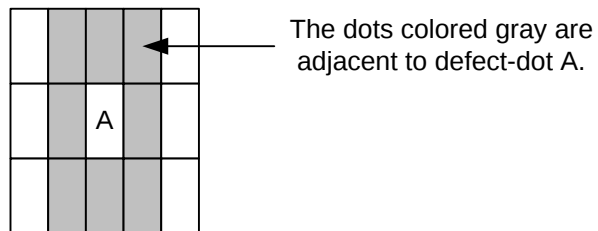


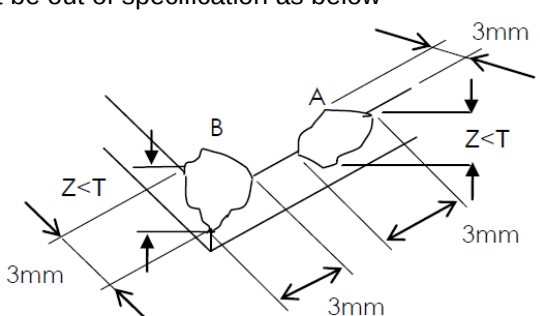
Fig. 12.5

12.3 TOUCH PANEL APPEARANCE SPECIFICATION

The specification as below is defined by the amount of unexpected material in different zones of touch panel.

Item	Criteria			Applied zone
Scratches	Width (mm)	Length (mm)	Maximum number	A
	$W \leq 0.05$	$L \leq 2$	8; Space=5 mm min.	
	$0.05 < W \leq 0.08$	$2 < L \leq 8$	3; Space=5 mm min.	
	$0.08 < W$	$L > 8$	Not allowed	
Foreign materials and spot	Round (Dot shape)			A
	$D \leq 0.15$	Ignored		
	$0.15 < D \leq 0.3$	10; Space=5 mm min.		
	$0.3 < D \leq 0.5$	2; Space=5 mm min.		
	$D < 0.5$	Not allowed		
	Filamentous (Line shape)			
	Width (mm)	Length (mm)	Maximum number	
	$W \leq 0.08$	$L \leq 1$	8; Space=5 mm min.	
	$0.05 < W \leq 0.08$	$1 < L \leq 5$	3; Space=5 mm min.	
	$0.08 < W$	$L > 5$	Not allowed	
Bubble	Round (Dot shape)			A
	Average diameter (mm)		Maximum number	
	$D \leq 0.15$		Ignored	
	$0.15 < D \leq 0.3$		10; Space=5 mm min.	
	$0.3 < D \leq 0.5$		2; Space=5 mm min.	
	$0.5 < D$		Not allowed	
Pin hole on printing area	$D \leq 0.1$	Acceptable		B
	$D > 0.1$	Unacceptable		

The limitation of glass flaw occurred on touch panel is defined in the table as below.

Item	Specifications
Glass chip	Chip size cannot be out of specification as below  Count of Chips: disregard

13. PRECAUTIONS

13.1 PRECAUTIONS of ESD

- 1) Before handling the display, please ensure your body has been connected to ground to avoid any damages by ESD. Also, do not touch display's interface directly when assembling.
- 2) Please remove the protection film very slowly before turning on the display to avoid generating ESD.

13.2 PRECAUTIONS of HANDLING

- 1) In order to keep the appearance of display in good condition; please do not rub any surfaces of the displays by sharp tools harder than 3H, especially touch panel, metal frame and polarizer.
- 2) Please do not pile the displays in order to avoid any scars leaving on the display. In order to avoid any injuries, please pay more attention for the edges of glasses and metal frame, and wear finger cots to protect yourself and the display before working on it.
- 3) Touching the display area or the terminal pins with bare hand is prohibited. This is because it will stain the display area and cause poor insulation between terminal pins, and might affect display's electrical characteristics furthermore.
- 4) Do not use any harmful chemicals such as acetone and toluene to clean display's surfaces.
- 5) Please use soft cloth or absorbent cotton with ethanol or isopropyl alcohol to clean the display by gently wiping. Moreover, when wiping the display, please wipe it by horizontal or vertical direction instead of circling to prevent leaving scars on the display's surface, especially polarizer.
- 6) Please wipe any unknown liquids immediately such as saliva, water or dew on the display to avoid color fading or any permanently damages.
- 7) Maximum pressure to the surface of the display must be less than 1.96×10^4 Pa. If the area of adding pressure is less than 1 cm^2 , the maximum pressure must be less than 1.96N.

13.3 PRECAUTIONS OF OPERATING

- 1) Please input signals and voltages to the displays according to the values defined in the section of electrical characteristics to obtain the best performance. Any voltages over than absolute maximum rating will cause permanent damages to this display. Also, any timing of the signals out of this specification would cause unexpected performance.
- 2) When the display is operating at significant low temperature, the response time will be slower than it at 25°C . In high temperature, the color will be slightly dark and blue compared to original pattern. However, these are temperature-related phenomenon of LCD and it will not cause permanent damages to the display when used within the operating temperature.
- 3) The use of screen saver or sleep mode is recommended when static images are likely for long periods of time. This is to avoid the possibility of image sticking.
- 4) Spike noise can cause malfunction of the circuit. The recommended limitation of spike noise is no bigger than $\pm 100 \text{ mV}$.

JDI Taiwan Inc. Kaohsiung Branch	SHEET NO.	7B64PS 2713-TX18D204VM0BVA-4	PAGE	13-1/2
----------------------------------	--------------	------------------------------	------	--------

13.4 PRECAUTIONS of STORAGE

If the displays are going to be stored for years, please be aware the following notices.

- 1) Please store the displays in a dark room to avoid any damages from sunlight and other sources of UV light.
- 2) The recommended long-term storage temperature is between 10 C° ~35 C° and 55%~75% humidity to avoid causing bubbles between polarizer and LCD glasses, and polarizer peeling from LCD glasses.
- 3) It would be better to keep the displays in the container, which is shipped from JDI, and do not unpack it.
- 4) Please do not stick any labels on the display surface for a long time, especially on the polarizer.

13.5 PRECAUTIONS of TOUCH PANEL

The housing should not cover the active area of touch panel.

JDI Taiwan Inc. Kaohsiung Branch	SHEET NO.	7B64PS 2713-TX18D204VM0BVA-4	PAGE	13-2/2
----------------------------------	--------------	------------------------------	------	--------

14. DESIGNATION of LOT MARK

- 1) The lot mark is showing in Fig.14.1. First 4 digits are used to represent production lot, T represented product of JDI Taiwan, and the last 6 digits are the serial number.

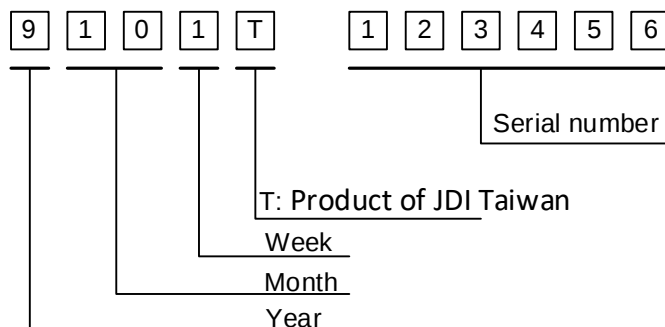


Fig. 14.1

- 2) The tables as below are showing what the first 4 digits of lot mark are shorted for.

Year	Lot Mark	Month	Lot Mark	Month	Lot Mark	Week	Lot Mark
2019	9	Jan.	01	Jul.	07	1~7 days	1
2020	0	Feb.	02	Aug.	08	8~14 days	2
2021	1	Mar.	03	Sep.	09	15~21 days	3
2022	2	Apr.	04	Oct.	10	22~28 days	4
2023	3	May	05	Nov.	11	29~31 days	5
		Jun.	06	Dec.	12		

- 3) Except letters I and O, revision number will be shown on lot mark and following letters A to Z.

REV.No	ITEM	REMARKS
A	-	-
B	Driver ICs and LCD changed	PCN 1077

- 4) The location of the lot mark is on the back of the display shown in Fig. 14.2.

Label example:



Fig. 14.2