Doc. Number:

☐ Tentative Specification
■ Preliminary Specification
☐ Approval Specification

MODEL NO.: WJ015ZE-01A

(1.5PI-OLED)

Customer:

APPROVED BY **SIGNATURE**

Name / Title _____ _____
Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
		鍾惠櫻 2019/11/4

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Revision History

Version	Date	Page	Description
Ver 1.0	Nov.4 ,2019	All	Spec Ver.1.0 was first issued..

1. Purpose

CE Wearable 1.5”手環 is a color active matrix of Organic Light-Emitting Diode (OLED), which uses Low Temperature Poly-silicon (LTPS) as switching devices. This panel has a 1.5 inches diagonally measured active display area with 120 x 240 resolutions. This product is composed of a LTPS-AMOLED panel, Polarizer, driver IC(COF) and FPCa. The following describes the features of this product.

2. Features

- Product Applications: Smart 手環
- 1.5” (diagonal) inch configuration
- 120xRGBX240 resolution
- 180 PPI

3. General Specification

3.1 Physical Specification

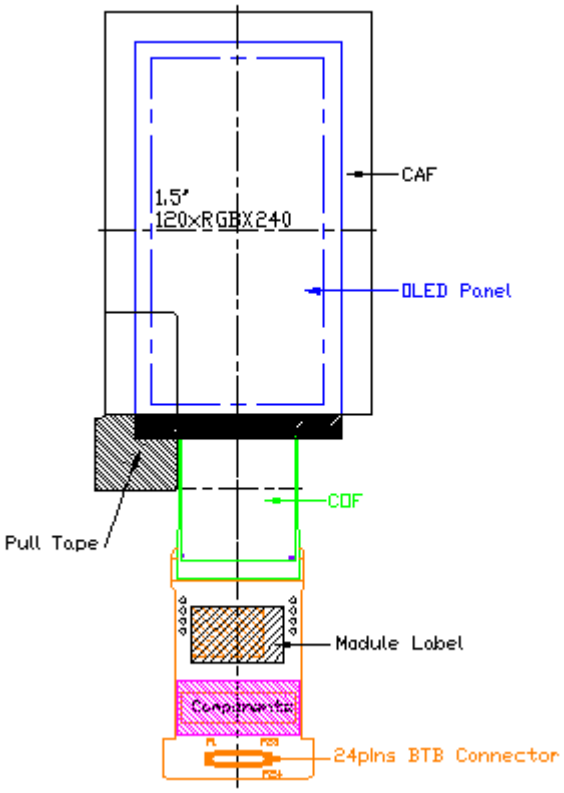
No.	Item	Specification	Unit	Remark
1	Screen Size	1.5	inch	Diameter
2	Display Resolution	120 x 240	pixel	
3	Pixel Pitch	0.141(H) x 0.141(V)	mm	
4	Pixel Configuration	RGB-SBS	--	
5	Color Depth	16.7M	--	
6	Display Type	Color OLED	--	
7	Luminance	350	Cd/m2	Typ
8	Interface Type	SPI/MIPI	--	
9	Power Consumption	Panel power :110	mW	Typ
		IC:14.24	mW	Typ
10	Surface Treatment	Hard coat treating (Glare)	3H	

3.2 Mechanical Specification

Item		Min.	Typ.	Max.	Unit	Note
CAF Area (Carry film)	Horizontal (H)	-	26.12	-	mm	(1)
	Vertical (V)	-	39.54	-	mm	
Module Size (w/oCOF&FPCa& CAF)	Horizontal	19.92	20.12	20.32	mm	
	Vertical	38.74	38.94	39.14	mm	
	Thickness (T)	--	0.71	0.80	mm	
Polarizer Area	Horizontal	19.92	20.12	20.32	mm	
	Vertical	36.34	36.54	36.74	mm	
Active Area	Horizontal	-	16.92	-	mm	
	Vertical	-	33.84	-	mm	
Weight		-	1.1	-	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

3.2.1 Module Appearance

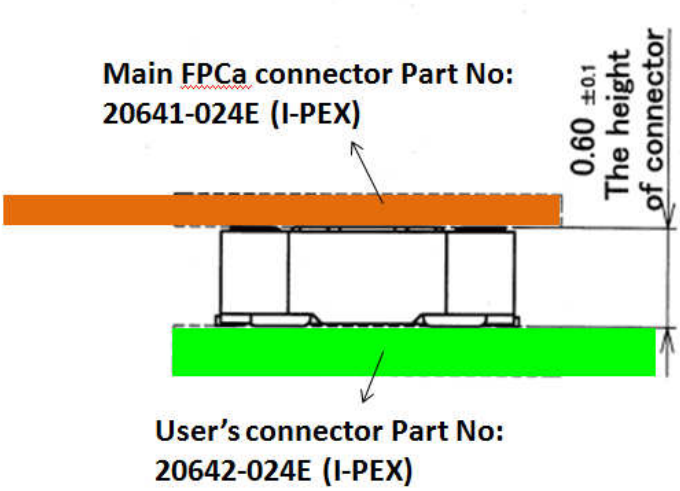


3.2.2 Connector type

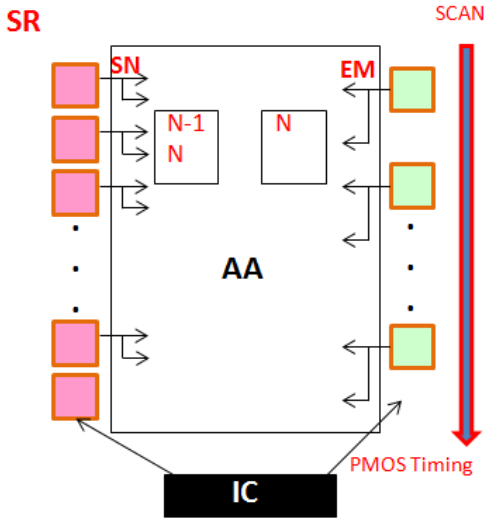
Please refer Appendix Outline Drawing for detail design

Connector Part No: 20641-024E (I-PEX),

User's connector Part No: 20642-024E (I-PEX)



3-3 Panel Scan Direction



4. Absolute Maximum Ratings

(Ta = 25 ± 2℃)

Item	Symbol	Min.	Max.	Unit	Remark
Power Supply Voltage	VCI	-0.3	5.5	V	Power for digital circuit
Interface supply voltage	VDDIO	-0.3	5.5	V	Power for Interface circuit
ELVDD power supply	ELVDD	-	5.0	V	Power for OLED
ELVSS power supply	ELVSS	-5.0	-	V	Power for OLED
Storage temperature	Tstg	-30	+70	℃	
Operating Temperature	Topr	-20	+60	℃	

Note:

(1) All of the voltages listed above are with respective to GND= 0V

(2) Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above.

5. Electrical Specification

5.1 Operating Conditions:

(Ta = 25 ± 2℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Driver driving voltage	VCI	2.7	2.8	3.6	V	(1)
	VDDIO	1.65	1.8	3.3	V	(1)
OLED driving voltage	ELVDD	4.55	4.6	4.65	V	(1)
	ELVSS	-2.35	-2.4	-2.45	V	(1)

Note:

(1) The operation is guaranteed under the recommended operating conditions only. The operation is not guaranteed if a quick voltage change occurs during the operation. To prevent the noise, a bypass capacitor must be inserted into the line closed to the power pin.

5.2 Power Consumption:

(Ta = 25 ± 2℃)

Display Mode	Item	Symbol	Spec	
			Typ	Max
			Current(mA)	Current(mA)
100% Pixel On (Normal mode)	Current of VDDIO	Ivddio	2.0	-
	Current of VCI	Ivci	3.8	-
	Current of ELVSS	Ielvss	15.71	-
50% Pixel On (Normal mode)	Current of VDDIO	Ivddio	2.0	-
	Current of VCI	Ivci	3.8	-
	Current of ELVSS	Ielvss	7.9	-
ALL Pixel Off (Normal mode)	Current of VDDIO	Ivddio	2.0	-
	Current of VCI	Ivci	3.7	-
	Current of ELVSS	Ielvss	0.0	-
ALL Pixel Off (Standby mode)	Current of VDDIO	Ivddio	-	<50uA
	Current of VCI	Ivci	-	<20uA
	Current of ELVSS	Ielvss	-	0

Note: (1) **Power supply**：VDDIO=1.8V VCI=2.8V

(2) **Frame Frequency**：Fframe =60Hz @25degC, Brightness 300nits MIPI CMD mode

(Ta = 25 ± 2℃)

Display Mode	Item	Symbol	Spec	
			Typ	Max
			Current(mA)	Current(mA)
10% Pixel On (Idle mode)	Current of VDDIO	Ivddio	1.8	-
	Current of VCI	Ivci	2.1	-
	Current of ELVSS	Ielvss	0.1	-

Note:

(1) **Power supply**：VDDIO=1.8V VCI=2.8V

(2) **Frame Frequency**：Frame =15Hz @25degC, Brightness 35nits MIPI CMD mode

6. DC Characteristics

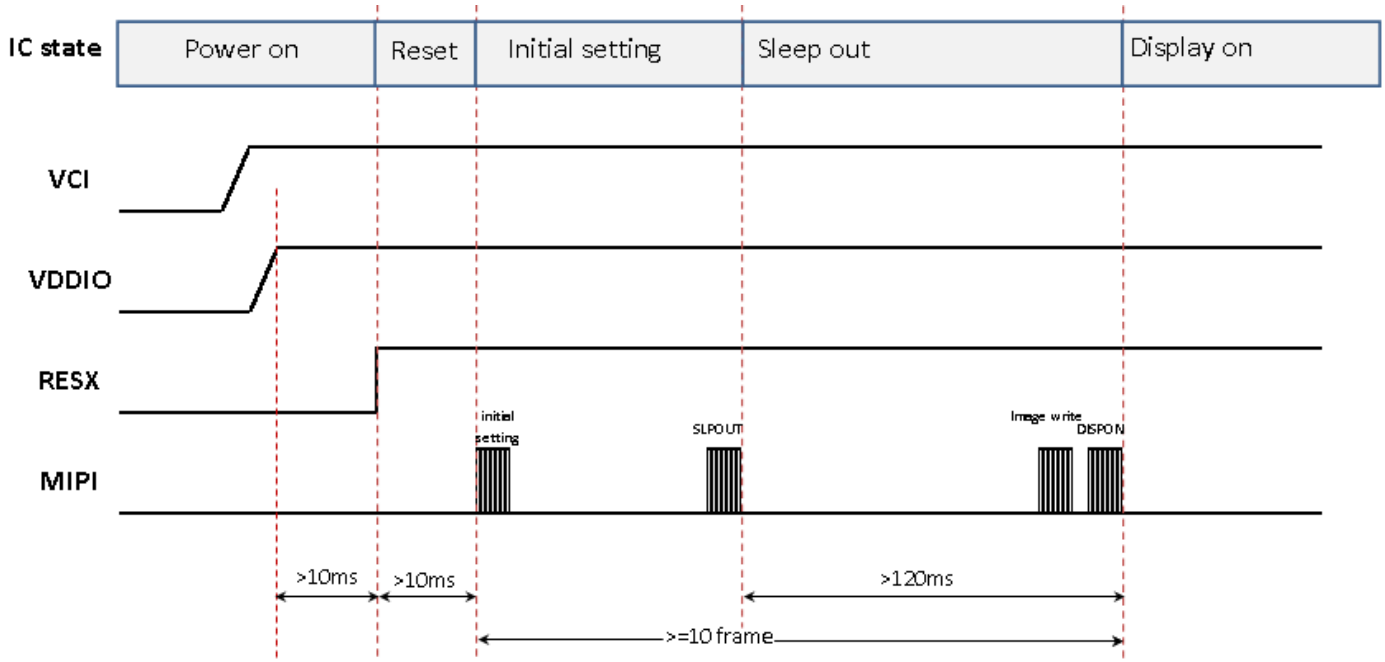
6.1 Parameter

(Ta = 25 ± 2℃)

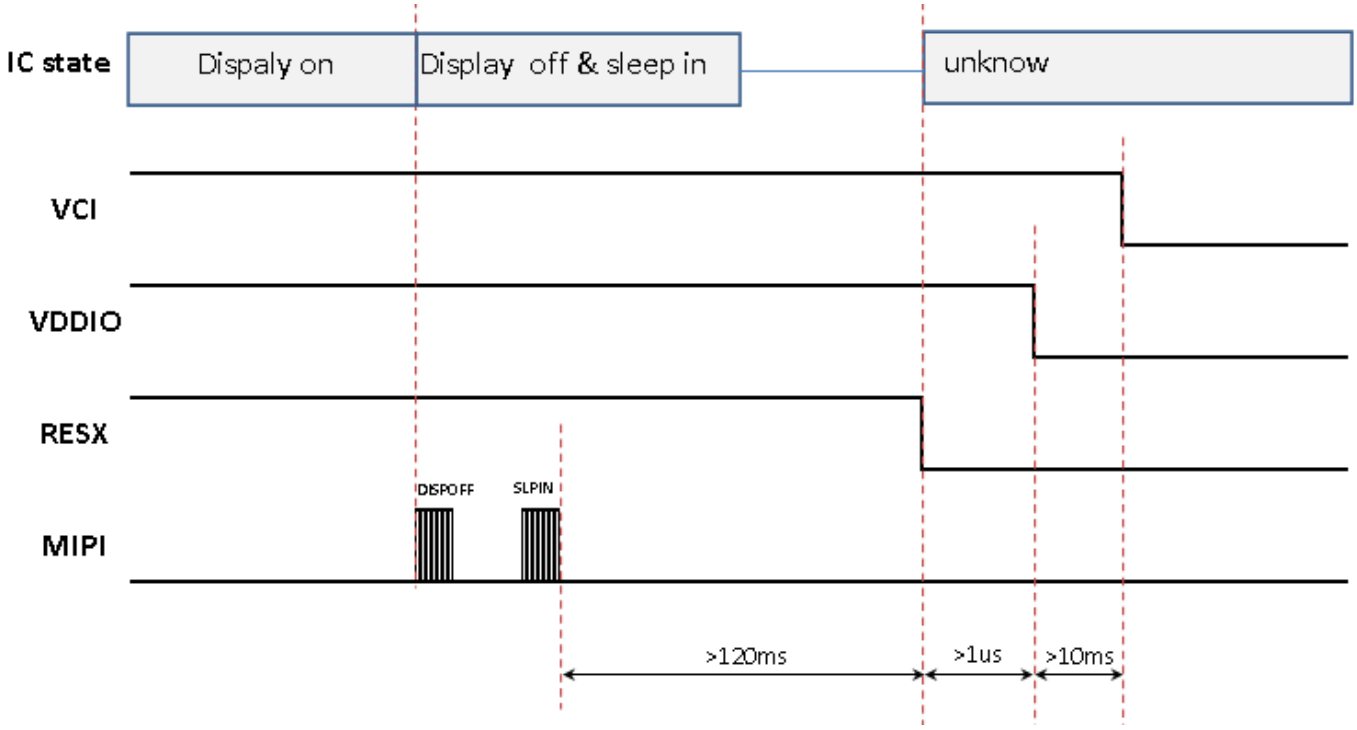
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
High Level Input Signal Voltage	VIH	VDDIO=1.65~3.3V	0.8xVDDIO	-	VDDIO	V	
Low Level Input Signal Voltage	VIL	VDDIO=1.65~3.3V	0	-	0.2xVDDIO	V	
High Level Output Signal Voltage	VOH	VDDIO=1.65~3.3V	0.8xVDDIO	-	VDDIO	V	
Low Level Output Signal Voltage	VOL	VDDIO=1.65~3.3V	0-8	-	0.2xVDDIO	V	

6.2 Operating Power Sequence

6.2.1 Power on sequence



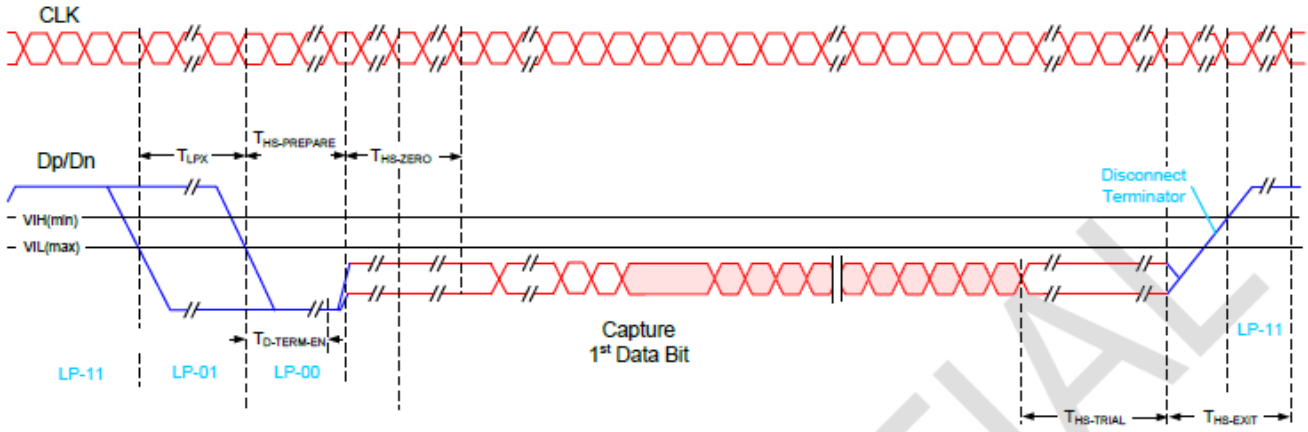
Power off sequence



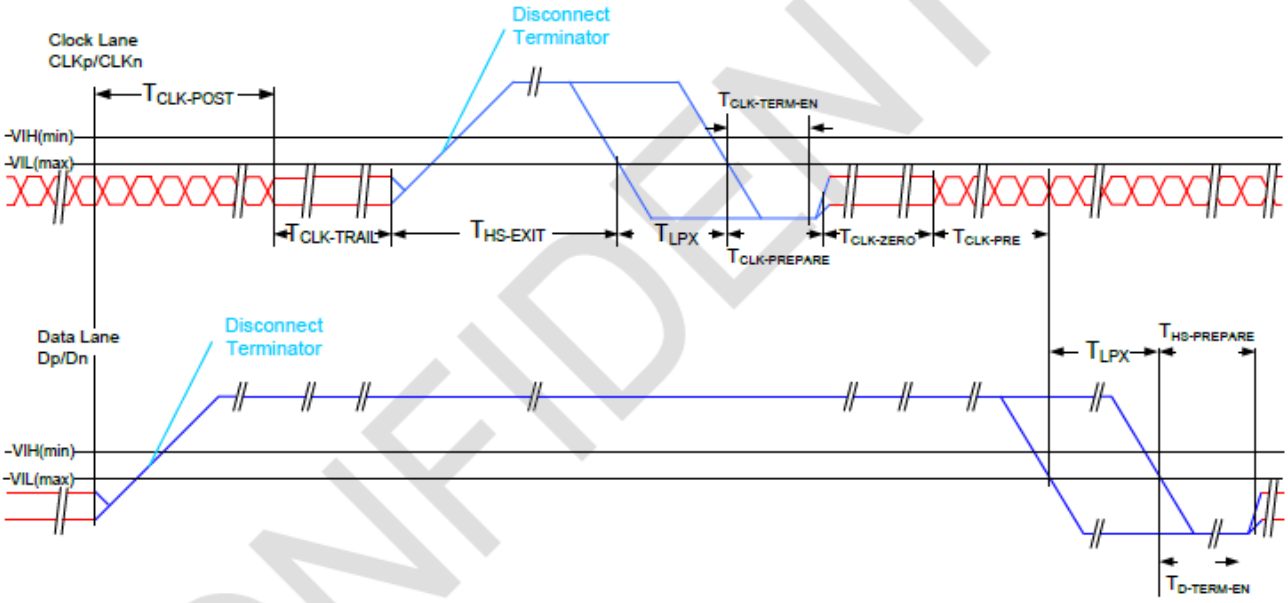
7. AC Characteristics

7.1 MIPI Interface Characteristics

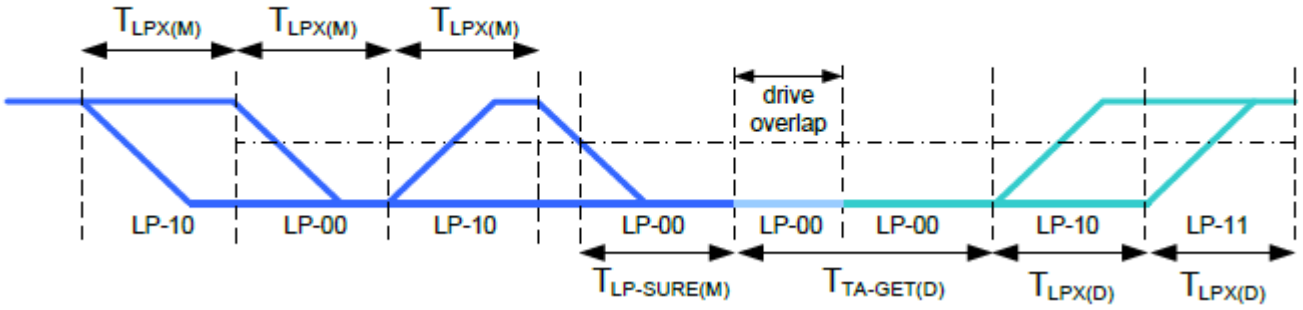
HS Data Transmission Burst



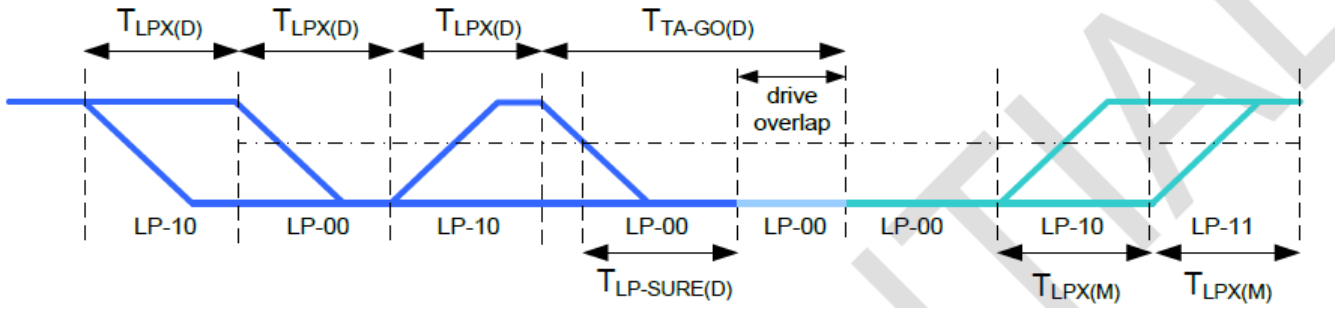
➢ HS clock transmission



Turnaround Procedure



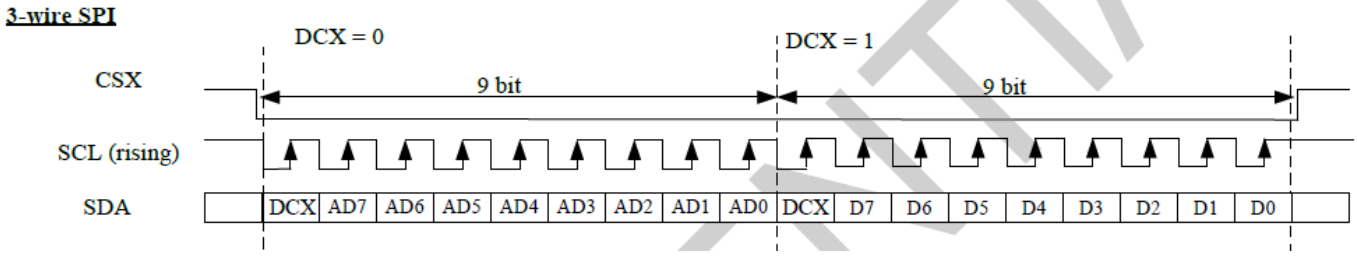
Bus turnaround (BAT) from MPU to display module timing



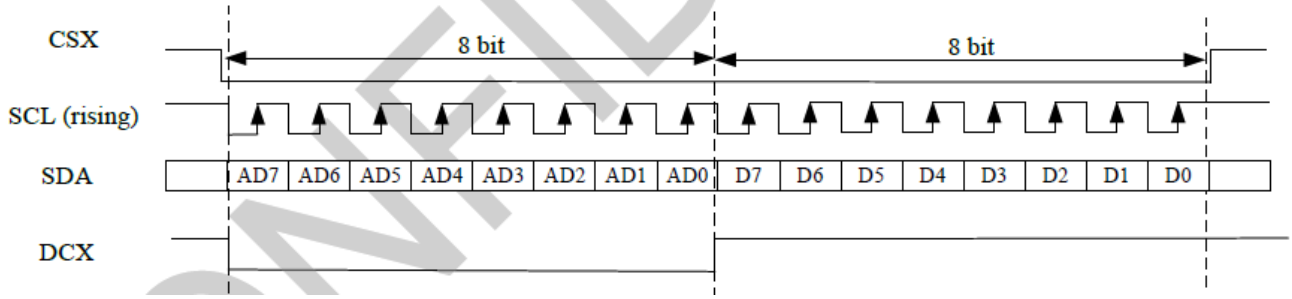
Timing Parameters: Parameter	Description	Min	Typ	Max	Unit
TCLK-POST	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of TCLK-TRAIL .	60ns + 52*UI			ns
TCLK-TRAIL	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
THS-EXIT	Time that the transmitter drives LP-11 following a HS burst.	300			ns
TCLK-TERM-EN	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX .	Time for Dn to reach VTERM-EN		38	ns
TCLK-PREPARE	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
TCLK-PRE	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI
TCLK-PREPARE + TCLK-ZERO	TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns

TD-TERM-EN	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX .	Time for Dn to reach VTERM-EN		35 ns +4*UI	
THS-PREPARE	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns + 4*UI		85 ns + 6*UI	ns
THS-PREPARE + THS-ZERO	THS-PREPARE + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145ns + 10*UI			ns
THS-TRAIL	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	60ns+4*UI			ns
TLPX(M)	Transmitted length of any Low-Power state period of MCU to display module	50		150	ns
TTA-SURE(M)	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	TLPX(M)		2*TLPX(M)	ns
TLPX(D)	Transmitted length of any Low-Power state period of display module to MCU	50		150	ns
TTA-GET(D)	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround.	5*TLPX(D)			ns
TTA-GO(D)	Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround.	4*TLPX(D)			ns
TTA-SURE(D)	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	TLPX(D)		2*TLPX(D)	ns

7.2 SPI Interface Characteristics

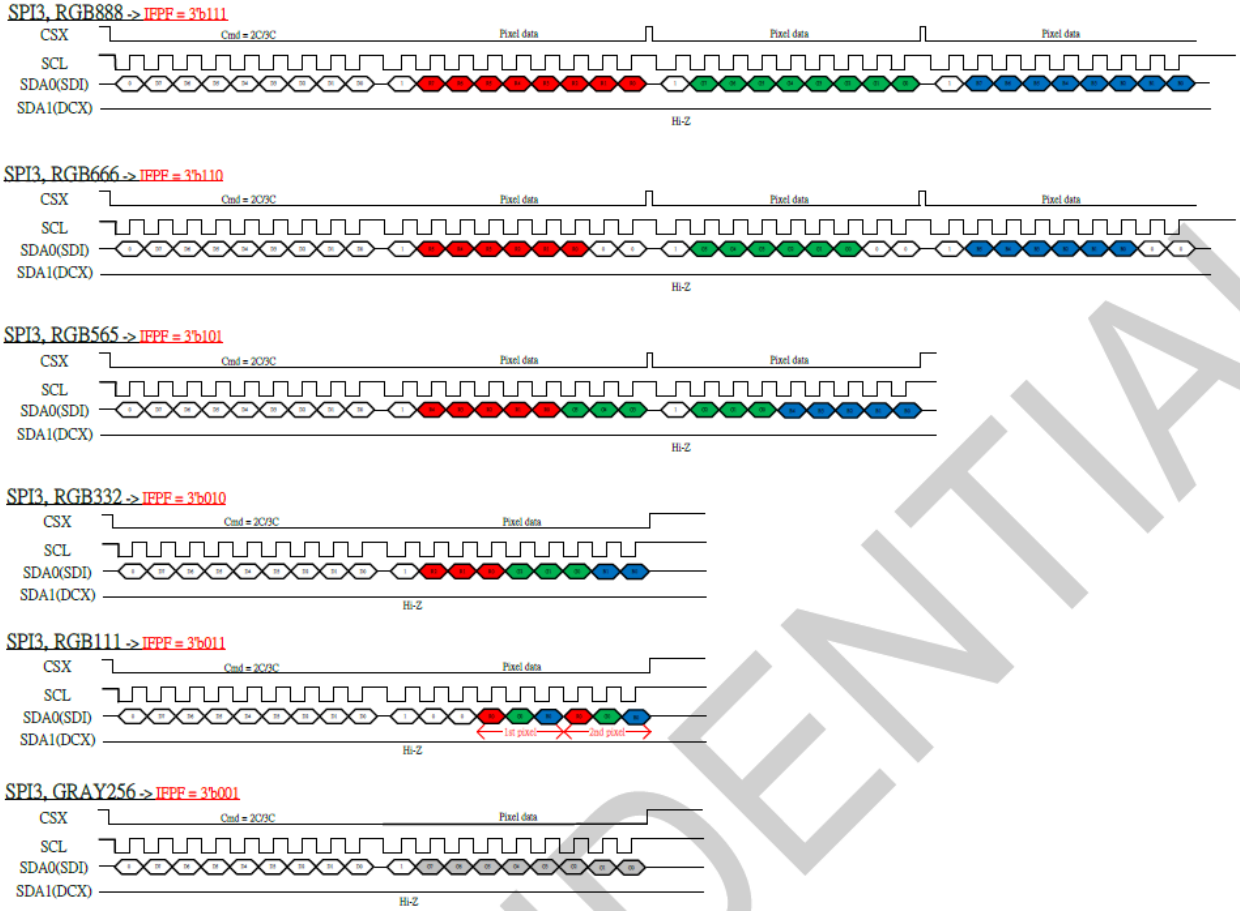


4-wire SPI

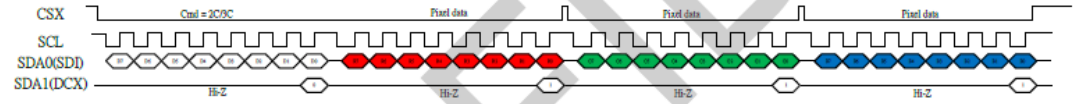


The 3-wire/4-wire SPI interface write display data sequences are described in the following figure.

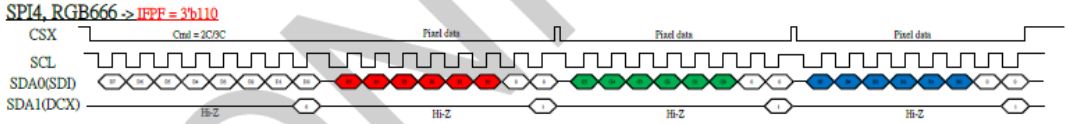
When DSPI_en =0, the host sends data by SDA only.



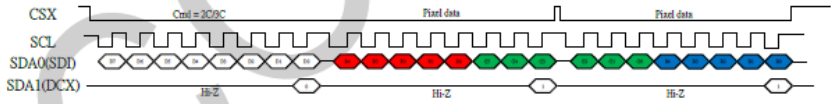
SPI4, RGB888 -> IFPF = 3'b111



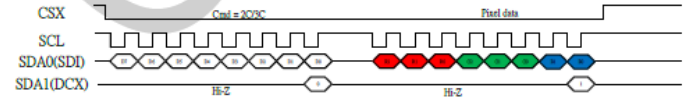
SPI4, RGB666 -> IFPF = 3'b110



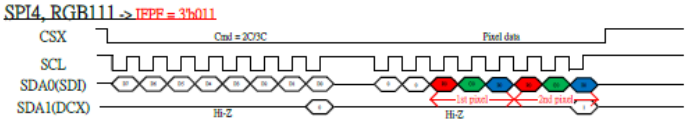
SPI4, RGB565 -> IFPF = 3'b101



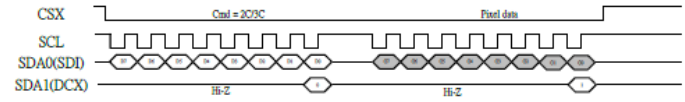
SPI4, RGB332 -> IFPF = 3'b010



SPI4, RGB111 -> IFPF = 3'b011

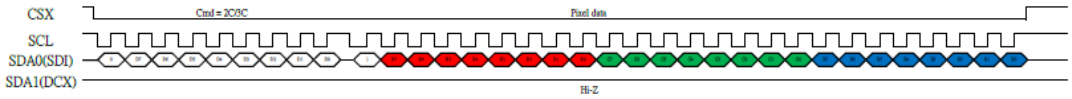


SPI4, GRAY256 -> IFPF = 3'b001

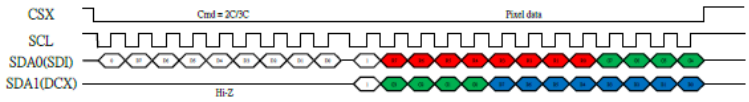


When DSPI_en =1, the host sends data by SDA and DCX.

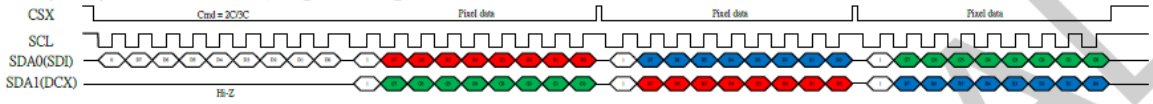
SPI3, 1wire, RGB888: IFPF = 3'b111, DSPI_EN = 1'b1, DSPI_CFG=2'b00



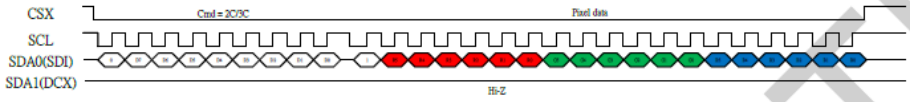
SPI3-1P1T, 2wire RGB888: IFPF = 3'b111, DSPI_EN=1'b1, DSPI_CFG=2'b10



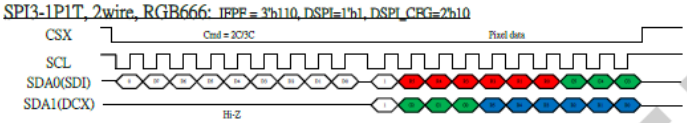
SPI3-2P3T, 2wire, RGB888: IFPF = 3'b111, DSPI_EN=1'b1, DSPI_CFG=2'b11



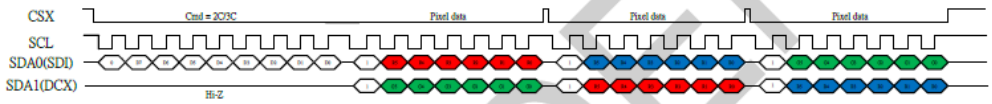
SPI3-1wire, RGB666: IFPF = 3'b110, DSPI_EN=1'b1, DSPI_CFG=2'b00



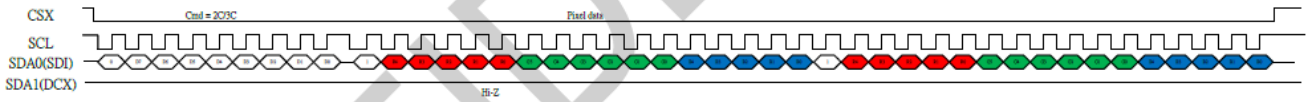
SPI3-1P1T, 2wire, RGB666: IFPF = 3'b110, DSPI=1'b1, DSPI_CFG=2'b10



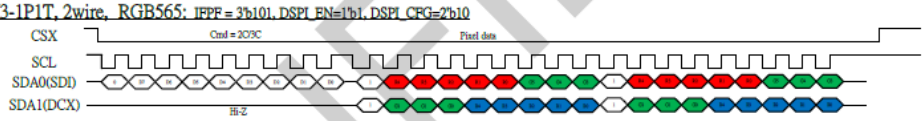
SPI3-2P3T, 2wire, RGB666: IFPF = 3'b110, DSPI_EN=1'b1, DSPI_CFG=2'b11



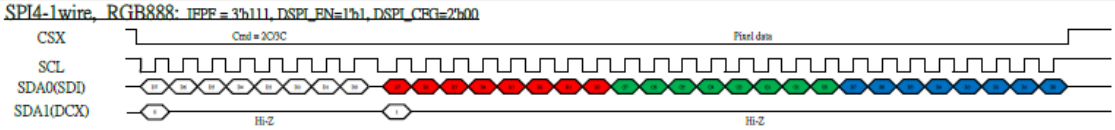
SPI3-1wire, RGB565: IFPF = 3'b101, DSPI_EN=1'b1, DSPI_CFG=2'b00



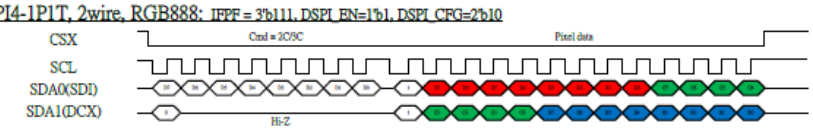
SPI3-1P1T, 2wire, RGB565: IFPF = 3'b101, DSPI_EN=1'b1, DSPI_CFG=2'b10



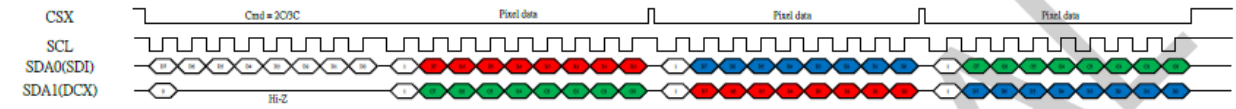
SPI4-1wire, RGB888: IFPF = 3'b111, DSPI_EN=1'b1, DSPI_CFG=2'b00



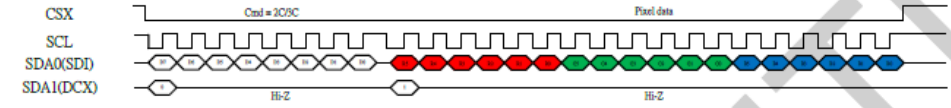
SPI4-1P1T, 2wire, RGB888: IFPF = 3'b111, DSPI_EN=1'b1, DSPI_CFG=2'b10



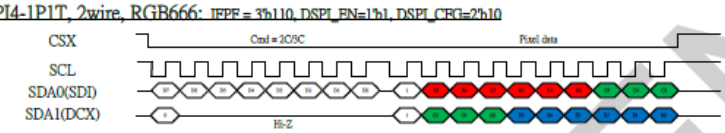
SPI4-2P3T, 2wire, RGB888: IFPF = 3'b111, DSPI_EN=1'b1, DSPI_CFG=2'b11



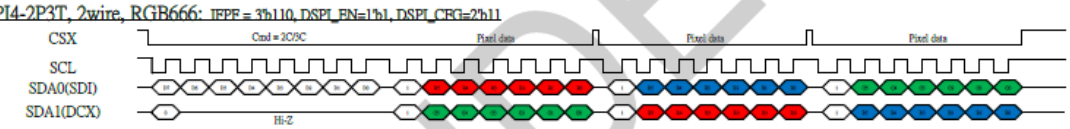
SPI4-1wire, RGB666: IFPF = 3'b110, DSPI_EN=1'b1, DSPI_CFG=2'b00



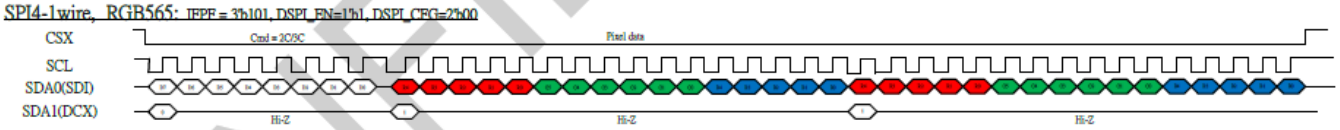
SPI4-1P1T, 2wire, RGB666: IFPF = 3'b110, DSPI_EN=1'b1, DSPI_CFG=2'b10



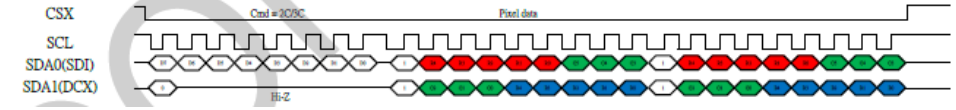
SPI4-2P3T, 2wire, RGB666: IFPF = 3'b110, DSPI_EN=1'b1, DSPI_CFG=2'b11



SPI4-1wire, RGB565: IFPF = 3'b101, DSPI_EN=1'b1, DSPI_CFG=2'b00

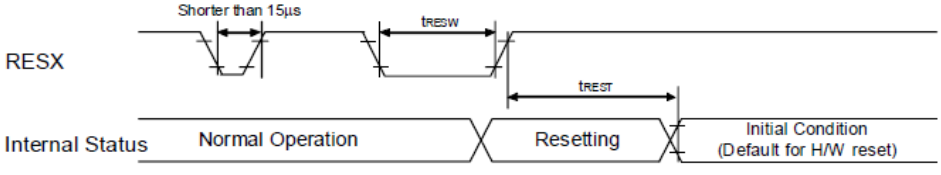


SPI4-1P1T, 2wire, RGB565: IFPF = 3'b101, DSPI_EN=1'b1, DSPI_CFG=2'b10



7.3 Display RESET Timing Characteristics

7.3.1 Reset Timing



IOVDD=1.65 to 1.95V, VDD=2.7 to 3.6V, AGND=DGND=0V, Ta=-40 to 85° C

7.3.2 Timing Parameters

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
tRESW	*1) Reset low pulse width	RESX	10	-	-	-	us
tREST	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-			120	When reset applied during Sleep out mode	ms

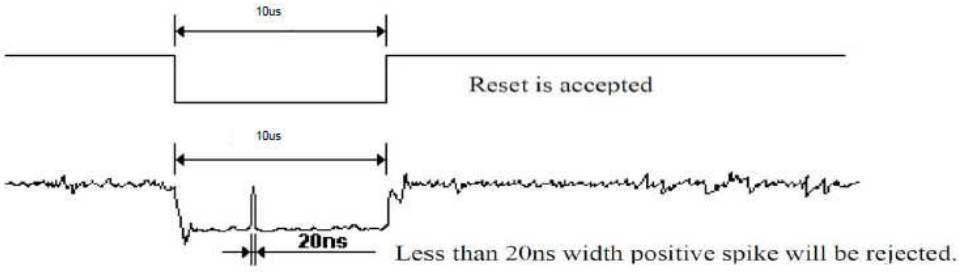
Note 1. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 15us	Reset starts (It depends on voltage and temperature condition.)

Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

Note 3. During Reset Complete Time, data in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.

Note 4. Spike Rejection also applies during a valid reset pulse as shown below:



Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8. Interface Pin Connection

8.1 Main FPC Pin assignment — AMOLED Panel Input /Output Signal Interface

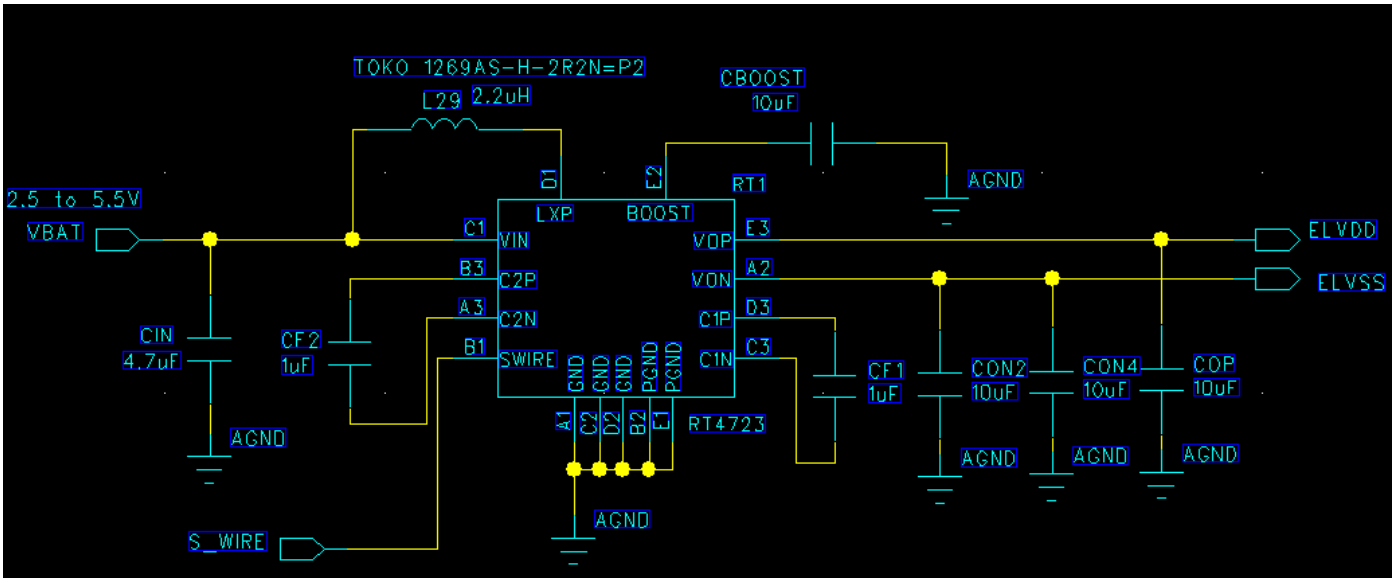
Pin No	Symbol	I/O	Function	Remark
1	**GND**	P	GND	
2	**RESX**	I	Device reset signal (0 : Enable ; 1: Disable)	
3	**HSSI_CLK_P**	I	MIPI positive clock signal	
4	**SWIRE**	O	SWIRE signal for PWR IC control	
5	**HSSI_CLK_N**	I	MIPI negative clock signal	
6	**MTP_PWR**	P	MTP(need to indicate to connect GND or NC)	
7	**GND**	P	GND	
8	**TE**	O	Vsync(vertical sync)signal output from panel to avoid tearing effect	
9	**HSSI_D0_P**	I/O	MIPI data positive signal	
10	**GND**	P	GND	
11	**HSSI_D0_N**	I/O	MIPI data negative signal	
12	**SDI**	I/O	Serial input signal in SPI I/F	
13	**GND**	P	GND	
14	**SCL**	I	Synchronous clock signal in SPI I/F	
15	**SDO**	O	Serial output signal in SPI I/F	
16	**CSX**	I	Chip select input pin in SPI I/F	
17	**DCX**	I	Display data/command selection in SPI I/F	
18	**VDDIO**	P	Power supply for Interface system	
19	**VCI**	P	Power supply for analog	
20	**GND**	P	GND	
21	**ELVSS**	P	AMOLED power Negative	
22	**ELVDD**	P	AMOLED power positive	
23	**ELVSS**	P	AMOLED power Negative	
24	**ELVDD**	P	AMOLED power positive	

Note1: I = input ; O = output ; P = Power ; I/O = input / output

Note2: If MIPI I/F not used, HSSI_CLK_P 、HSSI_CLK_N 、HSSI_D0_P 、HSSI_D0_N please connect to GND.

Note3:If SPI I/F not used, SCL & DCX please connect to GND, CSX please connect to VDDIO, SDI & SDO please leave it Open.

8.2 Power IC Application Circuit



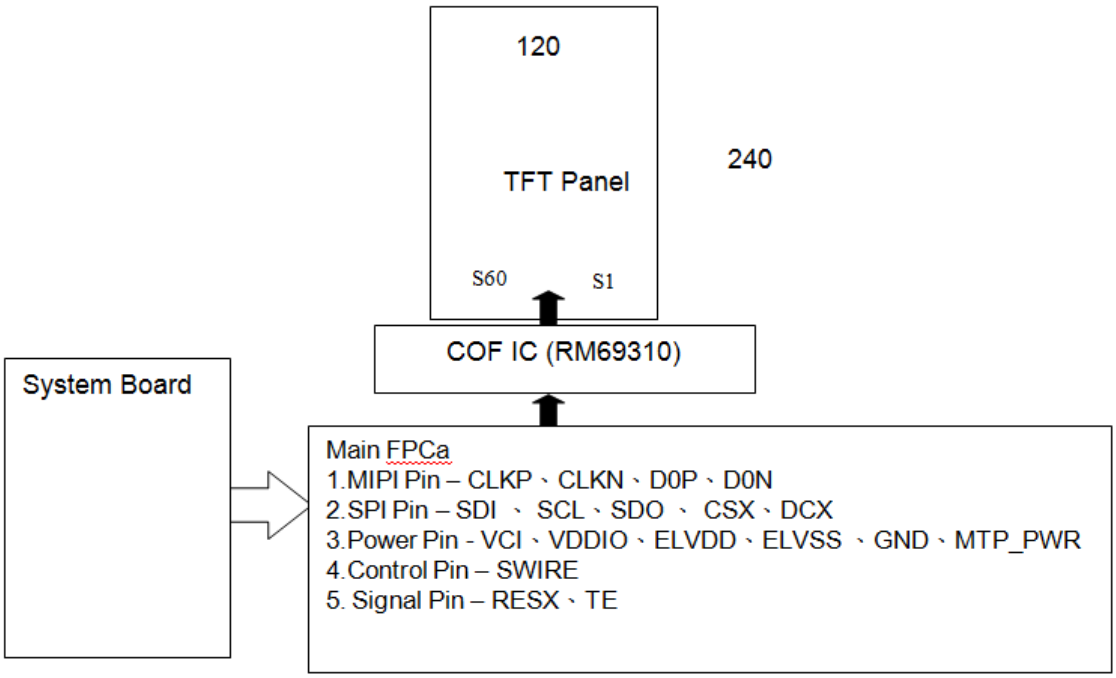
Note: OLED Power IC (RT4723)

Input: VBAT (2.5 ~ 5.5V)

Output: ELVDD, ELVSS

8.3 Display Initial Setting (TBD)

9. Block Diagram



10. Optical Specifications

(Ta = 25 ± 2℃,)

Item	Symbol		Condition	MIN	TYP	MAX	Unit	Remarks
Viewing Angle CR>1600	Top		-	80	-	-	Degree	Note 10.1 Note 10.8
	Bottom			80	-	-		
	Left			80	-	-		
	Right			80	-	-		
Contrast Ratio	CR		Θ=0°	-	10,000	-	-	Note 10.3 Note 10.8
Luminance	L		Θ=0°	300	350	-	cd/m^2	Note 10.5 Note 10.8
Uniformity	-		-	80	-	-	%	Note 10.6 Note 10.8
NTSC	-		-	85	100	-	%	Note 10.4 Note 10.8
Chromaticity	White	x	Θ=0°	0.270	0.300	0.330	-	Note 10.1 Note 10.4 Note 10.8
		y		0.280	0.310	0.340		
	Red	x		(0.641)	(0.671)	(0.701)		
		y		(0.297)	(0.327)	(0.357)		
	Green	x		(0.189)	(0.239)	(0.289)		
		y		(0.653)	(0.703)	(0.753)		
	Blue	x		(0.090)	(0.130)	(0.170)		
		y		(0.025)	(0.065)	(0.105)		
Response Time	Tr+Tf		Θ=0°	-	<4	-	ms	Note 10.7 Note 10.8
Gamma	-		-	1.9	2.2	2.5		

*( ): Means only for reference

Note 10.1 Definition of viewing angle range

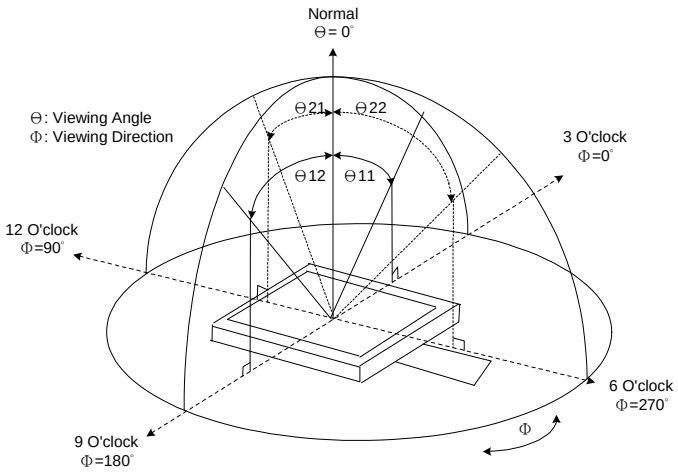


Fig. 10-1 Definition of viewing angle

Note 10.2 Measuring setup:

The module should be stabilized at a given temperature for 10 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting for 10 minutes in a windless room.

10.2.1 Driving voltage

ELVDD= 4.6V, ELVSS=-2.4V

10.2.2 Ambient temperature: Ta=25℃

10.2.3 Testing point: measure in the display center point and the test angle Θ=0°

10.2.4 Testing Facility

Environmental illumination: ≤ 1 Lux

Measurement equipment: DMS 900 series or similar equipment

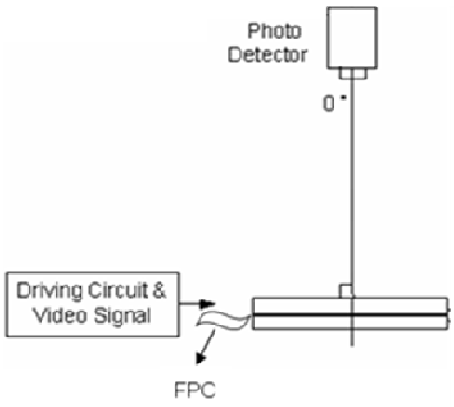


Fig. 10-2 Optical measurement system setup

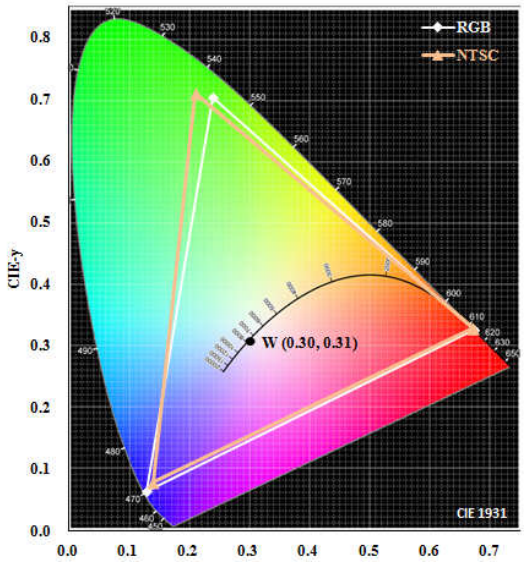
Note 10.3: Contrast ratio

$$CR = \frac{\text{Luminance with white image}}{\text{Luminance with black image}}$$

Note 10.4: Definition Chromaticity and NTSC ratio

Test Point: Display Center

$$\text{NTSC Ratio} = \frac{\text{Color gamut of panel RGB in CIE 1931 color space}}{\text{Color gamut of NTSC in CIE 1931 color space}}$$



Note 10.5: Luminance

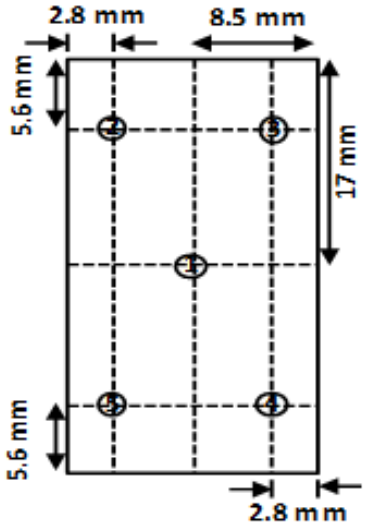
The measurement shall be done at the center of the display with a full white image.

Note 10.6: Uniformity

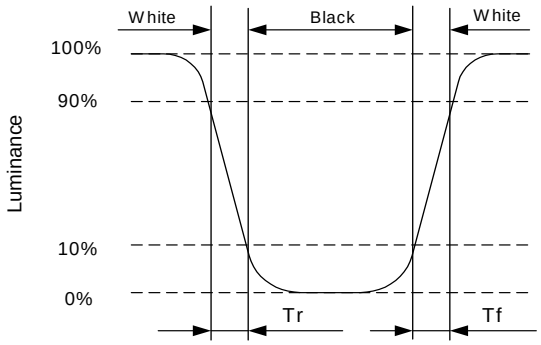
The luminance of 5 points in the figure shown below is measured and the uniformity is defined as the formula:

*

$$\text{Uniformity} = \frac{\text{The minimum luminance among 5 points}}{\text{The maximum luminance among 5 points}}$$



Note 10.7 Definition of response time: (Measure System: Photometer)



Note 10.8 The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted.

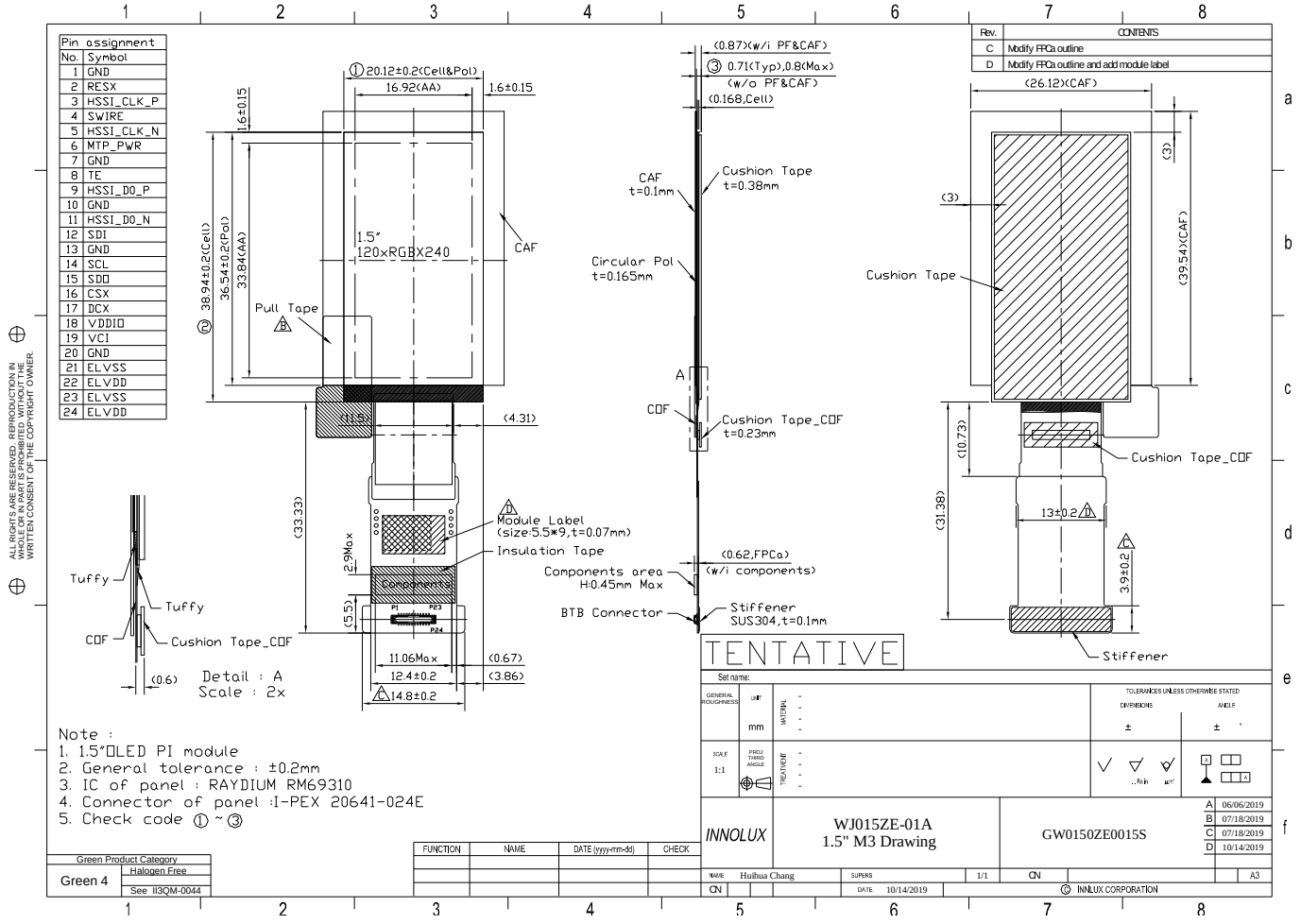
11. Reliability Test Items

No	Test Item	Condition	Remark
1	High Temperature Operation	Ta=60℃, 240Hrs	Note1, Note2
2	High Temperature Storage	Ta=70℃, 240Hrs	Note1, Note2
3	Low Temperature Operation	Ta=-20℃, 240Hrs	Note1, Note2
4	Low Temperature Storage	Ta=-30℃, 240Hrs	Note1, Note2
5	High Temperature & High Humidity Operation	Ta=60℃, RH=90%, 240Hrs	Note1, Note2
6	Thermal Shock	-30℃(30min)←→70℃(30min), 100Cycles	Note1, Note2
7	Vibration Test - Non Operation	1.5G / 10-500Hz, 30mins/cycle, 1cycle for each X, Y, Z	Note2
8	Package Vibration Test	1.14Grms [Spectrum： 1Hz(0.0001G2/Hz),4Hz(0.01G2/Hz),100Hz(0.01G2/Hz), 200Hz(0.001G2/Hz)] 30min/Bottom, 15min/Right-Left, 15min/Front-Back	Note2
9	Packing Drop test	1corner, 3edges, 6faces (1 time/direction) <follow ISTA(1A) height>	Note2

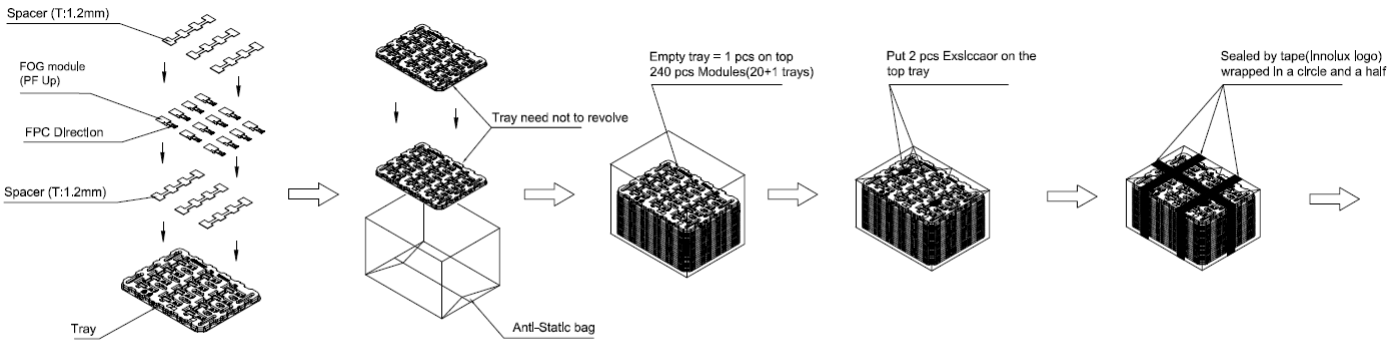
Note1: The test samples have recovery time for 2 hours at room temperature before the function check. In the standard conditions, there is no display function NG issue occurred.

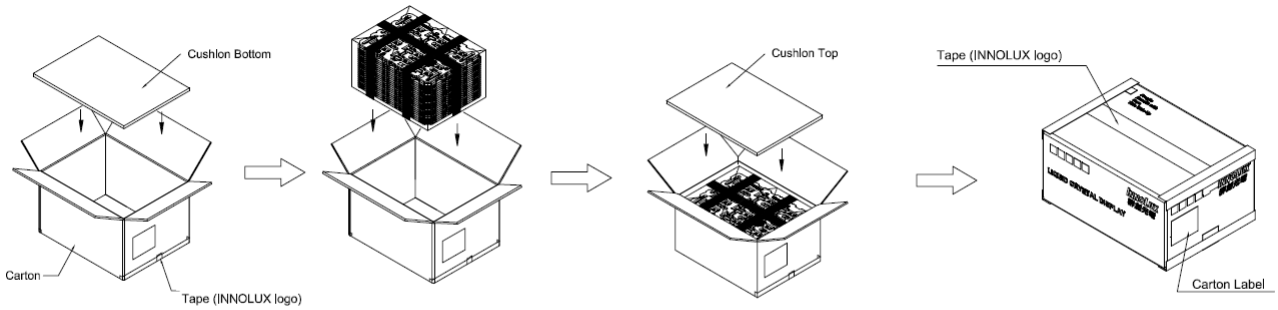
Note2: After the reliability test, the product only guarantees operation, but don't guarantee all of the cosmetic specification.

12. Outline Drawing



13. Package Form





(1) Carton Dimensions : 385(L)*290(W)*225(H)
(2) 240 FOG/Carton

14. Precautions

14.1 Adopt measures for good heat radiation. Be sure to use the module(panel) with in the specified temperature.

14.2 Avoid to display the fixed pattern in a long period, otherwise, it will cause image sticking.

14.3 Please operate module(panel) in suitable temperature. The performance will drift by different temperature.

14.4 Avoid dust or oil mist during assembly.

14.5 Follow the correct power on/off sequence while operating for preventing abnormal display or permanent damage to display.

14.6 Please be sure to turn-off the power when connecting or disconnecting the circuit.

14.7 High temperature and humidity may degrade performance. Please keep module away from direct sunlight or fluorescent light,

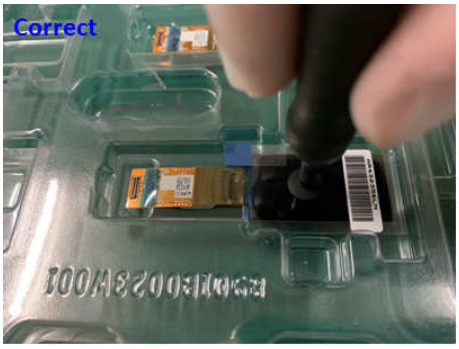
14.8 Avoid acetic acid or chlorine touch the AMOLED display module(panel).

14.9 Storage the modules(panel) in suitable environment with regular packing.

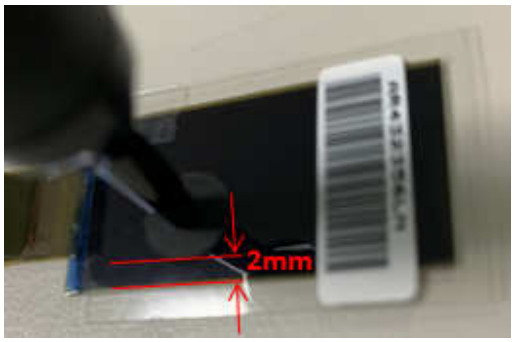
14.10 Polarizer scratches easily, please handle it carefully.

14.11 Sudden temperature changes cause condensation, and it will cause polarizer damaged.

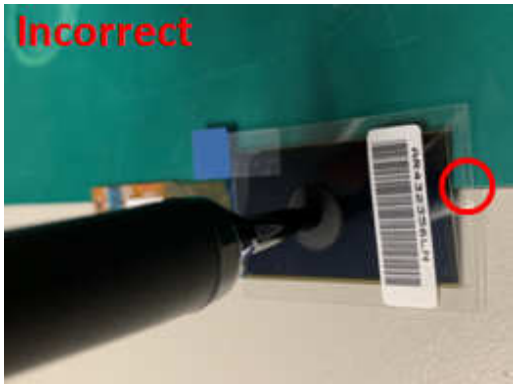
14.12 Please use a vacuum chuck to pick up a panel. Avoid using human hand directly contact panel.
(The vacuum chuck was certificated by ESD protection)



14.13 Please keep distance more than 2 mm from panel edge when the position of vacuum chuck contact panel.



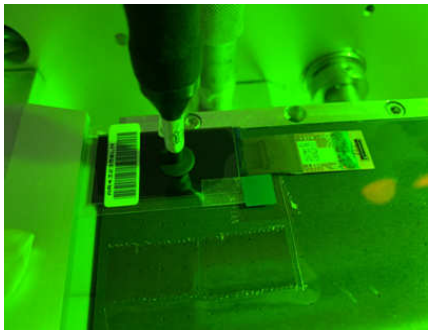
14.14 Please don't put the panel on the uneven surface



14.15 Please carefully transfer the panel, avoid the external force crashed panel edge.

14.16 Please put the panel down slowly, to avoid falling from the height of the panel.

14.17 Please put on the panel on vacuum equipment to remove the CAF, and use a vacuum chuck to pick up a panel.



14.18 Please use the pull tape to remove the CAF, and the remove direction from 7 clock to 1 clock.